SGLS286C – JUNE 2005 – REVISED SEPTEMBER 2008

14-Bit 125-MSPS Analog-to-Digital Converter

FEATURES

- 14-Bit Resolution
- 125−MSPS Sample Rate
- High Signal−to−Noise Ratio (SNR): 70.5 dBFS at 100 MHz f_{IN} (TYP)
- High Spurious−Free Dynamic Range (SFDR): 82 dBc at 100−MHz f_{IN} (TYP)
- 2.3-V_{PP} Differential Input Voltage
- Internal Voltage Reference
- 3.3-V Single-Supply Voltage
- Analog Power Dissipation: 578 mW
  - Total Power Dissipation: 780 mW
- Serial Programming Interface
- TQFP-64 PowerPAD™ Package

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (−55°C/125°C) Temperature Range(1)
- Extended Product Life Cycle
- Extended Product−Change Notification
- Product Traceability

(1) Custom temperature ranges available.

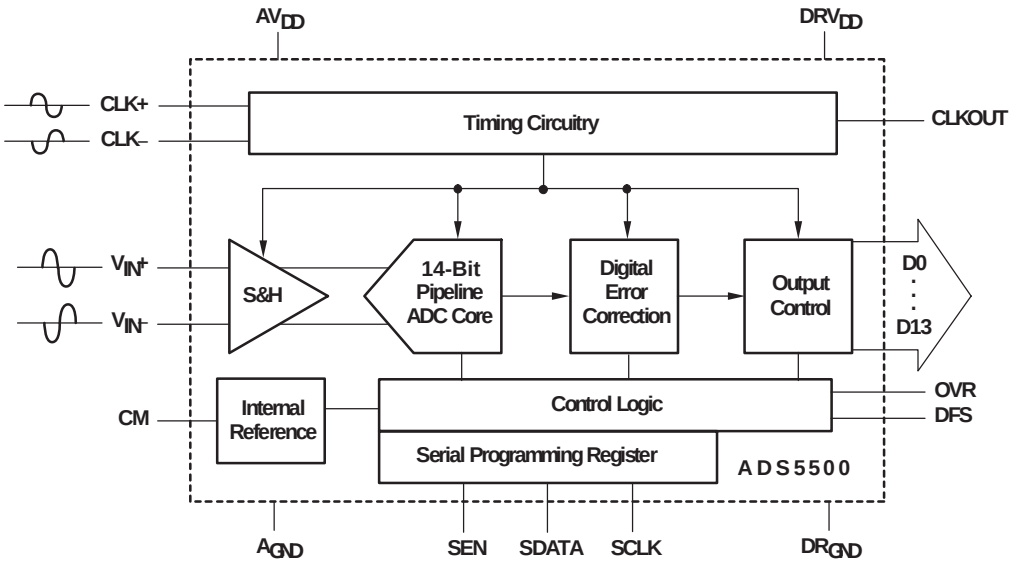
APPLICATIONS

- Wireless Communication
- Test and Measurement Instrumentation
- Single and Multichannel Digital Receivers
- Communication Instrumentation
  - Radar, Infrared
- Video and Imaging

DESCRIPTION

The ADS5500 is a high-performance, 14-bit 125−MSPS analog-to-digital converter (ADC). To provide a complete converter solution, it includes a high-bandwidth linear sample-and-hold stage (S&H) and internal reference. Designed for applications demanding the highest speed and highest dynamic performance in a small space, the ADS5500 has excellent power consumption of 780 mW at 3.3-V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements. A parallel CMOS-compatible output ensures seamless interfacing with common logic.

The ADS5500 is available in a 64-pin TQFP PowerPAD package and is specified over the full temperature range of −55°C to 125°C.



PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5500−EP	HTQFP-64(2) PowerPAD	PAP	−55°C to 125°C	ADS5500M	ADS5500MPAPEP	Tray, 160
					ADS5500MPAPREP	Tape and Reel, 1000

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 3,5 mm x 3,5 mm (min), 4 mm x 4 mm (max).

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		ADS5500-EP	UNIT
Supply Voltage	AV_{DD} to A_{GND}, DRV_{DD} to DR_{GND}	−0.3 to +3.7	V
	A_{GND} to DR_{GND}	±0.1	V
Analog input to A_{GND}		−0.15 to +2.5	V
Logic input to DR_{GND}		−0.3 to DRV_{DD} + 0.3	V
Digital data output to DR_{GND}		−0.3 to DRV_{DD} + 0.3	V
Input current (any input)		30	mA
Operating temperature range		−55 to +125	°C
Junction temperature		+142	°C
Storage temperature range		−65 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

TQFP−64 PowerPAD™ Package Thermal Characteristics

PARAMETER	SAME PACKAGE FORM WITHOUT PowerPAD	PowerPAD NOT CONNECTED TO PCB THERMAL PLAN	PowerPAD CONNECTED TO PCB THERMAL PLANE(2)
Thermal resistance, junction to ambient (see (1) and (2)), R_{TJA}	75.83ºC/W	42.2ºC/W	21.47ºC/W
Thermal resistance, junction to case (see (1) and (2)), R_{TJC}	7.8ºC/W	0.38ºC/W	0.38ºC/W

(1) Specified with the PowerPAD bond pad on the backside of the package soldered to a 2-oz Cu plate PCB thermal plane.

(2) Airflow is at 0 LFM (no airflow)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because small parametric changes could cause the device not to meet its published specifications.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
Supplies					
Analog supply voltage, AV_{DD}		3	3.3	3.6	V
Output driver supply voltage, DRV_{DD}		3	3.3	3.6	V
Analog Input					
Differential input range			2.3		V_{PP}
Input common-mode voltage, V_{CM}(1)		1.5		1.6	V
Digital Output					
Maximum output load			10		pF
Clock Input					
ADCLK input sample rate (sine wave) $1/t_C$	DLL ON	60		125	MSPS
	DLL OFF	10		80	
Clock amplitude, sine wave, differential(2)			3		V_{PP}
Clock duty cycle(3)			50%		
Open free-air temperature		−55		125	°C

(1) Input common-mode should be connected to CM.
(2) See Figure 14 for more information.
(3) See Figure 13 for more information.

Long-term high−temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See Figure 1 for additional information on thermal derating.

Electromigration failure mode applies to powered part; Kirkendall voiding failure mode is a function of temperature only.

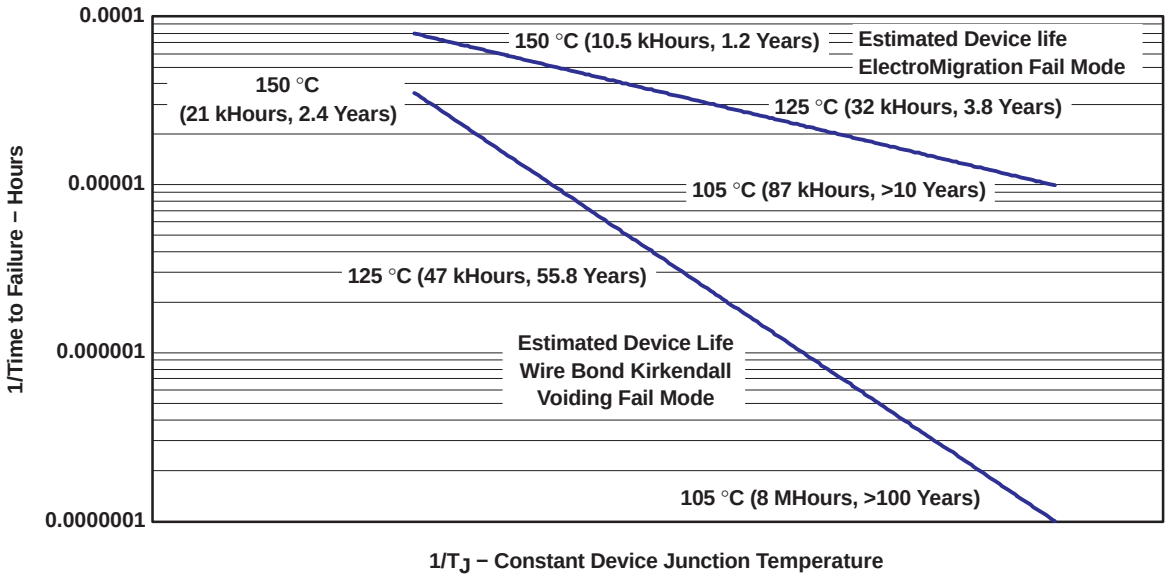


Figure 1. Time-to-Failure vs Junction Temperature

ELECTRICAL CHARACTERISTICS

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = −55°C to T_{MAX} = 125°C, sampling rate = 125 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, DLL On, −1−dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Resolution				14 Tested		Bits
Analog Inputs						
Differential input range				2.3		V_{PP}
Differential input impedance	See Figure 5			6.6		kΩ
Differential input capacitance	See Figure 5			4		pF
Total analog input common-mode current				4(1)		mA
Analog input bandwidth	Source impedance = 50 Ω			750		MHz
Conversion Characteristics						
Maximum sample rate			See note (2)		125	MSPS
Data latency	See timing diagram, See Figure 2			16.5		Clock Cycles
Internal Reference Voltages						
Reference bottom voltage, V_{REFM}				0.97		V
Reference top voltage, V_{REFP}				2.11		V
Reference error	Room temp		−4%		4%	
	Full temp range		−5%		5%	
Common-mode voltage output, V_{CM}				1.55 ±0.05		V
Dynamic DC Characteristics and Accuracy						
No missing codes				Tested		
Differential linearity error, DNL	f_{IN} = 10 MHz		−0.9	±0.75	1.1	LSB
Integral linearity error, INL	f_{IN} = 10 MHz	Room temp	−5		5	LSB
		Full temp range	−8		8	
Offset error				±1.5		mV
Offset temperature coefficient				0.0007		%/°C
Gain error				±0.45		%FS
Gain temperature coefficient				0.01		Δ%/°C
Dynamic AC Characteristics						
Signal-to-noise ratio (SNR)	f_{IN} = 10 MHz	Room temp	70.5	71.5		dBFS
		Full temp range	68	71.5		
	f_{IN} = 30 MHz			71.5		
	f_{IN} = 55 MHz			71.5		
	f_{IN} = 70 MHz	Room temp	70	71.2		
		Full temp range	66.5	71		
	f_{IN} = 100 MHz			70.5		
	f_{IN} = 150 MHz			70.1		
	f_{IN} = 225 MHz			69.1		
RMS output noise	Input tied to common-mode			1.1		LSB
Spurious-free dynamic range (SFDR)	f_{IN} = 10 MHz	Room temp	82	84		dBc
		Full temp range	76	84		
	f_{IN} = 30 MHz			84		
	f_{IN} = 55 MHz			79		
	f_{IN} = 70 MHz	Room temp	80	83		
		Full temp range	75	82		
	f_{IN} = 100 MHz			82		
	f_{IN} = 150 MHz			78		
	f_{IN} = 225 MHz			74		

(1) 2-mA per input
(2) See *Recommended Operating Conditions*.

ELECTRICAL CHARACTERISTICS(continued)

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = −55°C to T_{MAX} = 125°C, sampling rate = 125 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, DLL On, −1−dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Second−harmonic (HD2)	f_{IN} = 10 MHz	Room temp	82	91		dBc
		Full temp range	77	86		
	f_{IN} = 30 MHz			86		
	f_{IN} = 55 MHz			84		
	f_{IN} = 70 MHz	Room temp	80	87		
		Full temp range	75	83		
	f_{IN} = 100 MHz			84		
	f_{IN} = 150 MHz			78		
	f_{IN} = 225 MHz			74		
Third harmonic (HD3)	f_{IN} = 10 MHz	Room temp	82	89		dBc
		Full temp range	77	88		
	f_{IN} = 30 MHz			90		
	f_{IN} = 55 MHz			79		
	f_{IN} = 70 MHz	Room temp	80	85		
		Full temp range	75	82		
	f_{IN} = 100 MHz			82		
	f_{IN} = 150 MHz			80		
	f_{IN} = 225 MHz			76		
Worst-harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz	Room temp		88		dBc
	f_{IN} = 70 MHz	Room temp		86		
Signal-to-noise + distortion (SINAD)	f_{IN} = 10 MHz	Room temp	69	70		dBc
		Full temp range	66.5	70		
	f_{IN} = 30 MHz			70		
	f_{IN} = 55 MHz			69.5		
	f_{IN} = 70 MHz	Room temp	68.5	69		
		Full temp range	65	69.5		
	f_{IN} = 100 MHz			69		
	f_{IN} = 150 MHz			69		
	f_{IN} = 225 MHz			66.4		
Total harmonic distortion (THD)	f_{IN} = 10 MHz	Room temp	80	85		dBc
		Full temp range	76	83		
	f_{IN} = 30 MHz			82		
	f_{IN} = 55 MHz			77		
	f_{IN} = 70 MHz	Room temp	77.5	81		
		Full temp range	74	79.5		
	f_{IN} = 100 MHz			79		
	f_{IN} = 150 MHz			75		
	f_{IN} = 225 MHz			71.8		

ELECTRICAL CHARACTERISTICS(continued)

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = −55°C to T_{MAX} = 125°C, sampling rate = 125 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, DLL On, −1−dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Effective number of bits (ENOB)	f_{IN} = 70 MHz		11.3		Bits
Two-tone intermodulation distortion (IMD)	f = 10.1 MHz, 15.1 MHz (−7 dBFS each tone)		85		dBc
	f = 30.1 MHz, 35.1 MHz (−7 dBFS each tone)		85		
	f = 50.1 MHz, 55.1 MHz (−7 dBFS each tone)		88		
Power Supply					
Total supply current, I_{CC}	V_{IN} = full-scale, f_{IN} = 5 5 MHz, AV_{DD} = DRV_{DD} = 3.3V		236	265	mA
Analog supply current, I_{AVDD}	V_{IN} = full-scale, f_{IN} = 5 5 MHz, AV_{DD} = DRV_{DD} = 3.3V		175	190	mA
Output buffer supply current, I_{DRVDD}	V_{IN} = full-scale, f_{IN} = 55 MHz, AV_{DD} = DRV_{DD} = 3.3 V		61	75	mA
Power dissipation	Analog only		578	627	mW
	Total power with 10−pF load on digital output to ground		780	875	mW
Standby power	With clocks running		181	250	mW

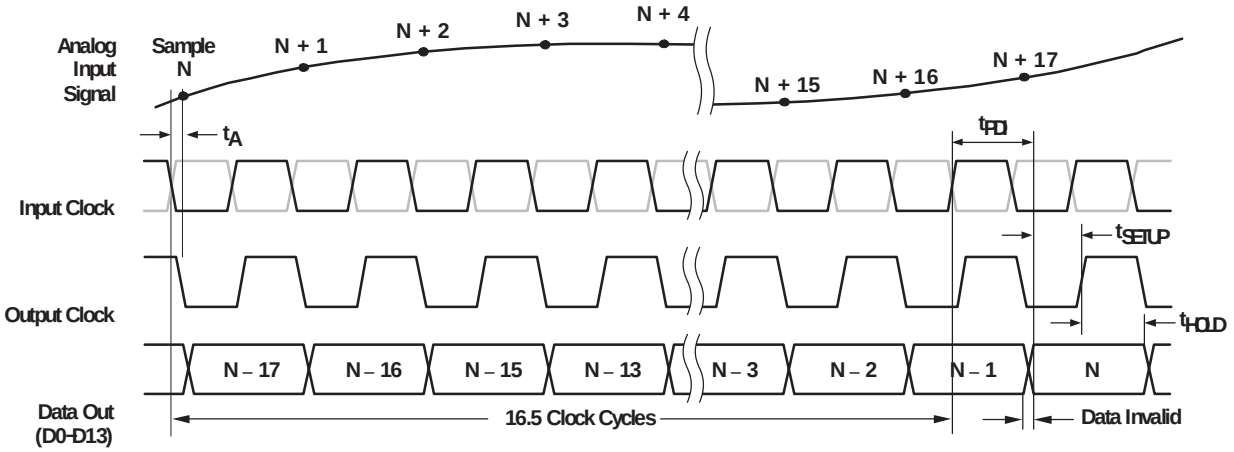
DIGITAL CHARACTERISTICS

Typ, min, and max values at T_A = 25°C, full temperature range is T_{MIN} = −55°C to T_{MAX} = 125°C, sampling rate = 125 MSPS, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, DLL On, −1 dBFS differential input, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current				10	µA
Low-level input current				10	µA
Input current for RESET			−20		µA
Input capacitance			4		pF
Digital Outputs(1)					
Low-level output voltage	C_{LOAD} = 10 pF(2), f_S = 125 MSPS		0.3		V
High-level output voltage	C_{LOAD} = 10 pF(2), f_S = 125 MSPS		3		V
Output capacitance			3		pF

(1) For optimal performance, all digital output lines (D0:D13), including the output clock, should see a similar load.
(2) Equivalent capacitance to ground of (load + parasitics of transmission lines)

TIMING CHARACTERISTCS



NOTE: It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

Figure 2. Timing Diagram

TIMING CHARACTERISTICS (1)

Typ, min, and max values at T_A = 25°C, min and max specified over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, 3−V_{PP} differential clock, and C_{LOAD} = 10 pF (unless otherwise noted)

PARAMETER	DESCRIPTION	TYP	UNIT
Switching Specification			
Aperture delay, t_A	Input CLK falling edge to data sampling point	1	ns
Aperture jitter (uncertainty)	Uncertainty in sampling instant	300	fs
Data setup time, t_{SU}	Data valid(2) to 50% of CLKOUT rising edge	2.5	ns
Data hold time, t_h	50% of CLKOUT rising edge to data becoming invalid(2)	2.1	ns
Input clock to output data valid start(3)(4), t_{START}	Input clock rising edge to Data valid start delay	2.2	ns
Input clock to output data valid end(3)(4), t_{END}	Input clock rising edge to Data valid end delay	6.9	ns
Output clock jitter, t_{JIT}	Uncertainty in CLKOUT rising edge, peak−to−peak	150	ps
Output clock rise time, t_r	Rise time of CLKOUT measured from 20% to 80% of DRVDD	1.7	ns
Output clock fall time, t_f	Fall time of CLKOUT measured from 80% to 20% of DRVDD	1.5	ns
Input clock to output clock delay, t_{PDI}	Input clock rising edge, zero crossing, to output clock rising edge 50%	4.8	ns
Data rise time, t_r	Data rise time measured from 20% to 80% of DRVDD	3.6	ns
Data fall time, t_f	Data fall time measured from 80% to 20% of DRVDD	2.8	ns
Latency Time for a sample to propagate to the ADC outputs 17.5 clock cycles		17.5	Clock Cycles

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) Data valid refers to 2 V for LOGIC high and 0.8 V for LOGIC low.
(2) See the *Output Information* section for details on using the input clock for data capture.
(4) These specifications apply when the CLKOUT polarity is set to rising edge (according to Table 3). Add one−half clock period for the valid number for a falling−edge CLKOUT polarity.

RESET TIMING CHARACTERISTICS

Typ, min, and max values at T_A = 25°C, min and max specified over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, 3−V_{PP} differential clock (unless otherwise noted)

PARAMETER	DESCRIPTION	TYP	UNIT
Switching Specification			
Power−up time	Delay from power−up of AV_{DD} and DRV_{DD} to output stable	40	ms

SERIAL PROGRAMMING INTERFACE CHARACTERISTICS

The device has a three-wire serial interface. The device latches the serial data SDATA on the falling edge of serial clock SCLK when SEN is active.

- Serial shift of bits is enabled when SEN is low. SCLK shifts serial data at falling edge.
- Minimum width of data stream for a valid loading is 16 clocks.
- Data is loaded at every 16th SCLK falling edge while SEN is low.
- In case the word length exceeds a multiple of 16 bits, the excess bits are ignored.
- Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

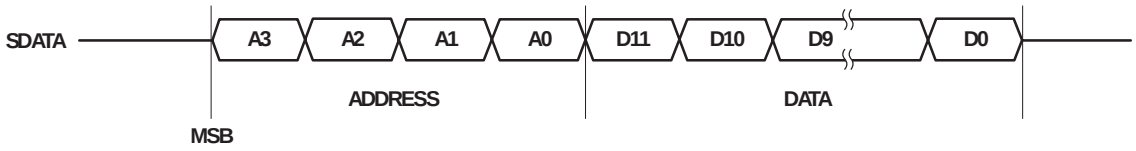


Figure 3. DATA Communication Is 2 Byte, MSB First

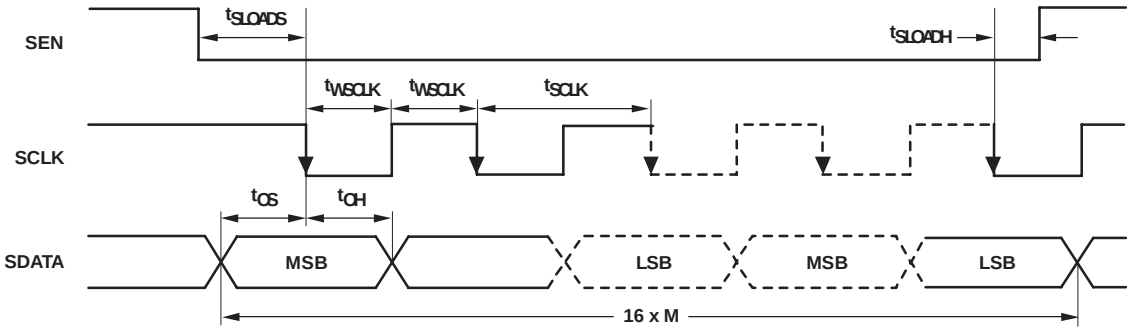


Figure 4. Serial Programming Interface Timing Diagram

Table 1. Serial Programming Interface Timing Characteristics

SYMBOL	PARAMETER	MIN(1)	TYP(1)	MAX(1)	UNIT
t_{SCLK}	SCLK period	50			ns
t_{WSCLK}	SCLK duty cycle	25%	50%	75%	
t_{SLOADS}	SEN to SCLK setup time	8			ns
t_{SLOADH}	SCLK to SEN hold time	6			ns
t_{DS}	Data setup time	8			ns
t_{DH}	Data hold time	6			ns

(1) Min, typ, and max values are characterized, but not production tested.

Table 2. Serial Register Table

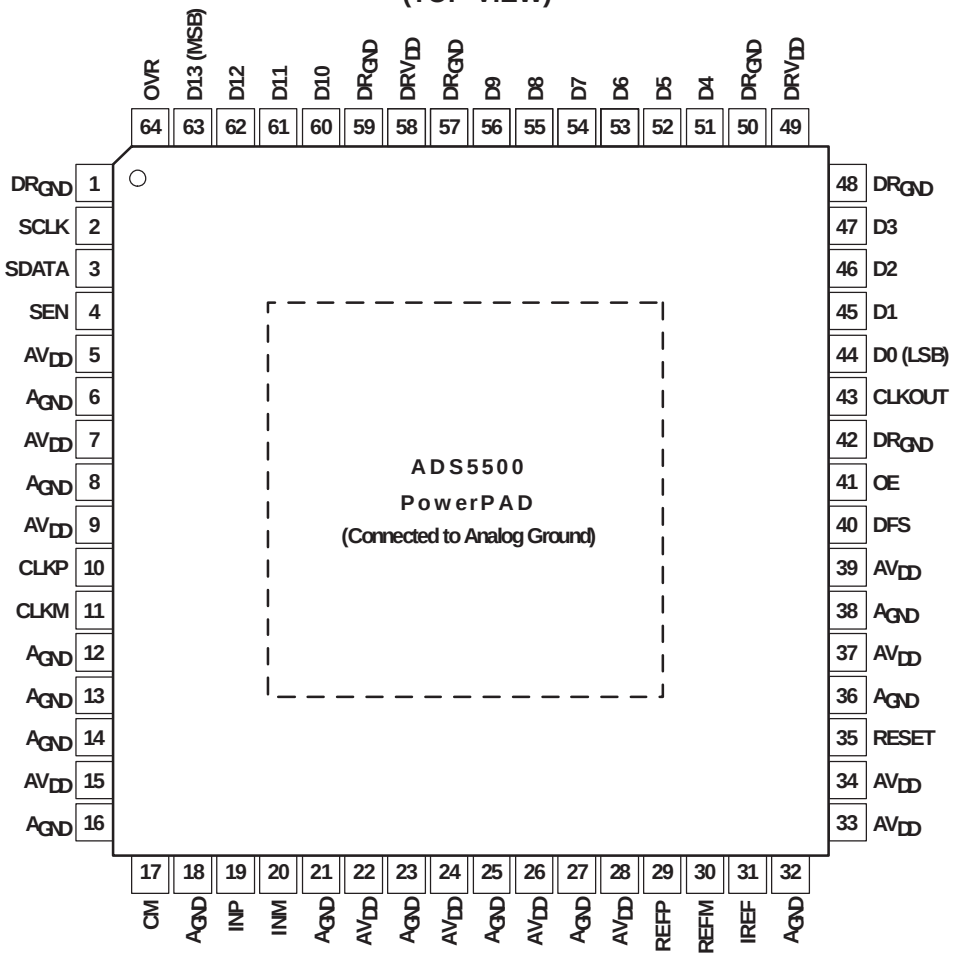
A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	1	0	1	0	0	0	0	0	0	0	0	0	0	DLL OFF	0	DLL OFF = 0: Internal DLL is on, recommended for 60−125 MSPS clock speed DLL OFF = 1: Internal DLL is off, recommended for 10−80 MSPS clock speed
1	1	1	0	0	TP<1>	TP<0>	0	0	0	0	0	0	0	0	0	TP<1:0>: Test modes for output data capture TP<1> = 0, TP<0> = 0: Normal mode of operation, TP<1> = 0 TP<0> = 1: All output lines are pulled to ’0’, TP<1> = 1 TP<0> = 0: All output lines are pulled to ’1’, TP<1> = 1 TP<0> = 1: A continuous stream of ’10’ comes out on all output lines
1	1	1	1	PDN	0	0	0	0	0	0	0	0	0	0	0	PDN = 0: Normal mode of operation, PDN = 1: Device is put in power down (low current) mode

Table 3. DATA FORMAT SELECT (DFS TABLE)

DFS-PIN VOLTAGE (V_{DFS})	DATA FORMAT	CLOCK OUTPUT POLARITY
$V_{DFS} < \frac{1}{6} \times AV_{DD}$	Straight binary	Data valid on rising edge
$\frac{5}{12} \times AV_{DD} > V_{DFS} > \frac{1}{3} \times AV_{DD}$	Twos complement	Data valid on rising edge
$\frac{2}{3} \times AV_{DD} > V_{DFS} > \frac{7}{12} \times AV_{DD}$	Straight binary	Data valid on falling edge
$V_{DFS} > \frac{5}{6} \times AV_{DD}$	Twos complement	Data valid on falling edge

PIN CONFIGURATION

PAP PACKAGE
(TOP VIEW)



PIN ASSIGNMENTS

TERMINAL NAME	TERMINAL NO.	NO. OF PINS	I/O	DESCRIPTION
AV_{DD}	5, 7, 9, 15, 22, 24, 26, 28, 33, 34, 37, 39	12	I	Analog power supply
A_{GND}	6, 8, 12, 13, 14, 16, 18, 21, 23, 25, 27, 32, 36, 38	14	I	Analog ground
DRV_{DD}	49, 58	2	I	Output driver power supply
DR_{GND}	1, 42, 48, 50, 57, 59	6	I	Output driver ground
INP	19	1	I	Differential analog input (positive)
INM	20	1	I	Differential analog input (negative)
REFP	29	1	O	Reference voltage (positive), 0.1-μF capacitor in series with a 1-Ω resistor to GND
REFM	30	1	O	Reference voltage (negative), 0.1-μF capacitor in series with a 1-Ω resistor to GND
IREF	31	1	I	Current set, 56-kΩ resistor to GND, do not connect capacitors
CM	17	1	O	Common-mode output voltage
RESET	35	1	I	Reset (active high), 200-kΩ resistor to AV_{DD}
OE	41	1	I	Output enable (active high)
DFS	40	1	I	Data format and clock out polarity select(1)
CLKP	10	1	I	Data converter differential input clock (positive)
CLKM	11	1	I	Data converter differential input clock (negative)
SEN	4	1	I	Serial interface chip select
SDATA	3	1	I	Serial interface data
SCLK	2	1	I	Serial interface clock
D0 (LSB)−D13 (MSB)	44−47, 51−56, 60−63	14	O	Parallel data output
OVR	64	1	O	Over-range indicator bit
CLKOUT	43	1	O	CMOS clock out in sync with data

NOTE: PowerPAD is connected to analog ground.

(1) The DFS pin is programmable to four discrete voltage levels: 0, 3/8 AV_{DD}, 5/8 AV_{DD}, and AV_{DD}. The thresholds are centered. More details are listed in Table 3 on page 11.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB

Aperture Delay

The delay in time between the falling edge of the input sampling clock and the actual time at which the sampling occurs

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay

Clock Pulse Width/Duty Cycle

A perfect differential sine−wave clock results in a 50% clock duty cycle on the internal coversion clock. Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic 1 state to achieve rated performance. Pulse width low is the minimum time that the ENCODE pulse should be left in a low state (logic 0). At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly one LSB apart. DNL is the deviation of any single LSB transition at the digital output from an ideal one LSB step at the analog input. If a device claims to have no missing codes, it means that all possible codes (for a 14-bit converter, 16384 codes) are present over the full operating range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine−wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

If SINAD is not known, SNR can be used exceptionally to calculate ENOB ($ENOB_{SNR}$).

Effective Resolution Bandwidth

The highest input frequency where the SNR (dB) is dropped by 3 dB for a full-scale input amplitude

Gain Error

The amount of deviation between the ideal transfer function and the measured transfer function (with the offset error removed) when a full-scale analog input voltage is applied to the ADC, resulting in all ones in the digital code. Gain error is usually given in LSB or as a percent of full-scale range (%FSR).

Integral Nonlinearity (INL)

The deviation of the transfer function from a reference line measured in fractions of one LSB using a *best straight line* or *best fit* determined by a least square curve fit. INL is independent from effects of offset, gain, or quantization errors.

Maximum Conversion Rate

The encode rate at which parametric testing is performed. This is the maximum sampling rate where certified operation is given.

Minimum Conversion Rate

The minimum sampling rate where the ADC still works.

Nyquist Sampling

When the sampled frequencies of the analog input signal are below $f_{CLOCK}/2$, it is called Nyquist sampling. The Nyquist frequency is $f_{CLOCK}/2$, which can vary depending on the sample rate (f_{CLOCK}).

Offset Error

The deviation of output code from mid-code when both inputs are tied to common-mode

Propagation Delay

The delay between the input clock rising edge and the time when all data bits are within valid logic levels

Signal-to-Noise and Distortion (SINAD)

The RMS value of the sine wave f_{IN} (input sine wave for an ADC) to the RMS value of the noise of the converter from DC to the Nyquist frequency, including harmonic content. It is typically expressed in decibels (dB). SINAD includes harmonics, but excludes DC.

$$\text{SINAD} = 20\text{Log}_{(10)}\frac{\text{Input}(V_S)}{\text{Noise} + \text{Harmonics}}$$

Signal-to-Noise Ratio (Without Harmonics)

SNR is a measure of signal strength relative to background noise. The ratio is usually measured in dB. If the incoming signal strength in μV is V_S, and the noise level (also in μV) is V_N, the SNR in dB is given by the formula:

$$\text{SNR} = 20\text{Log}_{(10)}\frac{V_S}{V_N}$$

This is the ratio of the RMS signal amplitude, V_S (set one dB below full-scale), to the RMS value of the sum of all other spectral components, V_N, excluding harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the RMS value of the analog input sine wave to the RMS value of the peak spur observed in the frequency domain. It may be reported in dBc (that is, it degrades as signal levels are lowered), or in dBFS (always related back to converter full-scale). The peak spurious component may or may not be a harmonic.

Temperature Drift

Temperature drift (for offset error and gain error) specifies the maximum change from the initial temperature value to the value at T_{MIN} or T_{MAX}.

Total Harmonic Distortion (THD)

The ratio of the RMS signal amplitude of the input sine wave to the RMS value of distortion appearing at multiples (harmonics) of the input, typically given in dBc

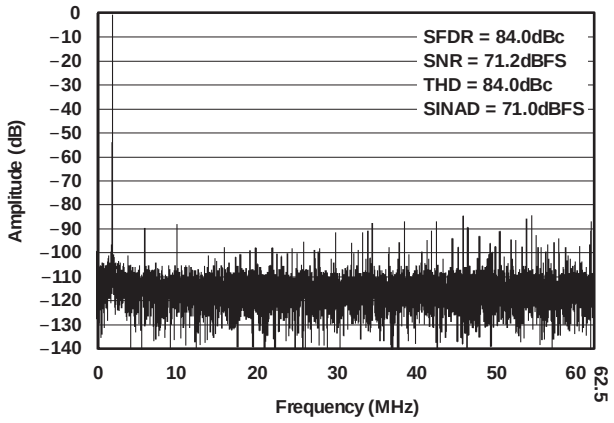
Two-Tone Intermodulation Distortion Rejection

The ratio of the RMS value of either input tone (f_1, f_2) to the RMS value of the worst third-order intermodulation product ($2f_1 - f_2$; $2f_2 - f_1$). It is reported in dBc.

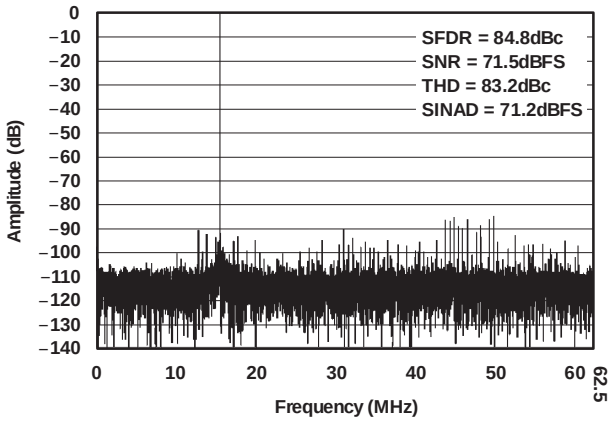
TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)

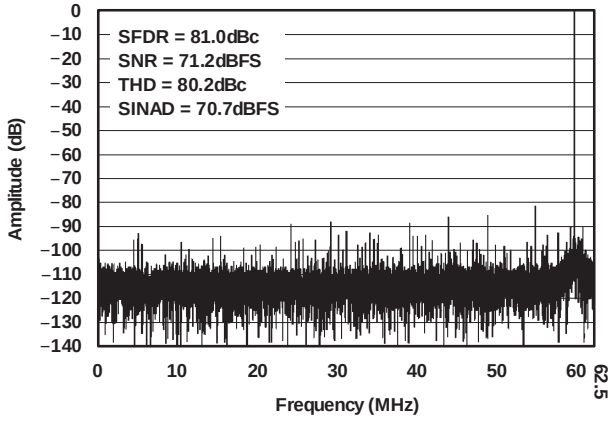
SPECTRAL PERFORMANCE
(FFT for 2MHz Input Signal)



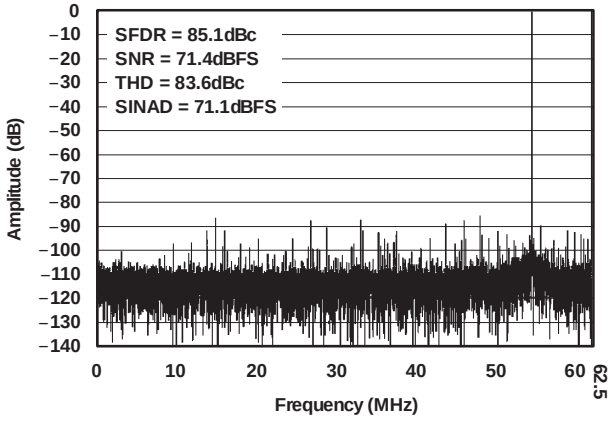
SPECTRAL PERFORMANCE
(FFT for 15MHz Input Signal)



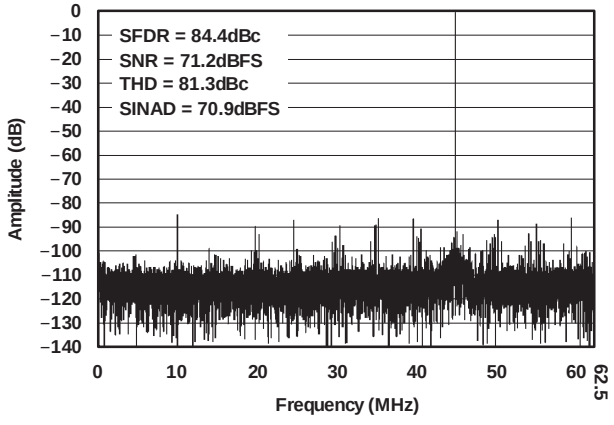
SPECTRAL PERFORMANCE
(FFT for 60MHz Input Signal)



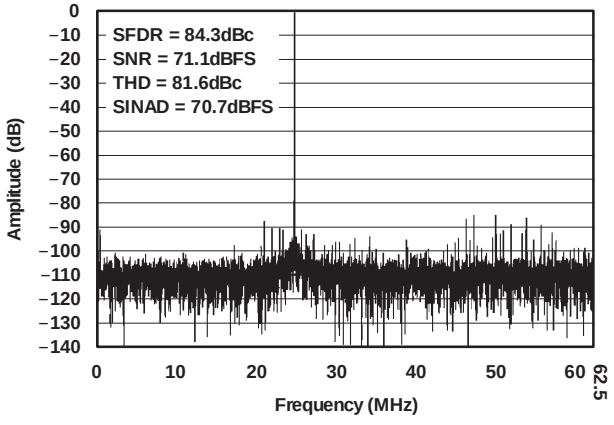
SPECTRAL PERFORMANCE
(FFT for 70MHz Input Signal)



SPECTRAL PERFORMANCE
(FFT for 80MHz Input Signal)



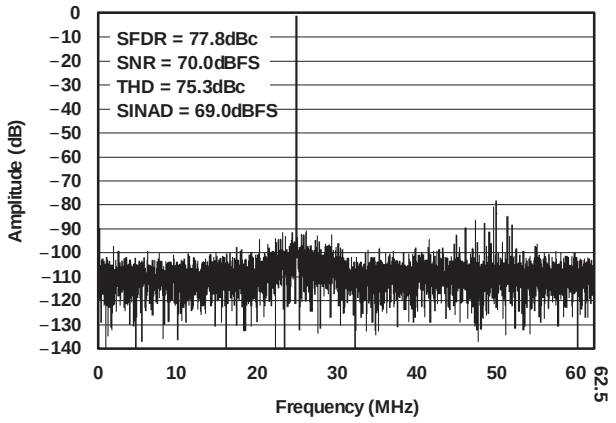
SPECTRAL PERFORMANCE
(FFT for 100MHz Input Signal)



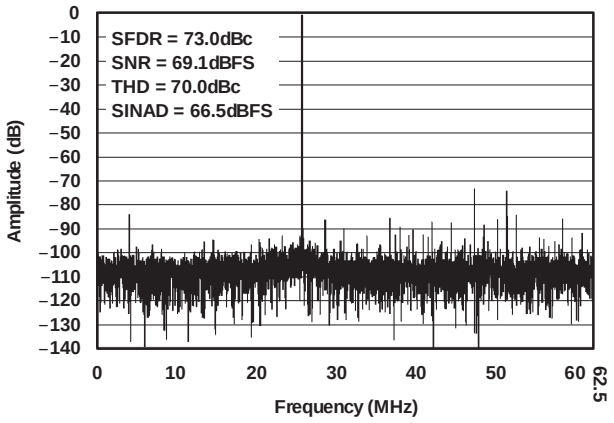
TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)

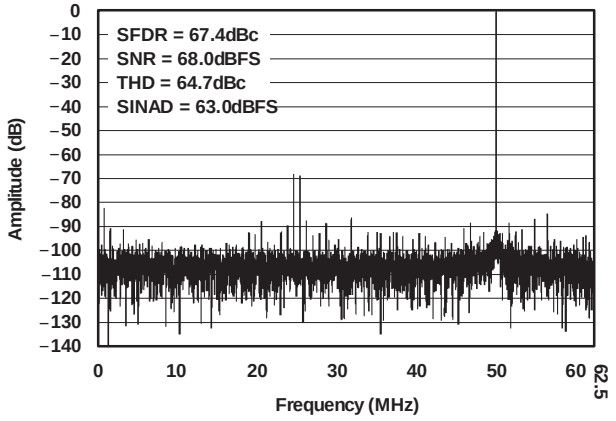
SPECTRAL PERFORMANCE
(FFT for 150MHz Input Signal)



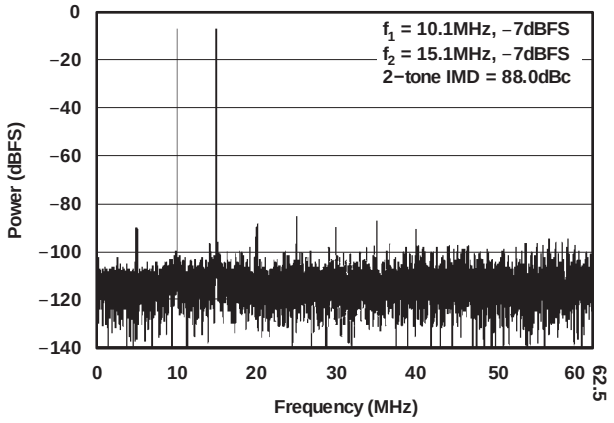
SPECTRAL PERFORMANCE
(FFT for 225MHz Input Signal)



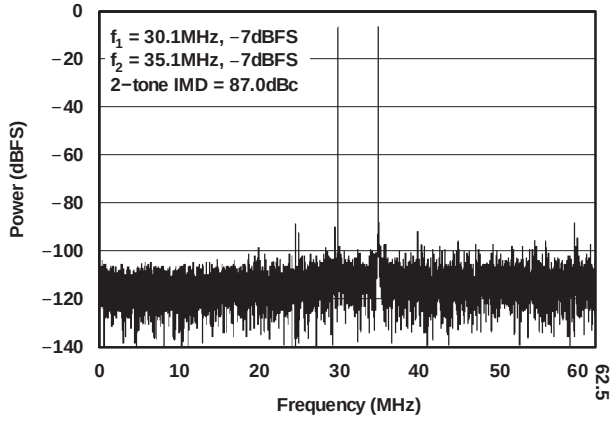
SPECTRAL PERFORMANCE
(FFT for 300MHz Input Signal)



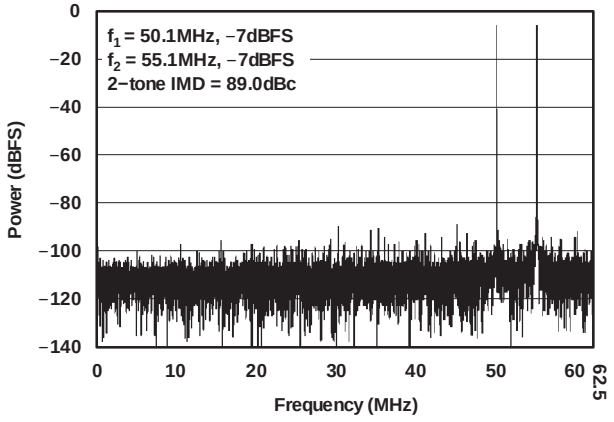
TWO−TONE INTERMODULATION



TWO−TONE INTERMODULATION



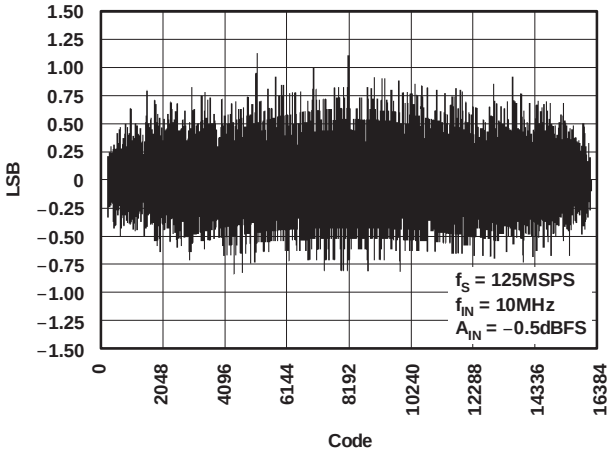
TWO−TONE INTERMODULATION



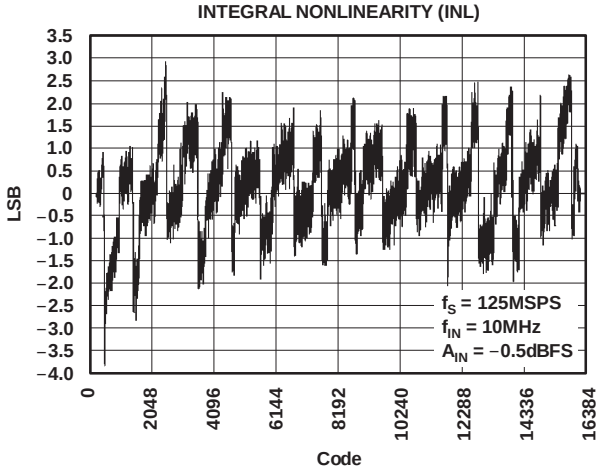
TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)

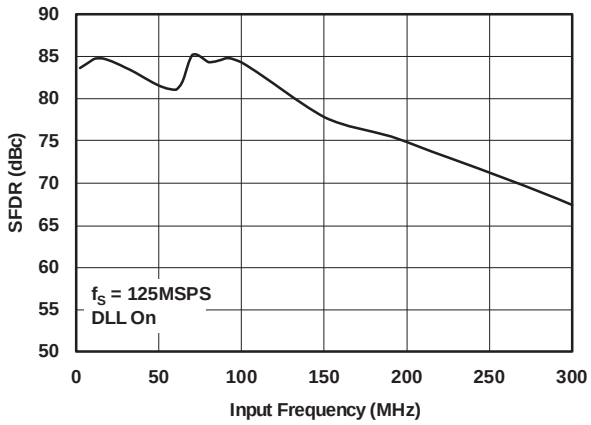
DIFFERENTIAL NONLINEARITY (DNL)



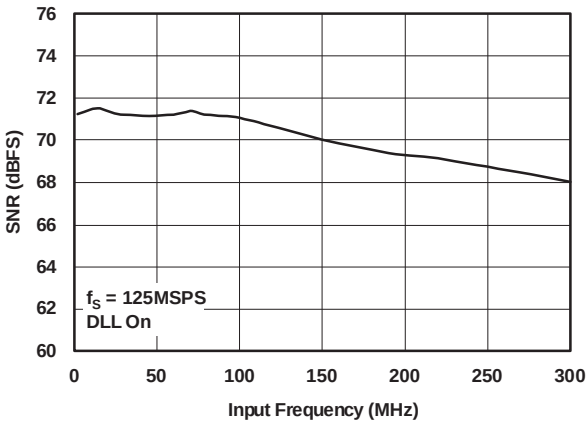
INTEGRAL NONLINEARITY (INL)



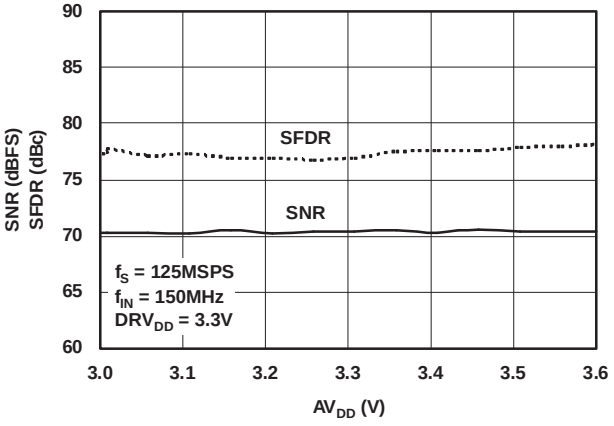
SPURIOUS−FREE DYNAMIC RANGE vs INPUT FREQUENCY



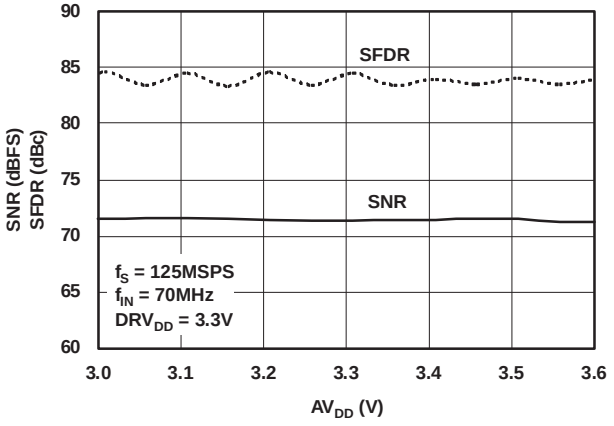
SIGNAL−TO−NOISE RATIO vs INPUT FREQUENCY



AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE



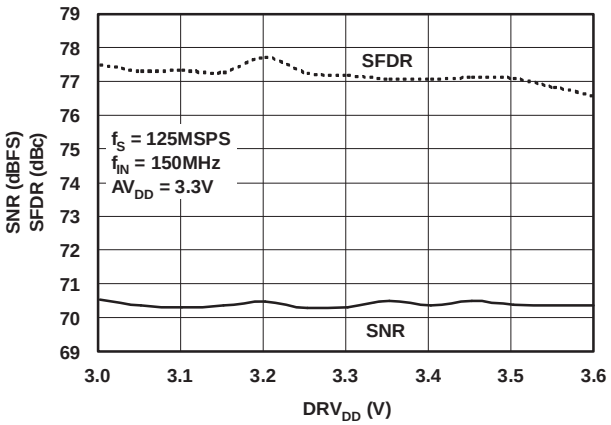
AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE



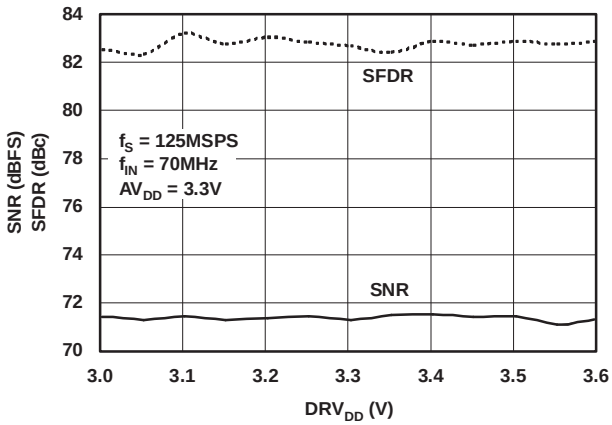
TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)

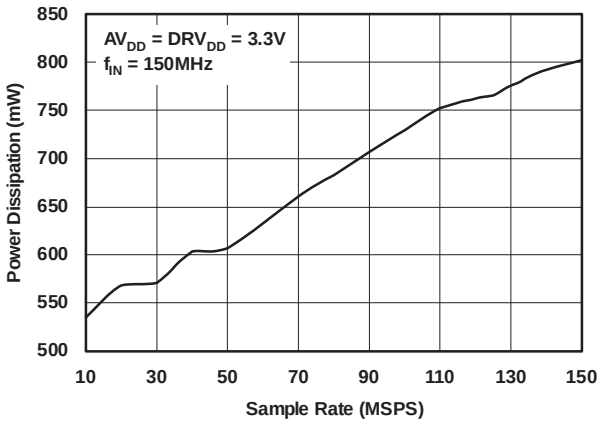
AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE



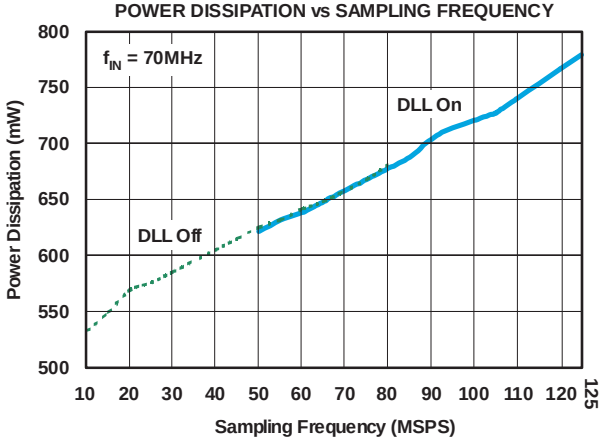
AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE



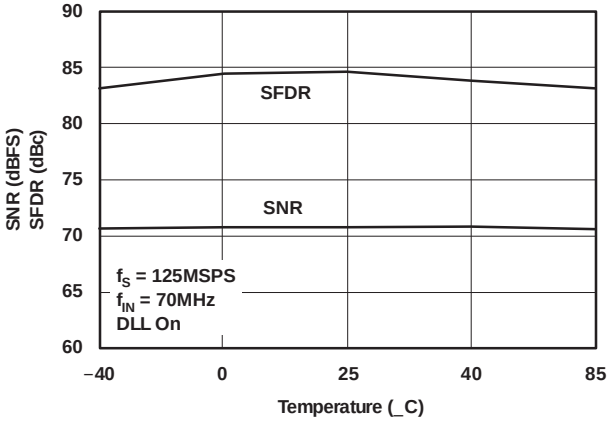
POWER DISSIPATION vs SAMPLE RATE



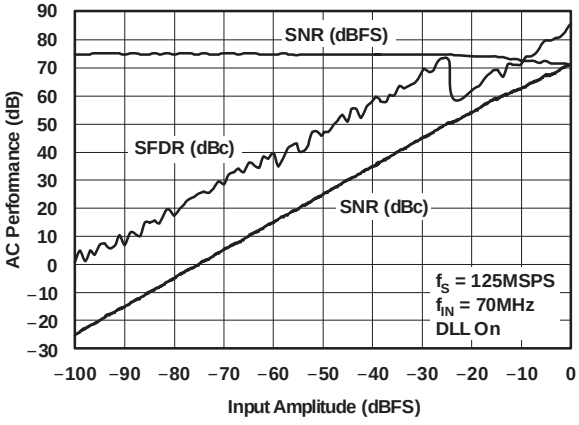
POWER DISSIPATION vs SAMPLING FREQUENCY



SIGNAL−TO−NOISE RATIO AND
SPURIOUS−FREE DYNAMIC RANGE vs TEMPERATURE

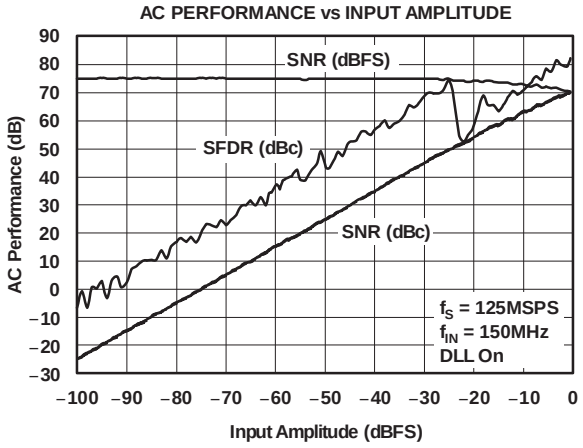


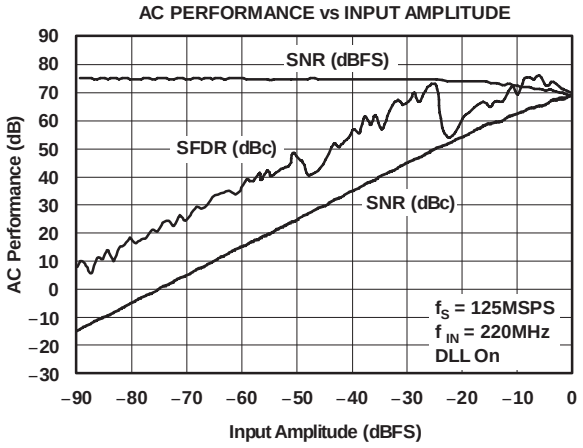
AC PERFORMANCE vs INPUT AMPLITUDE

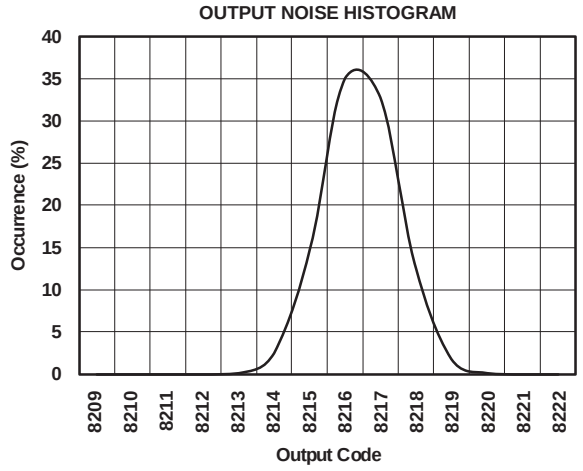


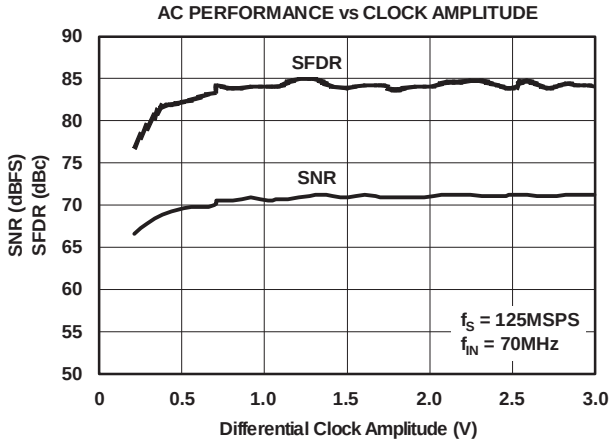
TYPICAL CHARACTERISTICS (continued)

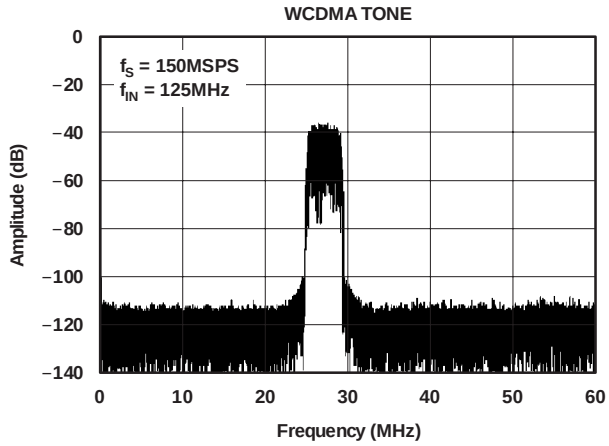
Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)







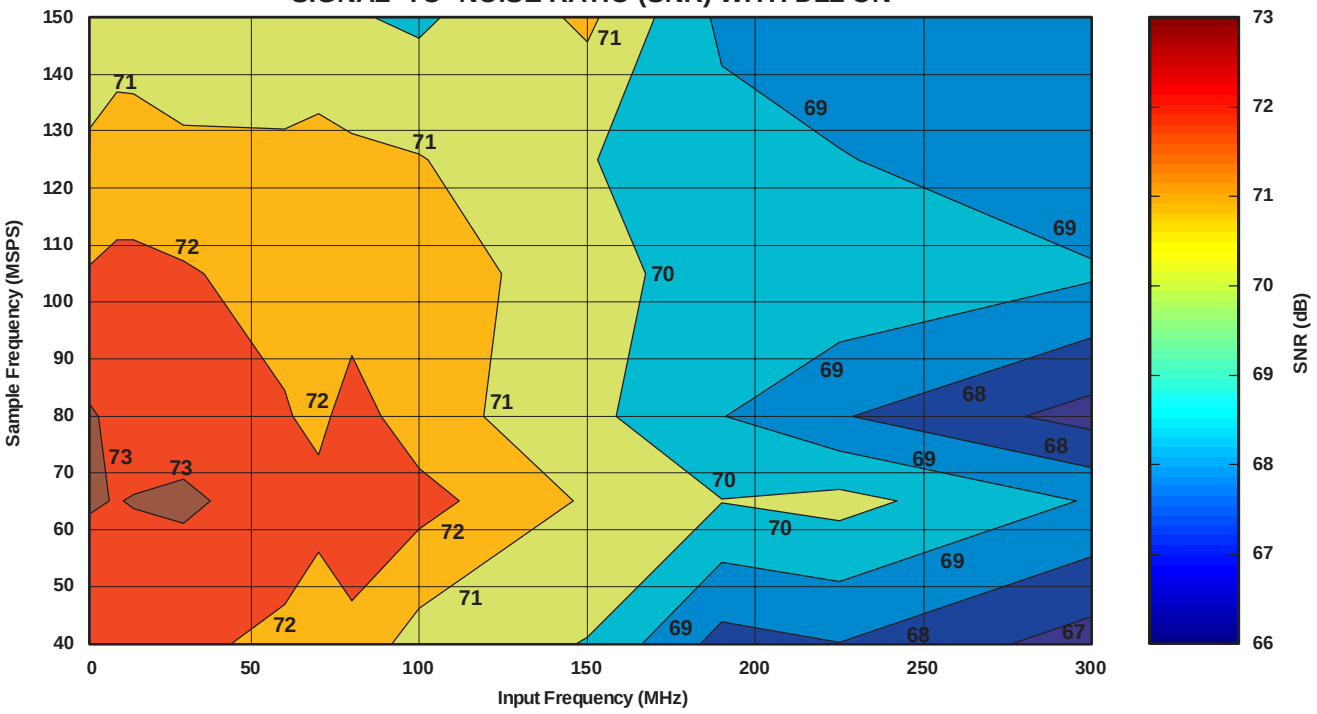




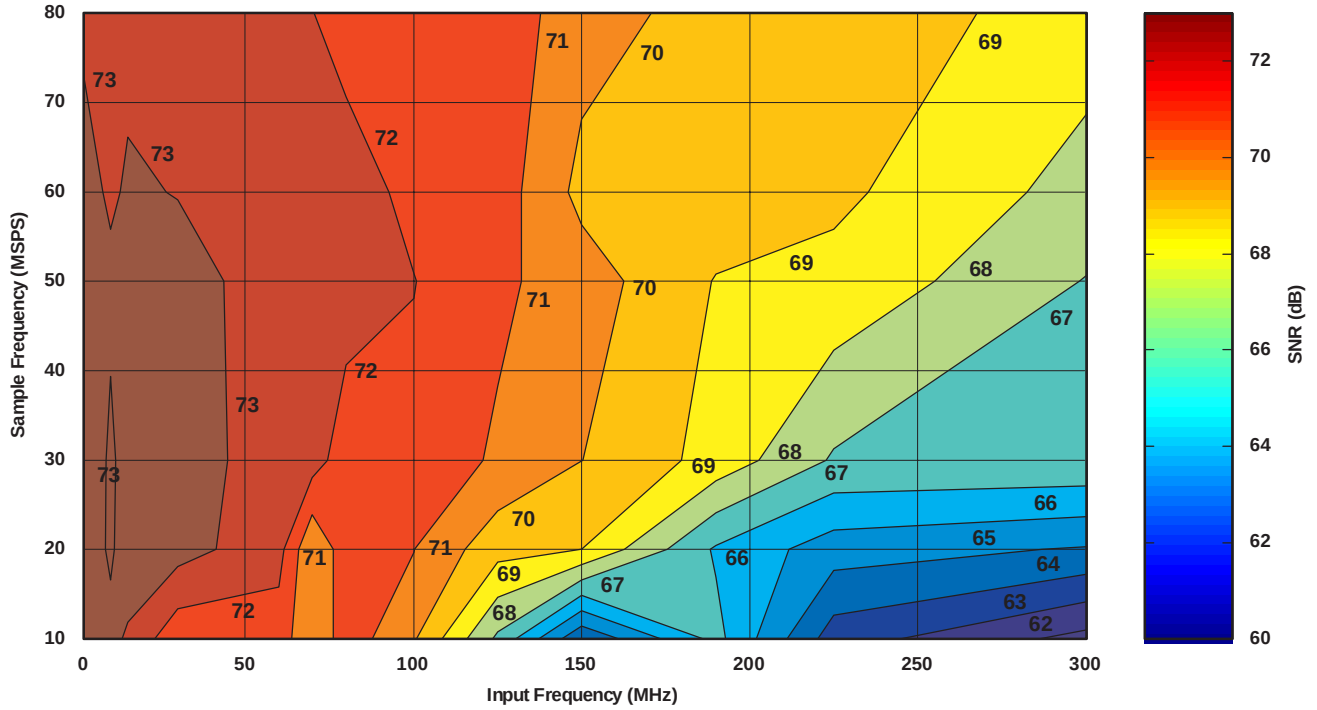
TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)

SIGNAL−TO−NOISE RATIO (SNR) WITH DLL ON



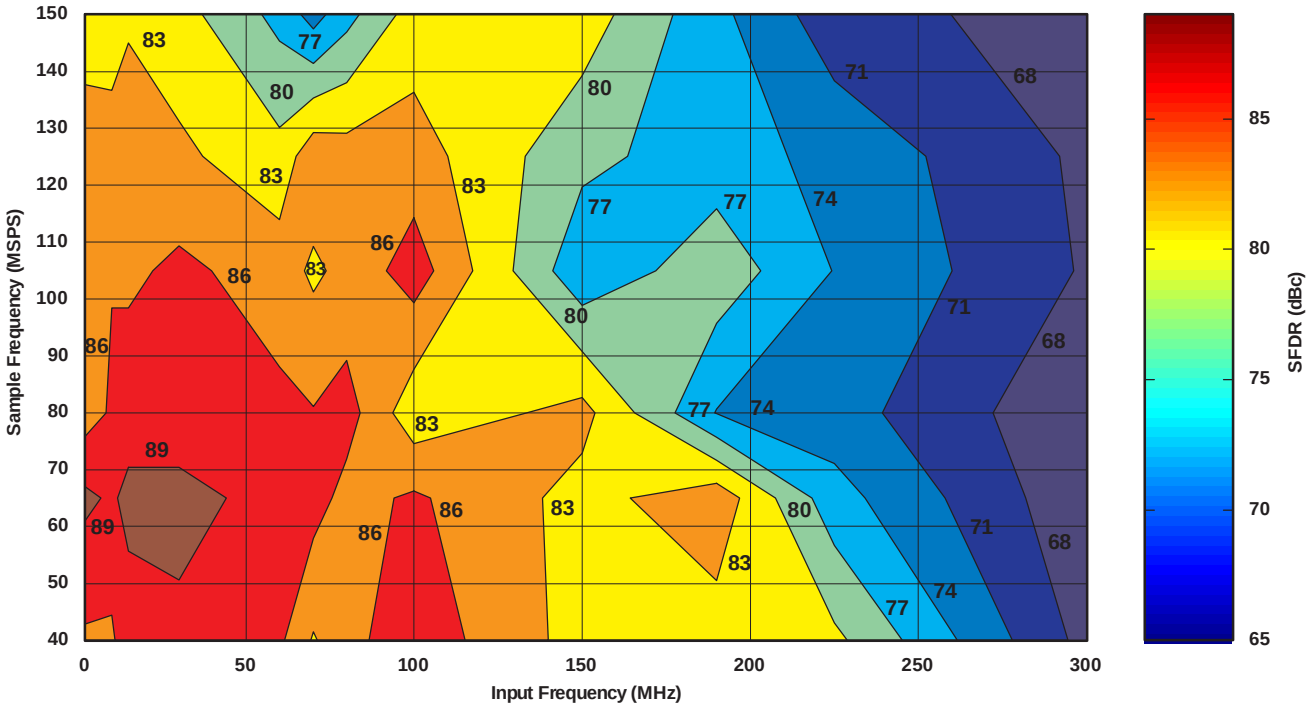
SIGNAL−TO−NOISE RATIO (SNR) WITH DLL OFF



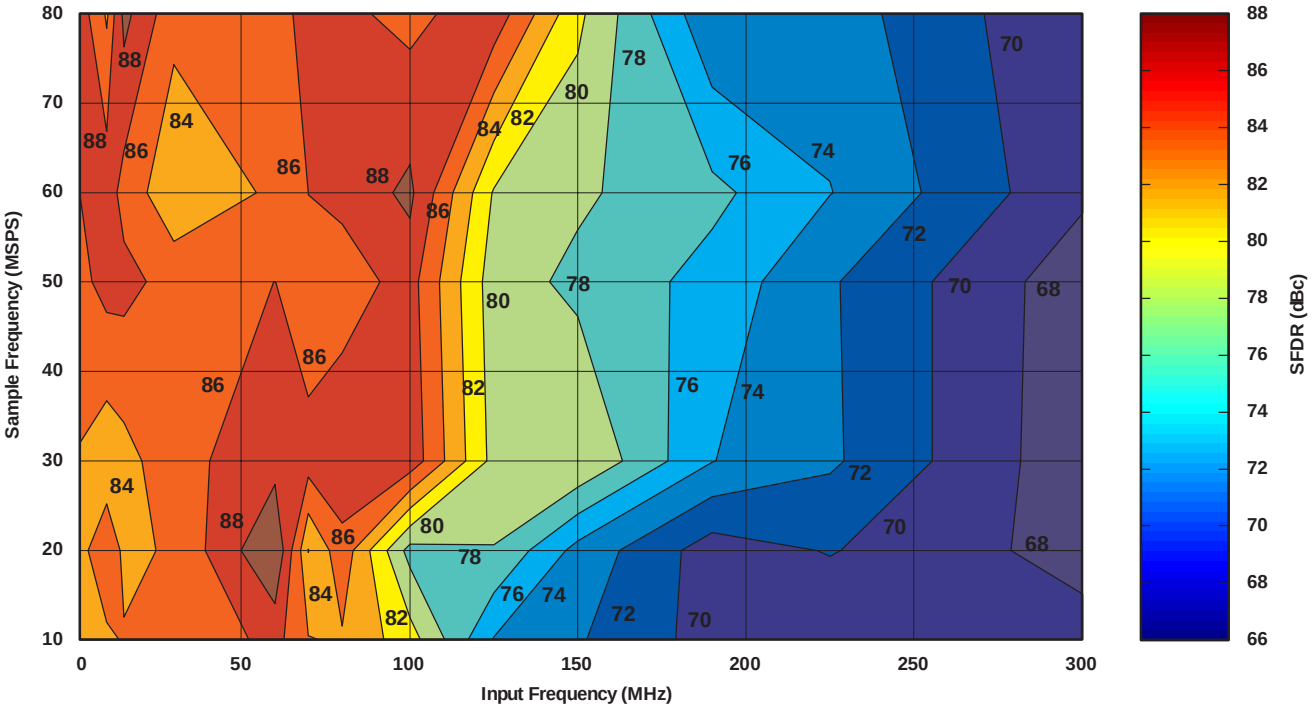
TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On(unless otherwise noted)

SPURIOUS−FREE DYNAMIC RANGE (SFDR) WITH DLL ON



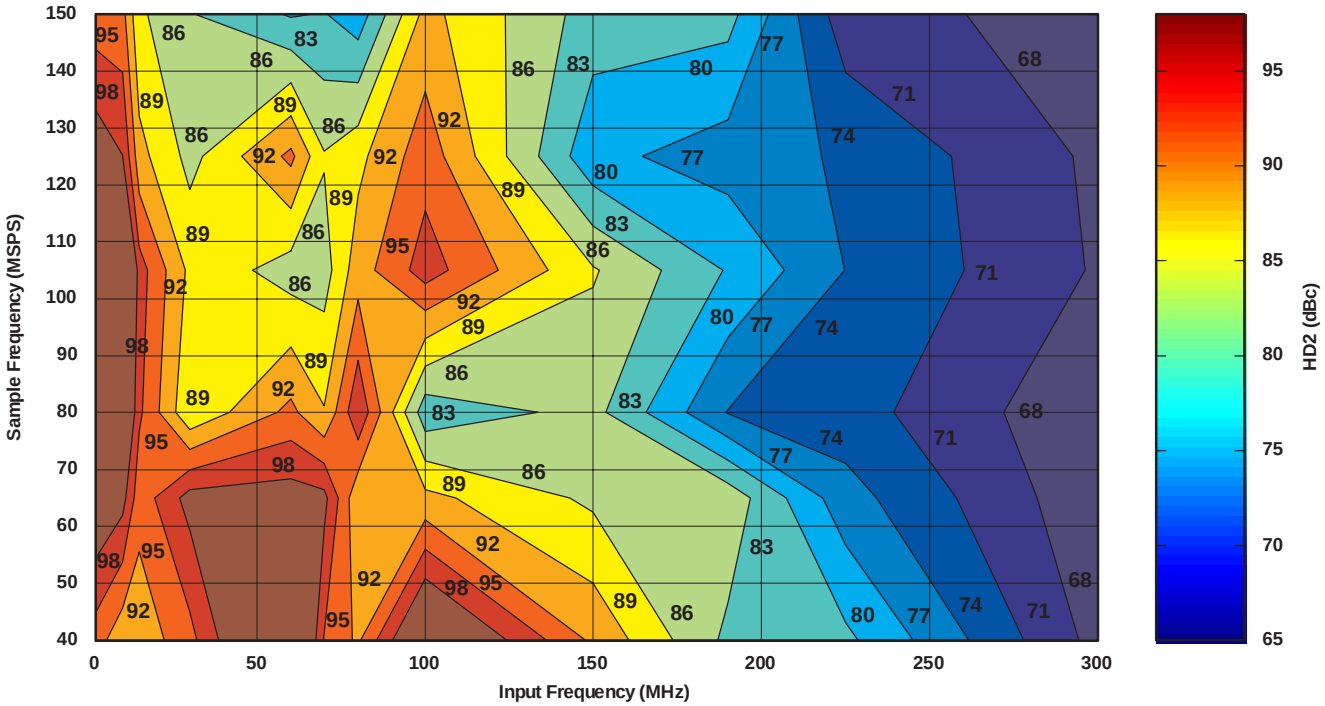
SPURIOUS−FREE DYNAMIC RANGE (SFDR) WITH DLL OFF



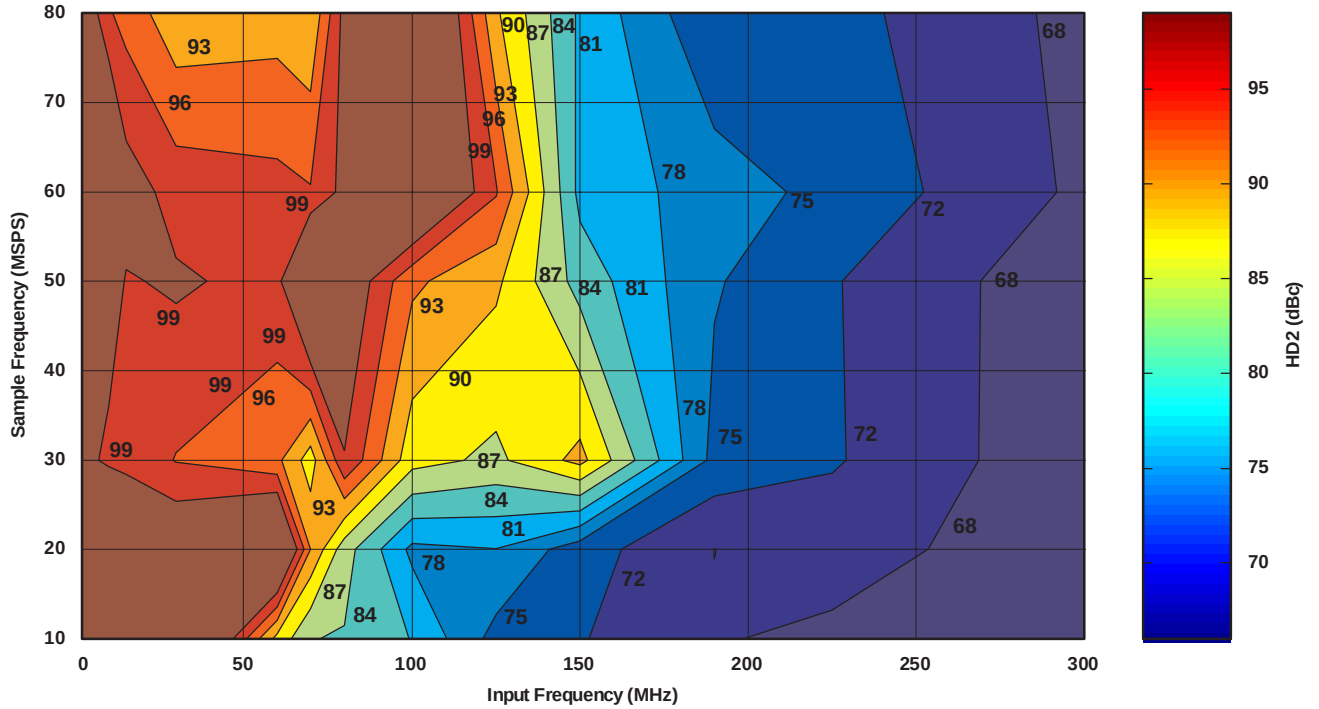
TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)

SECOND HARMONIC (HD2) WITH DLL ON



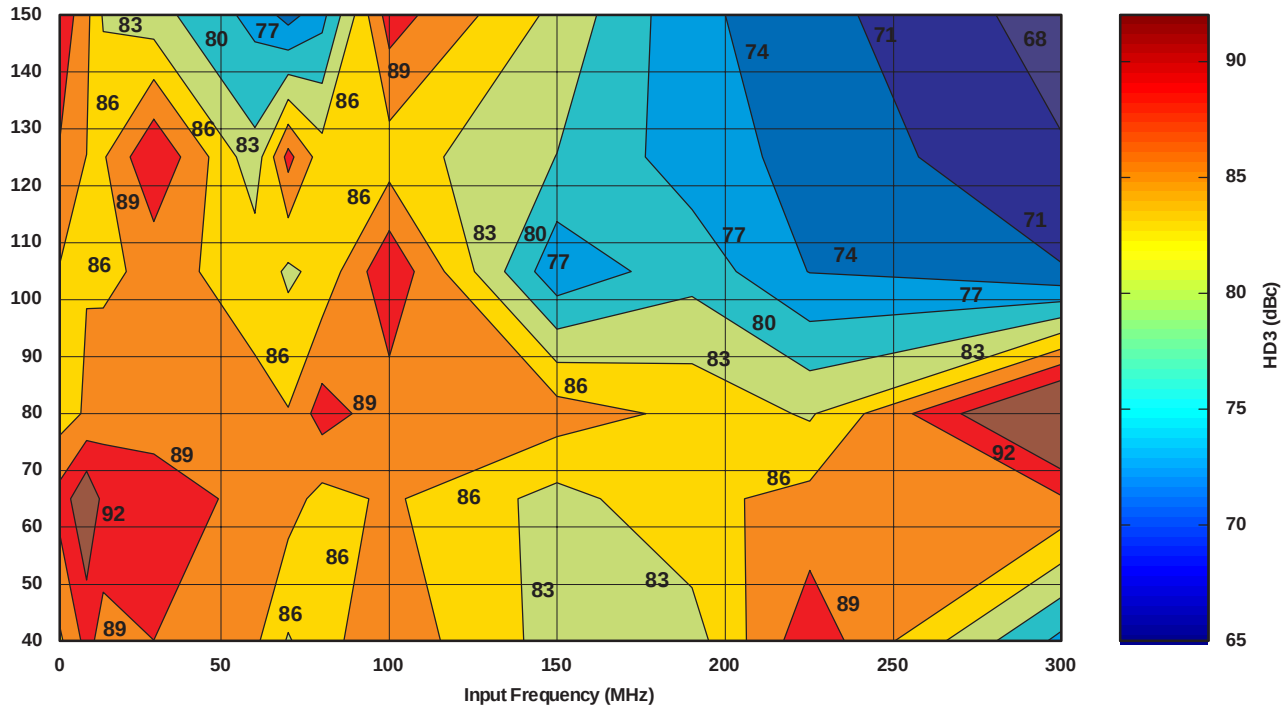
SECOND HARMONIC (HD2) WITH DLL OFF



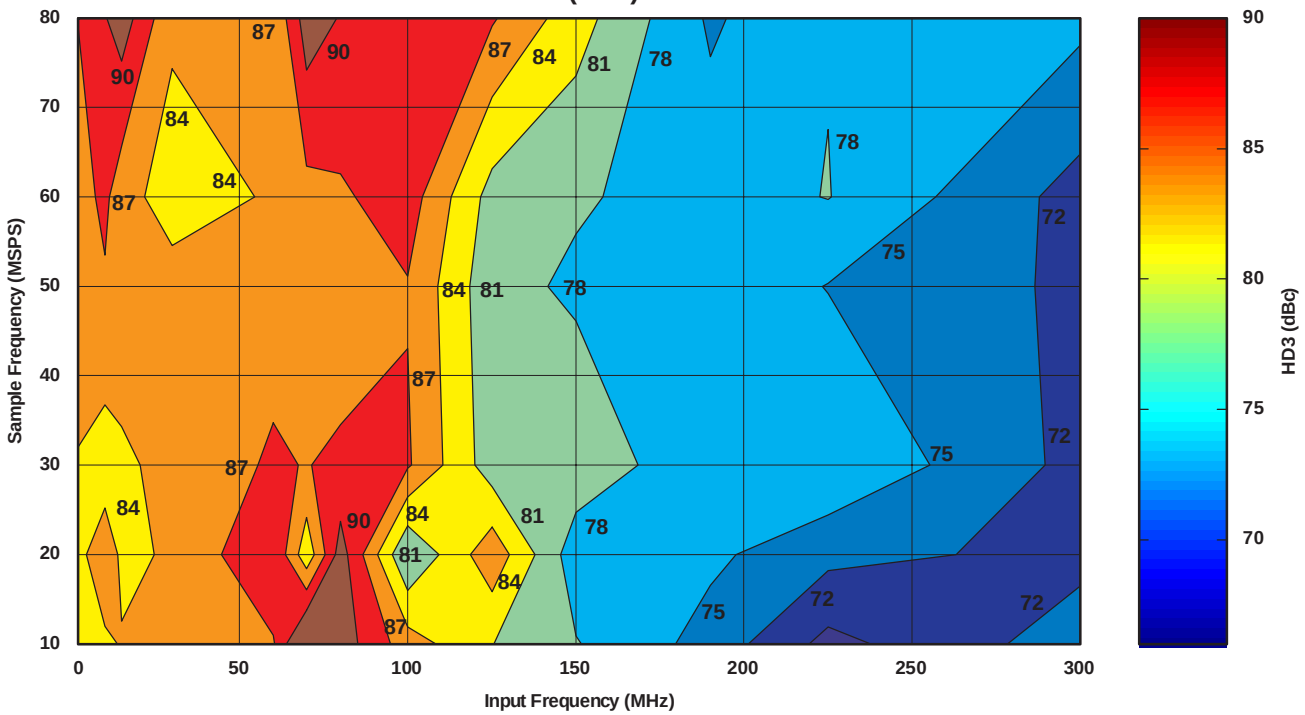
TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = −1 dBFS, sampling rate = 125 MSPS, and DLL On (unless otherwise noted)

THIRD HARMONIC (HD3) WITH DLL ON



THIRD HARMONIC (HD3) WITH DLL OFF



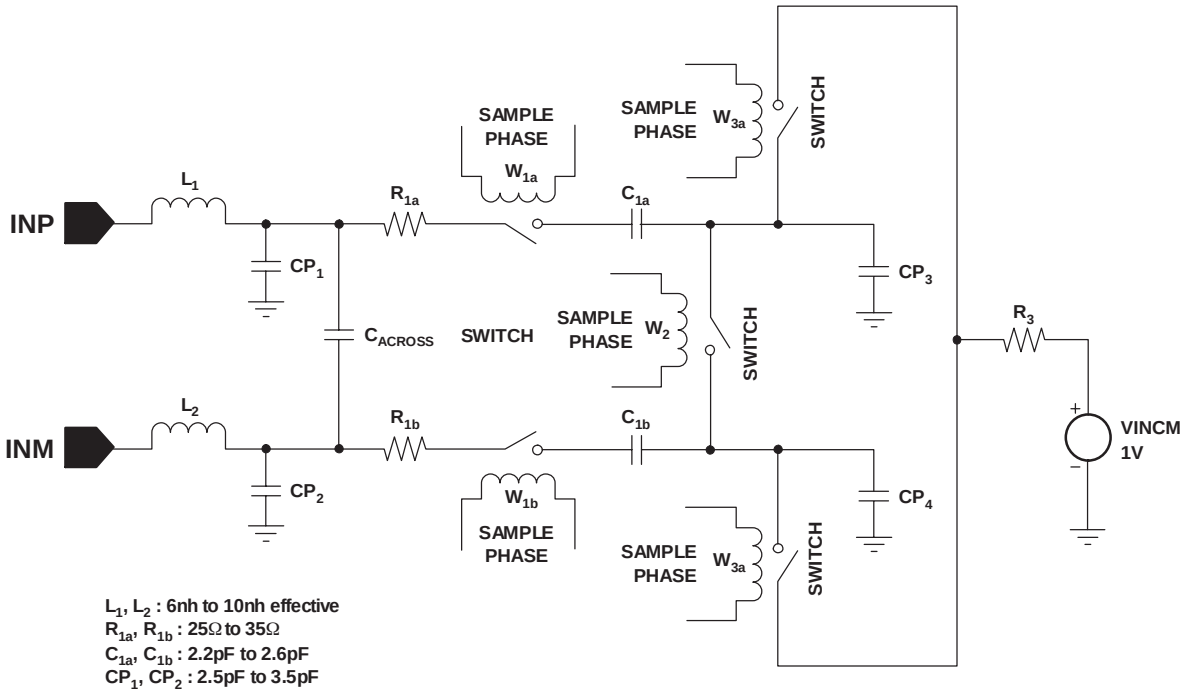
APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5500 is a low-power, 14-bit, 125−MSPS, CMOS, switched−capacitor, pipeline ADC that operates from a single 3.3-V supply. The conversion process is initiated by a falling edge of the external input clock. Once the signal is captured by the input S&H, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 16.5 clock cycles, after which the output data is available as a 14-bit parallel word, coded in either straight offset binary or binary twos−complement format.

INPUT CONFIGURATION

The analog input for the ADS5500 consists of a differential architecture implemented using a switched capacitor technique, shown in Figure 5.



L_1, L_2 : 6nh to 10nh effective
R_{1a}, R_{1b} : 25Ω to 35Ω
C_{1a}, C_{1b} : 2.2pF to 2.6pF
CP_1, CP_2 : 2.5pF to 3.5pF
CP_3, CP_4, : 1.2pF to 1.8pF
C_{ACROSS} : 0.8pF to 1.2pF
R_3 : 80Ω to 120Ω
Switches: W_{1a}, W_{1b} : On Resistance: 25Ω to 35Ω
W_2 : On Resistance: 7.5Ω to 15Ω
W_{3a}, W_{3b} : On Resistance: 40Ω to 60Ω
W_{1a}, W_{1b}, W_2, W_{3a}, W_{3b} : Off Resistance: 1e10

All switches are on in sample phase.
Approximately half of every clock period is a sample phase.

Figure 5. Analog Input Stage

This differential input topology produces a high level of ac performance for high sampling rates. It also results in a high usable input bandwidth, especially important for high intermediate frequency (IF) or undersampling applications. The ADS5500 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pin 17). For a full-scale differential input, each of the differential lines of the input signal (pins 19 and 20) swings symmetrically between CM + 0.575 V and CM – 0.575 V. This means that each input is driven with a signal of up to CM ± 0.575 V, so that each input has a maximum differential signal of 1.15 V_{PP} for a total differential input signal swing of 2.3 V_{PP}. The maximum swing is determined by the two reference voltages − the top reference (REFP, pin 29), and the bottom reference (REFM, pin 30).

The ADS5500 obtains optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 6 shows one possible configuration using an RF transformer.

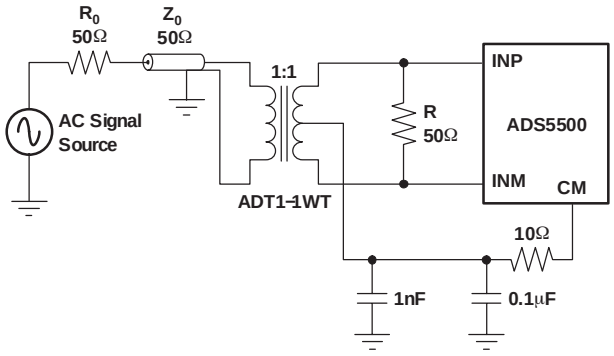


Figure 6. Transformer Input to Convert Single-Ended Signal to Differential Signal

The single-ended signal is fed to the primary winding of an RF transformer. Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5500 is connected to the center tap of the secondary winding. To ensure a steady low-noise V_{CM} reference, best performance is obtained when the CM (pin 17) output is filtered to ground with 0.1−μF and 0.01-μF low-inductance capacitors.

Output V_{CM} (pin 17) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of 4 mA (2 mA per input). Equation 1 describes the dependency of the common-mode current and the sampling frequency:

$$\frac{4\text{mA} \times f_s}{125\text{MSPS}} \quad (1)$$

Where: f_S > 60 MSPS.

This equation designs the output capability and impedance of the driving circuit accordingly.

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer or to use a differential input/output amplifier without a transformer to drive the input of the ADS5500. Texas Instruments offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, OPA847, and OPA695) that can be selected, depending on the application. An RF gain block amplifier, such as the TI THS9001, can also be used with an RF transformer for very high input frequency applications. The THS4503 is a recommended differential input/output amplifier. Table 4 lists the recommended amplifiers.

When using single-ended operational amplifiers (such as the THS3201, THS3202, OPA847, or OPA695) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5500. These three amplifier circuits minimize even-order harmonics. For high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5500 directly (see Figure 6) or with the addition of the filter circuit (see Figure 7).

Figure 7 shows how R_{IN} and C_{IN} can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. It is recommended that these components be included in the ADS5500 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine tuning of the circuit performance. Any mismatch between the differential lines of the ADS5500 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring dc coupling of the input. Flexible in their configurations (see Figure 8), such amplifiers can be used for single-ended-to-differential conversion signal amplification.

Table 4. Recommended Amplifiers to Drive Input of ADS5500

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER?
DC to 20 MHz	THS4503 (1)	Differential in/out amplifier	No
DC to 50 MHz	OPA847 (1)	Operational amplifier	Yes
10 MHz to 120 MHz	OPA695 (1)	Operational amplifier	Yes
	THS3201 (1)	Operational amplifier	Yes
	THS3202 (1)	Operational amplifier	Yes
Over 100 MHz	THS9001 (1)	RF gain block	Yes

(1) Potential EP devices

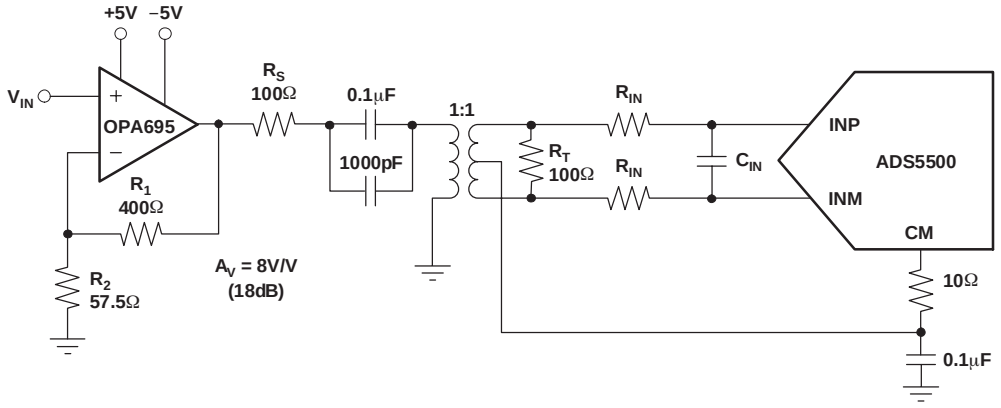


Figure 7. Converting Single-Ended Input Signal to Differential Signal Using an RF Transformer

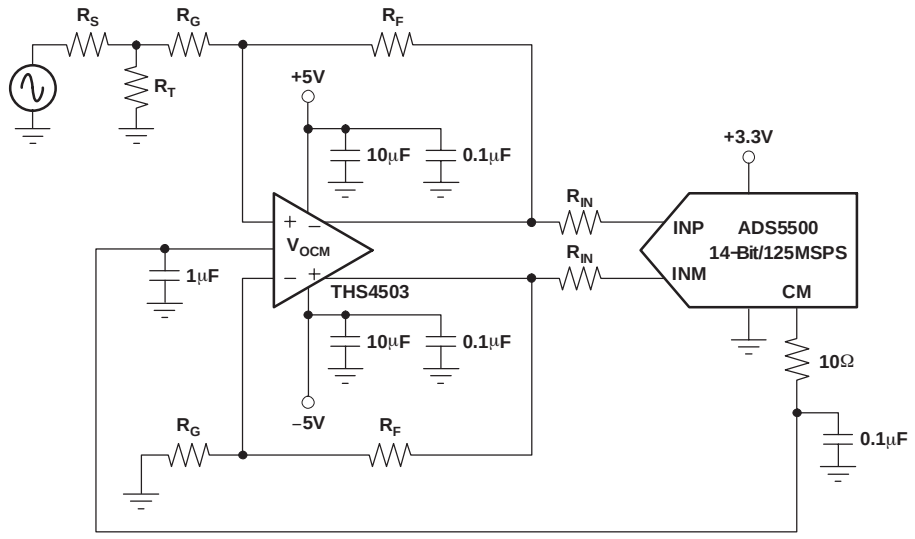


Figure 8. Using THS4503 With ADS5500

POWER−SUPPLY SEQUENCE

The ADS5500 requires a power-up sequence where the DRV_{DD} supply must be at least 0.4 V by the time the AV_{DD} supply reaches 3 V. Powering up both supplies at the same time works without any problem. If this sequence is not followed, the device may stay in power-down mode.

POWER DOWN

The device enters power down in one of two ways − either by reducing the clock speed to between dc and 1 MHz, or by setting a bit through the serial programming interface. Using the reduced clock speed, the power down may be initiated for clock frequencies below 10 MHz. For clock frequencies between 1 MHz and 10 MHz, this can vary from device to device, but will power down for clock speeds below 1 MHz.

The device can be powered down by programming the internal register (see *Serial Programming Interface* section). The outputs become 3-stated and only the internal reference is powered up to shorten the power-up time. The power-down mode reduces power dissipation to a minimum of 180 mW.

REFERENCE CIRCUIT

The ADS5500 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a 1−µF decoupling capacitor in series with a 1-Ω resistor (see Figure 9). In addition, an external 56.2-kΩ resistor should be connected from IREF (pin 31) to AGND to set the proper current for the operation of the ADC (see Figure 9). No capacitor should be connected between pin 31 and ground; only the 56.2-kΩ resistor should be used.

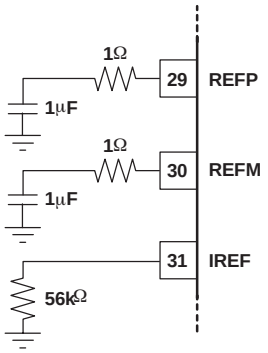


Figure 9. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5500 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM (pin 17) using internal 5-kΩ resistors that connect CLKP (pin 10) and CLKM (pin 11) to CM (pin 17) (see Figure 10).

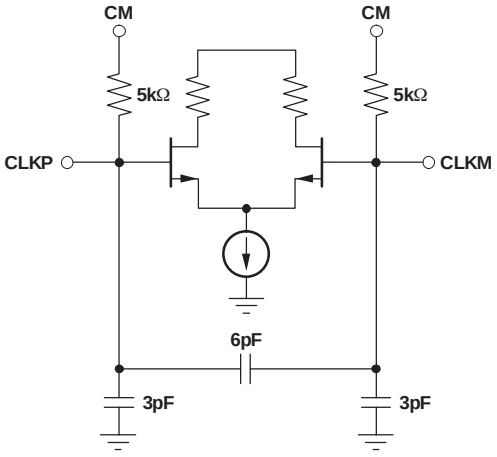


Figure 10. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM (pin 11) to ground with a 0.01-µF capacitor, while CLKP is ac coupled with a 0.01-µF capacitor to the clock source (see Figure 11).

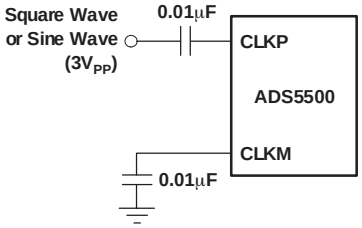


Figure 11. AC-Coupled Single-Ended Clock Input

The ADS5500 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01-µF capacitors (see Figure 12).

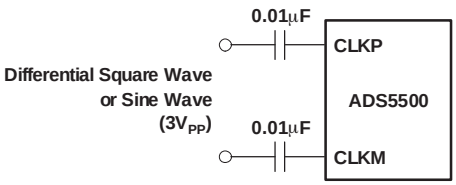


Figure 12. AC-Coupled Differential Clock Input

For high input frequency sampling, it is recommended to use a clock source with very low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 13 shows the performance variation of the ADC versus clock duty cycle.

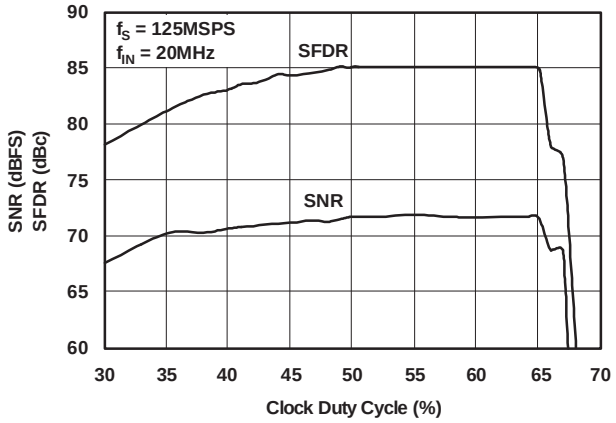


Figure 13. AC Performance vs Clock Duty Cycle

Bandpass filtering of the source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter further improves as the amplitude is increased. In that sense, using a differential clock allows for the use of larger amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 14 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, see the *ADS5500EVM user's guide* (SLWU010), available for download from www.ti.com.

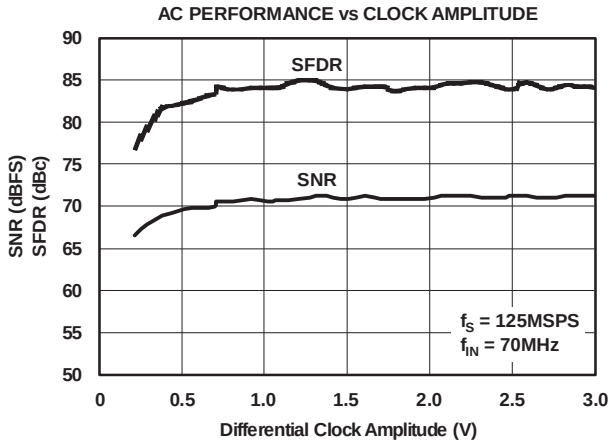


Figure 14. AC Performance vs Clock Amplitude

INTERNAL DLL

In order to obtain the fastest sampling rates achievable with the ADS5500, the device uses an internal digital phase lock loop (DLL). Nevertheless, the limited frequency range of operation of DLL degrades the performance at clock frequencies below 60 MSPS. In order to operate the device below 60 MSPS, the internal DLL must be shut off using the DLL OFF mode described in the *Serial Interface Programming* section. The *Typical Performance Curves* show the performance obtained in both modes of operation − DLL ON (default) and DLL OFF. In either of the two modes, the device enters power-down mode if no clock or a slow clock is provided. The limit of the clock frequency where the device functions properly is ensured to be over 10 MHz.

OUTPUT INFORMATION

The ADC provides 14 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (CLKOUT, pin 43), and an out-of-range indicator (OVR, pin 64) that equals 1 when the output reaches the full-scale limits.

Two different output formats (straight offset binary or twos complement) and two different output clock polarities (latching output data on rising or falling edge of the output clock) can be selected by setting DFS (pin 40) to one of four different voltages. Table 3 details the four modes. In addition, output enable control (OE, pin 41, active high) is provided to 3-state the outputs.

The output circuitry of the ADS5500 has being designed to minimize the noise produced by the transients of the data switching, and in particular its coupling to the ADC analog circuitry. Output D4 (pin 51) senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 2, as long as all outputs (including CLKOUT) have a similar load as the one at D4 (pin 51). This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. External series resistors with the output are not necessary.

SERIAL PROGRAMMING INTERFACE

The ADS5500 has internal registers for the programming of some of the modes described in the previous sections. The registers should be reset after power up by applying a 2−µs (minimum) high pulse on RESET (pin 35); this also resets the entire ADC and sets the data outputs to low. This pin has a 200-kΩ internal pullup resistor to AV_{DD}. The programming is done through a three-wire interface. The timing diagram and serial register setting in the *Serial Programing Interface* section describe the programming of this register.

Table 2 shows the different modes and the bit values to be written on the register to enable them.

Note that some of these modes may modify the standard operation of the device and possibly vary the performance, with respect to the typical data shown in this data sheet.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS5500MPAPEP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5500MEP	Samples
ADS5500MPAPREP	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5500MEP	Samples
V62/05613-01XE	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5500MEP	Samples
V62/05613-02XE	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS5500MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADS5500-EP :

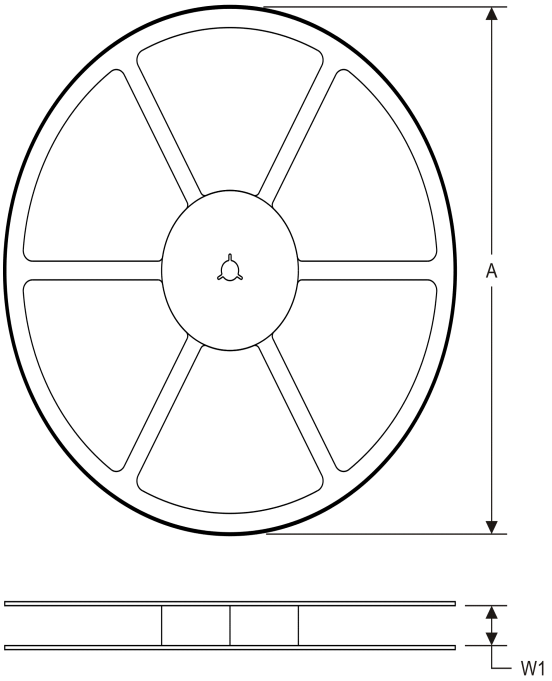
- Catalog: ADS5500

NOTE: Qualified Version Definitions:

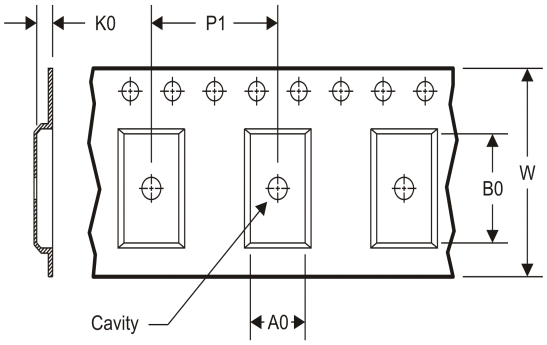
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



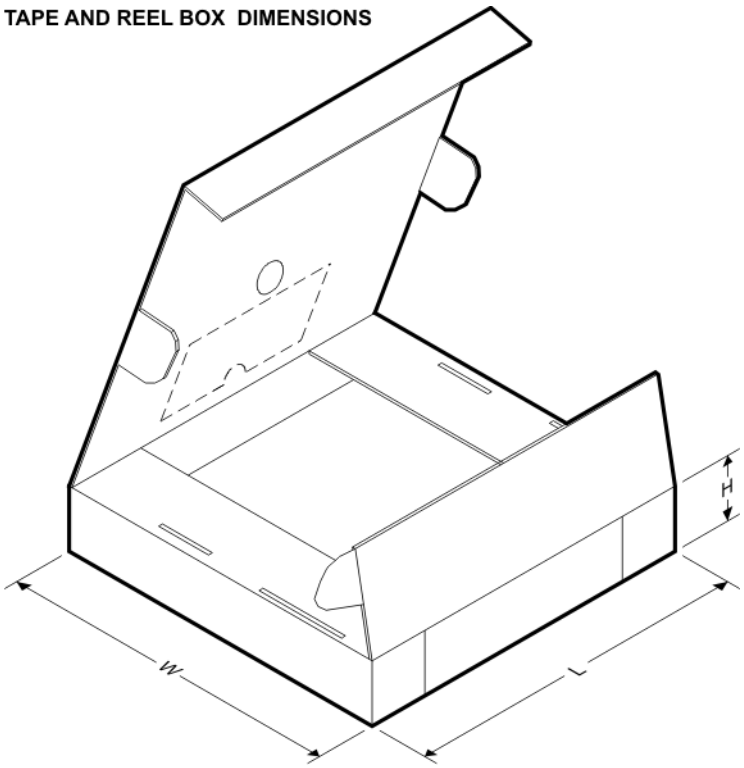
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5500MPAPREP	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

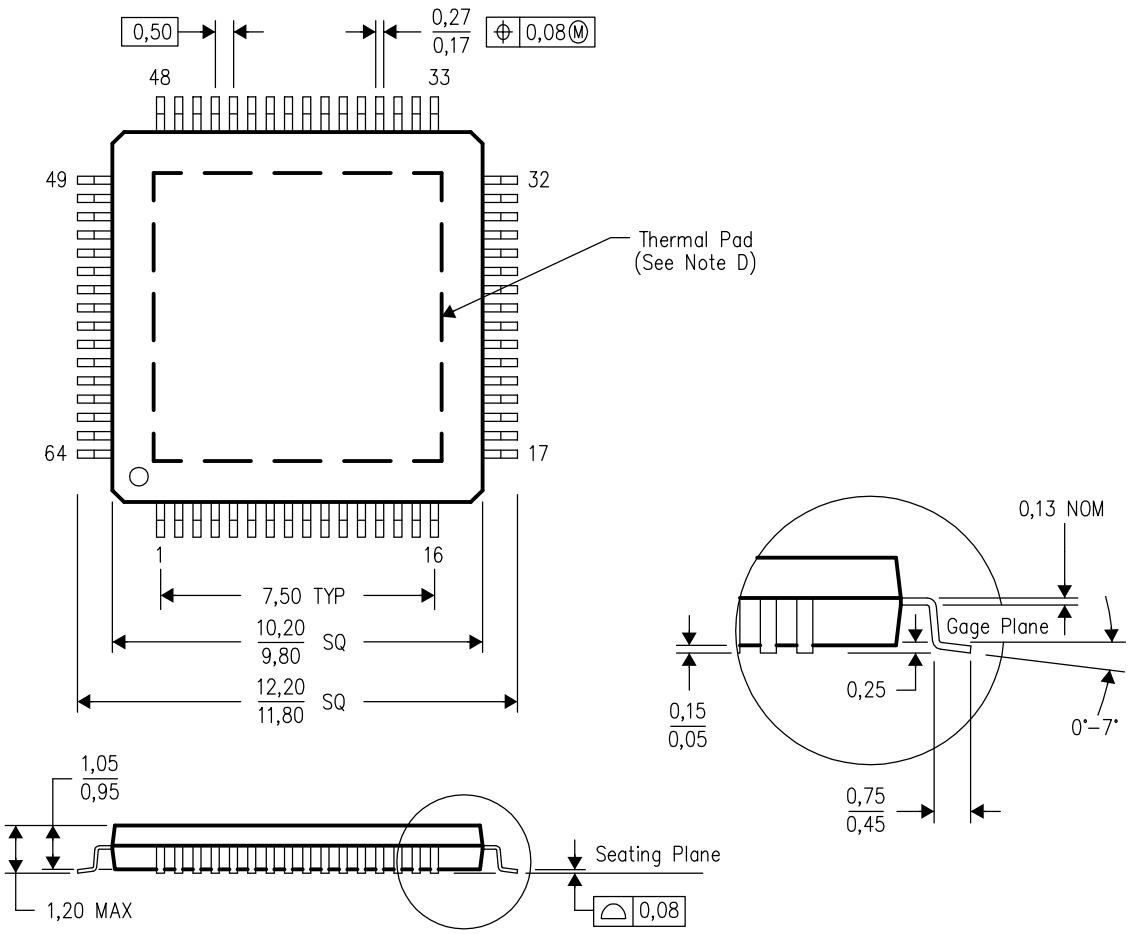
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5500MPAPREP	HTQFP	PAP	64	1000	367.0	367.0	45.0

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

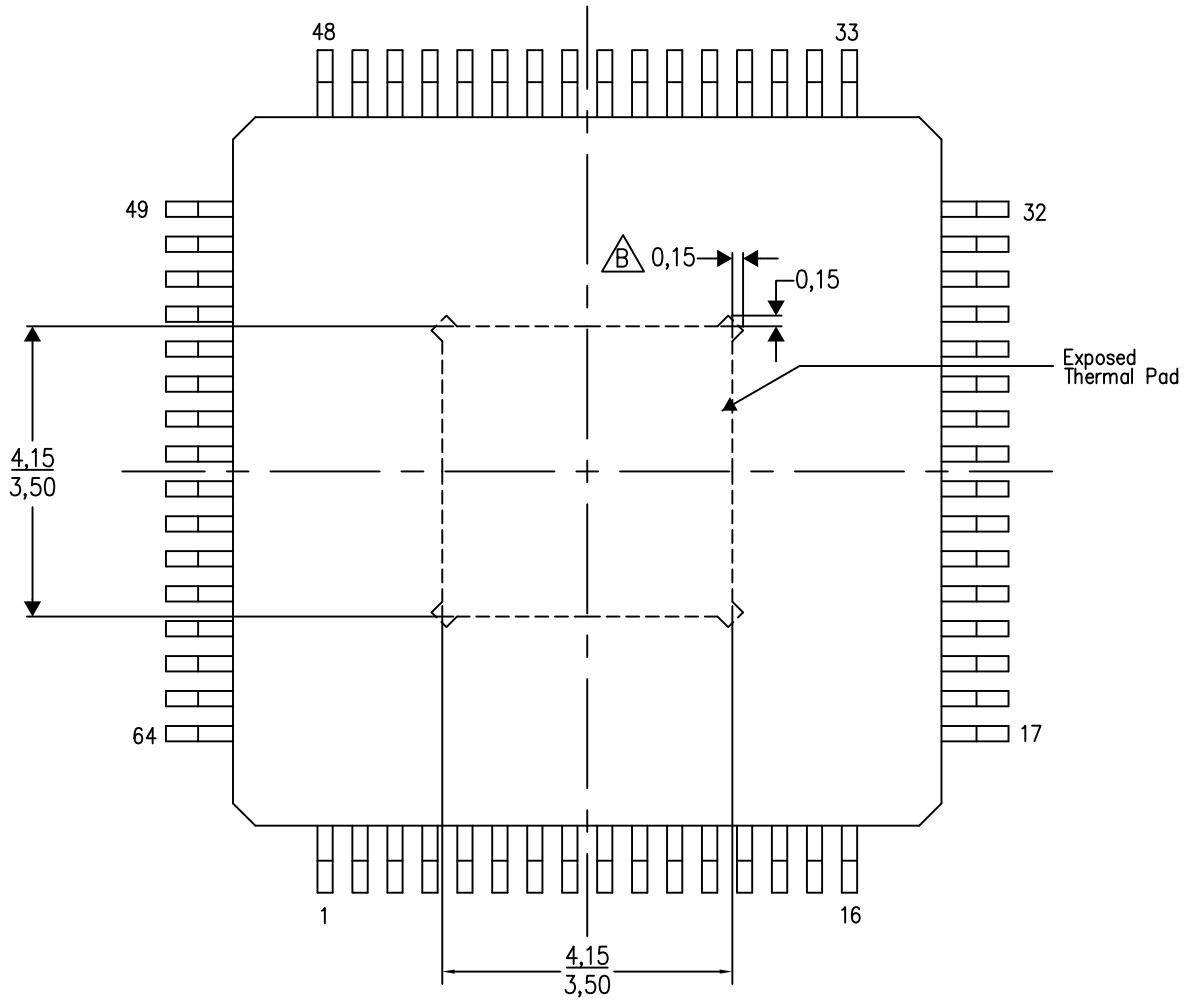
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–2/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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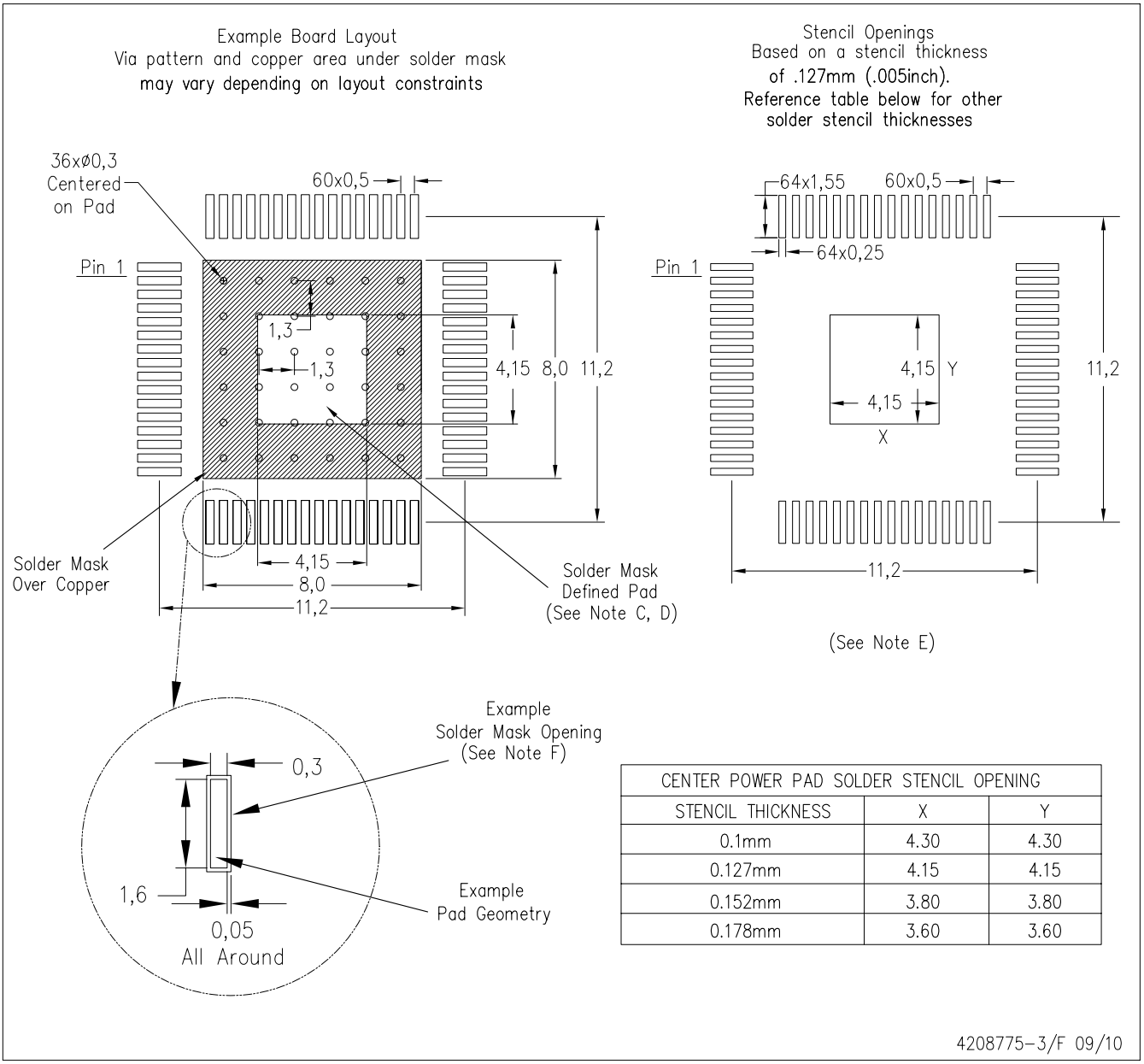
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	4.30	4.30
0.127mm	4.15	4.15
0.152mm	3.80	3.80
0.178mm	3.60	3.60

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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