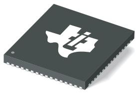

Dual-Channel, 14-Bit, 250-MSPS Ultralow-Power ADC

Check for Samples: ADS4249

FEATURES

- **Maximum Sample Rate: 250 MSPS**
- **Ultralow Power with Single 1.8-V Supply:**
  - **560-mW Total Power at 250 MSPS**
- **High Dynamic Performance:**
  - **80-dBc SFDR at 170 MHz**
  - **71.7-dBFS SNR at 170 MHz**
- **Crosstalk: > 90 dB at 185 MHz**
- **Programmable Gain Up to 6 dB for SNR/SFDR Trade-off**
- **DC Offset Correction**
- **Output Interface Options:**
  - **1.8-V Parallel CMOS Interface**
  - **Double Data Rate (DDR) LVDS with Programmable Swing:**
    - **Standard Swing: 350 mV**
    - **Low Swing: 200 mV**
- **Supports Low Input Clock Amplitude Down to 200 mV_{PP}**
- **Package: 9-mm × 9-mm, 64-Pin Quad Flat No-Lead (QFN) Package**

APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**

DESCRIPTION

The ADS4249 is a member of the ADS42xx ultralow-power family of dual-channel, 12-bit/14-bit analog-to-digital converters (ADCs). Innovative design techniques are used to achieve high dynamic performance, while consuming extremely low power with a 1.8-V supply. This topology makes the ADS4249 well-suited for multi-carrier, wide-bandwidth communications applications.

The ADS4249 has gain options that can be used to improve SFDR performance at lower full-scale input ranges. This device also includes a dc offset correction loop that can be used to cancel the ADC offset. Both DDR LVDS and parallel CMOS digital output interfaces are available in a compact QFN-64 PowerPAD™ package.

The device includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The ADS4249 is specified over the industrial temperature range (–40°C to +85°C).

ADS424x/2x Family Comparison (1)

	65 MSPS	125 MSPS	160 MSPS	250 MSPS
ADS422x 12-bit family	ADS4222	ADS4225	ADS4226	ADS4229
ADS424x 14-bit family	ADS4242	ADS4245	ADS4246	ADS4249

(1) See Table 1 for details on migrating from the ADS62P49 family.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS4249	QFN-64	RGC	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ4249	ADS4249IRGCT	Tape and reel
							ADS4249IRGCR	Tape and reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.

The ADS4249 is pin-compatible with the previous generation ADS62P49 data converter; this similar architecture enables easy migration. However, there are some important differences between the two device generations, summarized in Table 1.

Table 1. Migrating from the ADS62P49

ADS62P49	ADS4249
PINS	
Pin 22 is NC (not connected)	Pin 22 is AVDD
Pins 38 and 58 are DRVDD	Pins 38 and 58 are NC (do not connect, must be floated)
Pins 39 and 59 are DRGND	Pins 39 and 59 are NC (do not connect, must be floated)
SUPPLY	
AVDD is 3.3 V	AVDD is 1.8 V
DRVDD is 1.8 V	No change
INPUT COMMON-MODE VOLTAGE	
VCM is 1.5 V	VCM is 0.95 V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol New serial register map
EXTERNAL REFERENCE	
Supported	Not supported

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ABSOLUTE MAXIMUM RATINGS(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		–2.4	2.4	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		–2.4	2.4	V
Voltage applied to input pins	INP_A, INM_A, INP_B, INM_B	–0.3	Minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM(2)	–0.3	AVDD + 0.3	V
	RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	–0.3	3.9	V
Operating free-air temperature range, T_A		–40	+85	°C
Operating junction temperature range, T_J			+125	°C
Storage temperature range, T_{stg}		–65	+150	°C
ESD rating	Human body model (HBM)		2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS4249	UNITS
		RGC	
		64 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	23.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	10.9	
θ_{JB}	Junction-to-board thermal resistance	4.3	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	4.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		ADS4249			UNIT
		MIN	NOM	MAX	
SUPPLIES					
Analog supply voltage, AVDD		1.7	1.8	1.9	V
Digital supply voltage, DRVDD		1.7	1.8	1.9	V
ANALOG INPUTS					
Differential input voltage range			2		V_{PP}
Input common-mode voltage			VCM ± 0.05		V
Maximum analog input frequency with 2-V_{PP} input amplitude(1)			400		MHz
Maximum analog input frequency with 1-V_{PP} input amplitude(1)			600		MHz
CLOCK INPUT					
Input clock sample rate					
Low-speed mode enabled(2)		1		80	MSPS
Low-speed mode disabled(2) (by default after reset)		80		250	MSPS
Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.2	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
	LVCMOS, single-ended, ac-coupled		1.5		V
Input clock duty cycle					
Low-speed mode disabled		35	50	65	%
Low-speed mode enabled		40	50	60	%
DIGITAL OUTPUTS					
Maximum external load capacitance from each output pin to DRGND, C_{LOAD}			5		pF
Differential load resistance between the LVDS output pairs (LVDS mode), R_{LOAD}			100		Ω
Operating free-air temperature, T_A		–40		+85	°C

(1) See the *Theory of Operation* section in the Application Information.
(2) See the *Serial Interface Configuration* section for details on programming the low-speed mode.

HIGH-PERFORMANCE MODES(1)(2)

PARAMETER	DESCRIPTION
High-performance mode	Set the HIGH PERF MODE[2:1] register bit to obtain best performance across sample clock and input signal frequencies. Register address = 03h, data = 03h
High-frequency mode	Set the HIGH FREQ MODE CH A and HIGH FREQ MODE CH B register bits for high input signal frequencies greater than 200 MHz. Register address = 4Ah, data = 01h Register address = 58h, data = 01h
High-speed mode	Set the HIGH PERF MODE[8:3] bits to obtain best performance across input signal frequencies for sampling rates greater than 160 MSPS. Note that this mode changes VCM to 0.87 V from its default value of 0.95 V. Register address = 2h, data = 40h Register address = D5h, data = 18h Register address = D7h, data = 0Ch Register address = DBh, data = 20h

(1) It is recommended to use these modes to obtain best performance.
(2) See the *Serial Interface Configuration* section for details on register programming.

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ELECTRICAL CHARACTERISTICS: ADS4249

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	ADS4249 (250 MSPS) MIN	TYP	MAX	UNIT
Resolution					14	Bits
Signal-to-noise ratio	SNR	f_{IN} = 20 MHz		72.8		dBFS
		f_{IN} = 70 MHz		72.5		dBFS
		f_{IN} = 100 MHz		72.2		dBFS
		f_{IN} = 170 MHz	67.5	71.7		dBFS
		f_{IN} = 300 MHz		69.4		dBFS
Signal-to-noise and distortion ratio	SINAD	f_{IN} = 20 MHz		72		dBFS
		f_{IN} = 70 MHz		71.6		dBFS
		f_{IN} = 100 MHz		71.6		dBFS
		f_{IN} = 170 MHz	66.5	70.7		dBFS
		f_{IN} = 300 MHz		68.7		dBFS
Spurious-free dynamic range	SFDR	f_{IN} = 20 MHz		80		dBc
		f_{IN} = 70 MHz		79		dBc
		f_{IN} = 100 MHz		82		dBc
		f_{IN} = 170 MHz	71	80		dBc
		f_{IN} = 300 MHz		76		dBc
Total harmonic distortion	THD	f_{IN} = 20 MHz		78		dBc
		f_{IN} = 70 MHz		77		dBc
		f_{IN} = 100 MHz		79		dBc
		f_{IN} = 170 MHz	69	76		dBc
		f_{IN} = 300 MHz		75		dBc
Second-harmonic distortion	HD2	f_{IN} = 20 MHz		80		dBc
		f_{IN} = 70 MHz		79		dBc
		f_{IN} = 100 MHz		81		dBc
		f_{IN} = 170 MHz	71	80		dBc
		f_{IN} = 300 MHz		76		dBc
Third-harmonic distortion	HD3	f_{IN} = 20 MHz		85		dBc
		f_{IN} = 70 MHz		87		dBc
		f_{IN} = 100 MHz		96		dBc
		f_{IN} = 170 MHz	71	80		dBc
		f_{IN} = 300 MHz		84		dBc
Worst spur (other than second and third harmonics)		f_{IN} = 20 MHz		92		dBc
		f_{IN} = 70 MHz		95		dBc
		f_{IN} = 100 MHz		94		dBc
		f_{IN} = 170 MHz	77	88		dBc
		f_{IN} = 300 MHz		85		dBc
Two-tone intermodulation distortion	IMD	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		82		dBFS
Crosstalk		20-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel		95		dB
Input overload recovery		Recovery to within 1% (of full-scale) for 6 dB overload with sine-wave input		1		Clock cycle
AC power-supply rejection ratio	PSRR	For 50-mV_{PP} signal on AVDD supply, up to 10 MHz		30		dB
Effective number of bits	ENOB	f_{IN} = 170 MHz		11.45		LSBs
Differential nonlinearity	DNL	f_{IN} = 170 MHz	–0.95	±0.5	1.7	LSBs
Integrated nonlinearity	INL	f_{IN} = 170 MHz		±2	±4.5	LSBs

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ELECTRICAL CHARACTERISTICS: GENERAL

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, and –1 dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		ADS4249			UNIT
		MIN	TYP	MAX	
ANALOG INPUTS					
Differential input voltage range			2		V_{PP}
Differential input resistance (at 200 MHz)			0.75		kΩ
Differential input capacitance (at 200 MHz)			3.7		pF
Analog input bandwidth (with 50-Ω source impedance, and 50-Ω termination)			550		MHz
Analog input common-mode current (per input pin of each channel)			1.5		µA/MSPS
Common-mode output voltage	VCM		0.95[1]		V
VCM output current capability			4		mA
DC ACCURACY					
Offset error		–15	2.5	15	mV
Temperature coefficient of offset error			0.003		mV/°C
Gain error as a result of internal reference inaccuracy alone	E_{GREF}	–2		2	%FS
Gain error of channel alone	E_{GCHAN}		±0.1	1	%FS
Temperature coefficient of E_{GCHAN}			0.002		Δ%/°C
POWER SUPPLY					
IAVDD Analog supply current			167	190	mA
IDRVDD Output buffer supply current LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz			144	160	mA
IDRVDD Output buffer supply current CMOS interface, no load capacitance, f_{IN} = 2.5 MHz[2]			94		mA
Analog power			301	342	mW
Digital power LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz			259	288	mW
Digital power CMOS interface, 8-pF external load capacitance[2] f_{IN} = 2.5 MHz			169		mW
Global power-down				25	mW

(1) VCM changes to 0.87 V when serial register bits HIGH PERF MODE[7:2] are set.

(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Application Information*).

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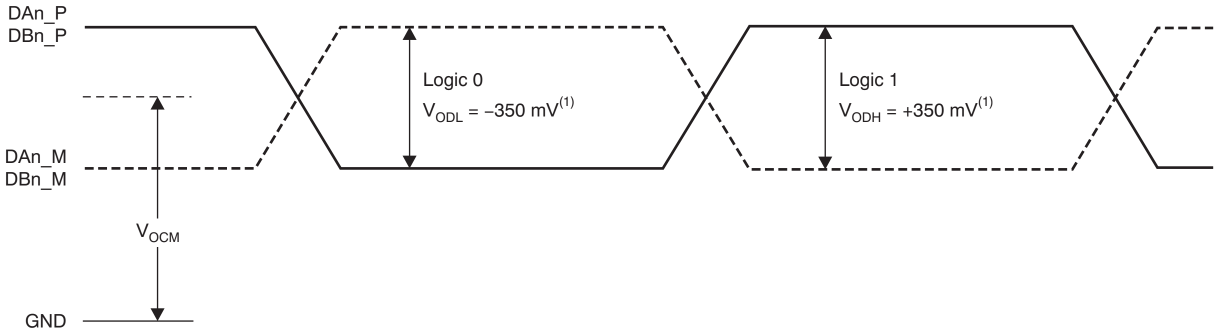
DIGITAL CHARACTERISTICS

At AVDD = 1.8 V and DRVDD = 1.8 V, unless otherwise noted. DC specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level '0' or '1'.

PARAMETER		TEST CONDITIONS	ADS4249 MIN	ADS4249 TYP	ADS4249 MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3)(1)						
High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input current	SDATA, SCLK(2)	V_{HIGH} = 1.8 V		10		µA
	SEN(3)	V_{HIGH} = 1.8 V		0		µA
Low-level input current	SDATA, SCLK	V_{LOW} = 0 V		0		µA
	SEN	V_{LOW} = 0 V		10		µA
DIGITAL OUTPUTS, CMOS INTERFACE (DA[13:0], DB[13:0], CLKOUT, SDOUT)						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS, LVDS INTERFACE						
High-level output differential voltage	V_{ODH}	With an external 100-Ω termination	270	350	430	mV
Low-level output differential voltage	V_{ODL}	With an external 100-Ω termination	–430	–350	–270	mV
Output common-mode voltage	V_{OCM}		0.9	1.05	1.25	V

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK have internal 150-kΩ pull-down resistor.
(3) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up is weak, SEN can also be driven by 1.8 V or 3.3 V CMOS buffers.



(1) With external 100-Ω termination.

Figure 1. LVDS Output Voltage Levels

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TIMING REQUIREMENTS: LVDS and CMOS Modes

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5 pF, and R_{LOAD} = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

Table 2. LVDS and CMOS Modes[1]

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.5	0.8	1.1	ns
	Aperture delay matching	Between the two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150		ps
t_J	Aperture jitter			140		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		50	100	µs
		Time to valid data after coming out of GLOBAL power-down mode		100	500	µs
	ADC latency[2]	Default latency after reset		16		Clock cycles
		Digital functions enabled (EN DIGITAL = 1)		24		Clock cycles
DDR LVDS MODE[3]						
t_{SU}	Data setup time	Data valid[4] to zero-crossing of CLKOUTP	0.6	0.88		ns
t_H	Data hold time	Zero-crossing of CLKOUTP to data becoming invalid[4]	0.33	0.55		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	5.0	6.0	7.5	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM)		48		%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100 mV to +100 mV Fall time measured from +100 mV to –100 mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.13		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to +100 mV Fall time measured from +100 mV to –100 mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.13		ns
PARALLEL CMOS MODE						
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	4.5	6.2	8.5	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		50		%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.7		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.7		ns

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(3) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(4) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

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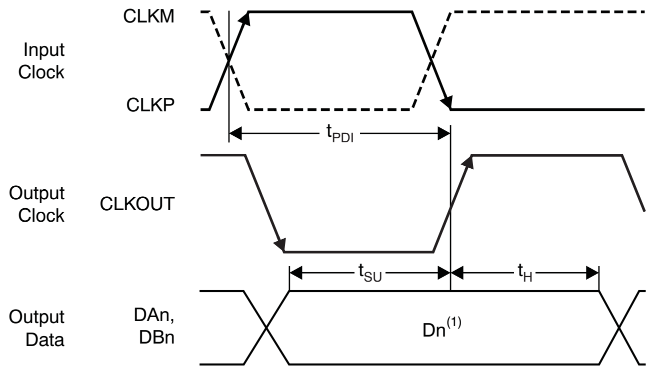
Table 3. LVDS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)			t_{PDI}, CLOCK PROPAGATION DELAY (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	5.9	6.6		0.35	0.6		5.0	6.0	7.5
80	4.5	5.2		0.35	0.6		5.0	6.0	7.5
125	2.3	2.9		0.35	0.6		5.0	6.0	7.5
160	1.5	2		0.33	0.55		5.0	6.0	7.5
185	1.3	1.6		0.33	0.55		5.0	6.0	7.5
200	1.1	1.4		0.33	0.55		5.0	6.0	7.5
230	0.76	1.06		0.33	0.55		5.0	6.0	7.5

Table 4. CMOS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	TIMINGS SPECIFIED WITH RESPECT TO CLKOUT								
	SETUP TIME (1) (ns)			HOLD TIME (1) (ns)			t_{PDI}, CLOCK PROPAGATION DELAY (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65	6.1	6.7		6.7	7.5		4.5	6.2	8.5
80	4.7	5.2		5.3	6		4.5	6.2	8.5
125	2.7	3.1		3.1	3.6		4.5	6.2	8.5
160	1.6	2.1		2.3	2.8		4.5	6.2	8.5
185	1.1	1.6		1.9	2.4		4.5	6.2	8.5
200	1	1.4		1.7	2.2		4.5	6.2	8.5

(1) In CMOS mode, setup time is measured from the beginning of data valid to 50% of the CLKOUT rising edge, whereas hold time is measured from 50% of the CLKOUT rising edge to data becoming invalid. Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.



(1) Dn = bits D0, D1, D2, etc. of channels A and B.

Figure 2. CMOS Interface Timing Diagram

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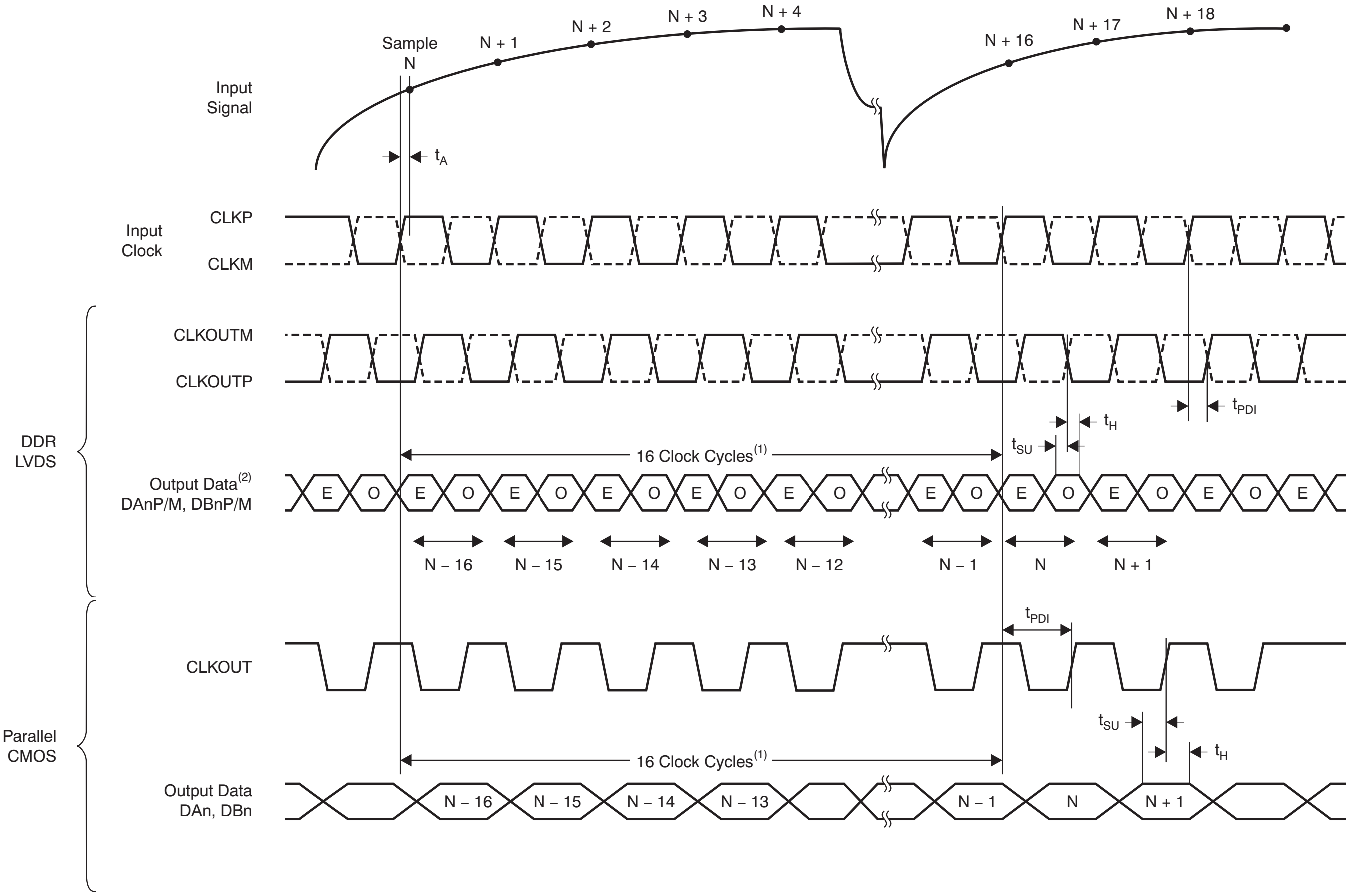

(1) ADC latency after reset. At higher sampling frequencies, t_{PDI} is greater than one clock cycle, which then makes the overall latency = ADC latency + 1.

(2) E = even bits (D0, D2, D4, etc.); O = odd bits (D1, D3, D5, etc.).

Figure 3. Latency Timing Diagram

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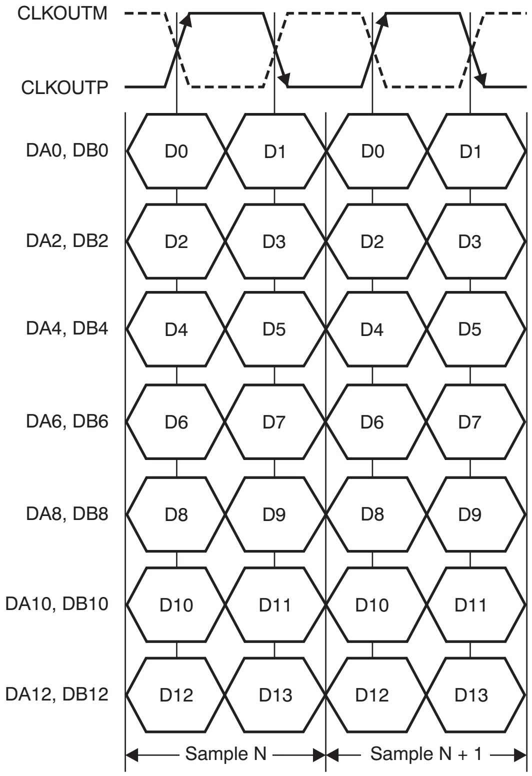

Figure 4. LVDS Interface Timing Diagram

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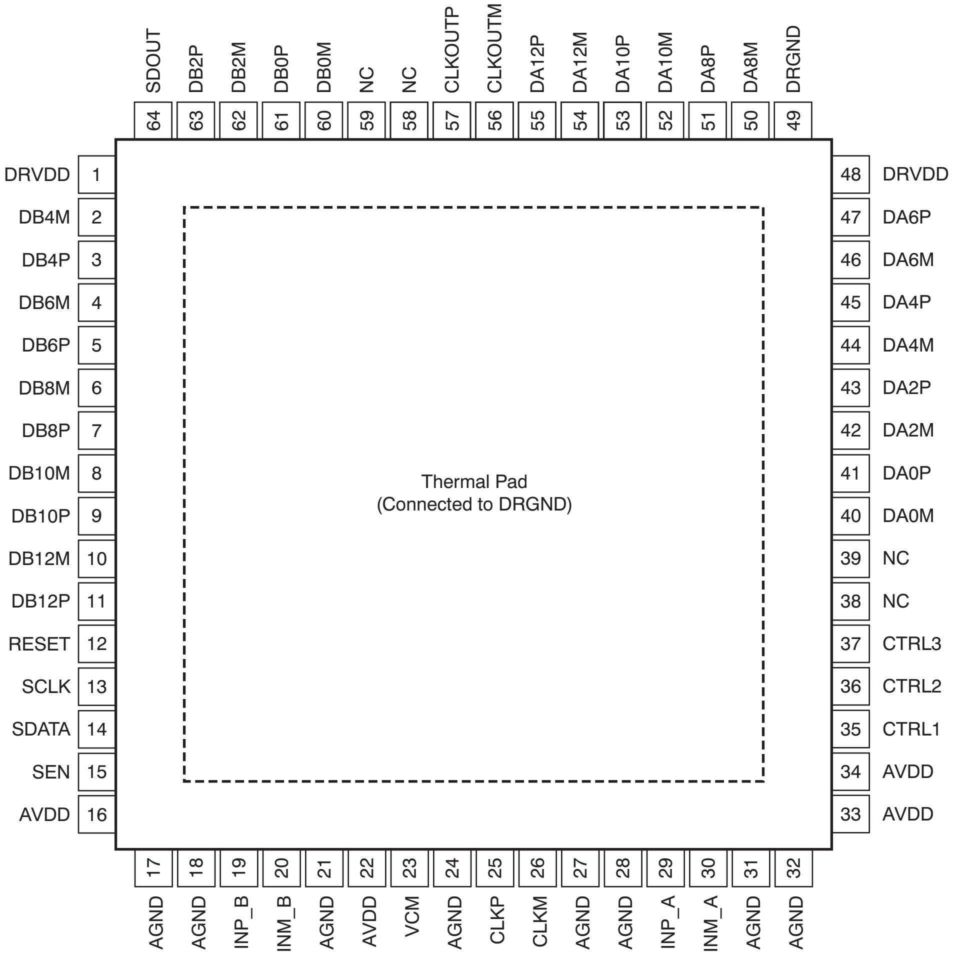
PIN CONFIGURATION: LVDS MODE

RGC PACKAGE(1)
QFN-64
(TOP VIEW)



(1) The PowerPAD is connected to DRGND.

NOTE: NC = do not connect; must float.

Figure 5. LVDS Mode

Pin Descriptions: LVDS Mode

PIN NUMBER	PIN NAME	# OF PINS	FUNCTION	DESCRIPTION
1, 48	DRVDD	2	Input	Output buffer supply
12	RESET	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor.
13	SCLK	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150-kΩ pull-down resistor.
14	SDATA	1	Input	Serial interface data input; this pin has an internal 150-kΩ pull-down resistor.
15	SEN	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150-kΩ pull-up resistor to AVDD.

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Pin Descriptions: LVDS Mode (continued)

PIN NUMBER	PIN NAME	# OF PINS	FUNCTION	DESCRIPTION
16, 22, 33, 34	AVDD	4	Input	Analog power supply
17, 18, 21, 24, 27, 28, 31, 32	AGND	8	Input	Analog ground
19	INP_B	1	Input	Differential analog positive input, channel B
20	INM_B	1	Input	Differential analog negative input, channel B
23	VCM	1	Output	This pin outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins
25	CLKP	1	Input	Differential clock positive input
26	CLKM	1	Input	Differential clock negative input
29	INP_A	1	Input	Differential analog positive input, channel A
30	INM_A	1	Input	Differential analog negative input, channel A
35	CTRL1	1	Input	Digital control input pins. Together, they control the various power-down modes.
36	CTRL2	1	Input	Digital control input pins. Together, they control the various power-down modes.
37	CTRL3	1	Input	Digital control input pins. Together, they control the various power-down modes.
49, PAD	DRGND	2	Input	Output buffer ground
56	CLKOUTM	1	Output	Differential clock negative output
57	CLKOUTP	1	Output	Differential clock positive output
64	SDOUT	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state.
Refer to Figure 5	DA0P, DA0M	2	Output	Channel A differential output data pair, D0 and D1 multiplexed
Refer to Figure 5	DA2P, DA2M	2	Output	Channel A differential output data D2 and D3 multiplexed
Refer to Figure 5	DA4P, DA4M	2	Output	Channel A differential output data D4 and D5 multiplexed
Refer to Figure 5	DA6P, DA6M	2	Output	Channel A differential output data D6 and D7 multiplexed
Refer to Figure 5	DA8P, DA8M	2	Output	Channel A differential output data D8 and D9 multiplexed
Refer to Figure 5	DA10P, DA10M	2	Output	Channel A differential output data D10 and D11 multiplexed
Refer to Figure 5	DA12P, DA12M	2	Output	Channel A differential output data D12 and D13 multiplexed
Refer to Figure 5	DB0P, DB0M	2	Output	Channel B differential output data pair, D0 and D1 multiplexed
Refer to Figure 5	DB2P, DB2M	2	Output	Channel B differential output data D2 and D3 multiplexed
Refer to Figure 5	DB4P, DB4M	2	Output	Channel B differential output data D4 and D5 multiplexed
Refer to Figure 5	DB6P, DB6M	2	Output	Channel B differential output data D6 and D7 multiplexed
Refer to Figure 5	DB8P, DB8M	2	Output	Channel B differential output data D8 and D9 multiplexed
Refer to Figure 5	DB10P, DB10M	2	Output	Channel B differential output data D10 and D11 multiplexed
Refer to Figure 5	DB12P, DB12M	2	Output	Channel B differential output data D12 and D13 multiplexed
Refer to Figure 5	NC	4	—	Do not connect, must be floated

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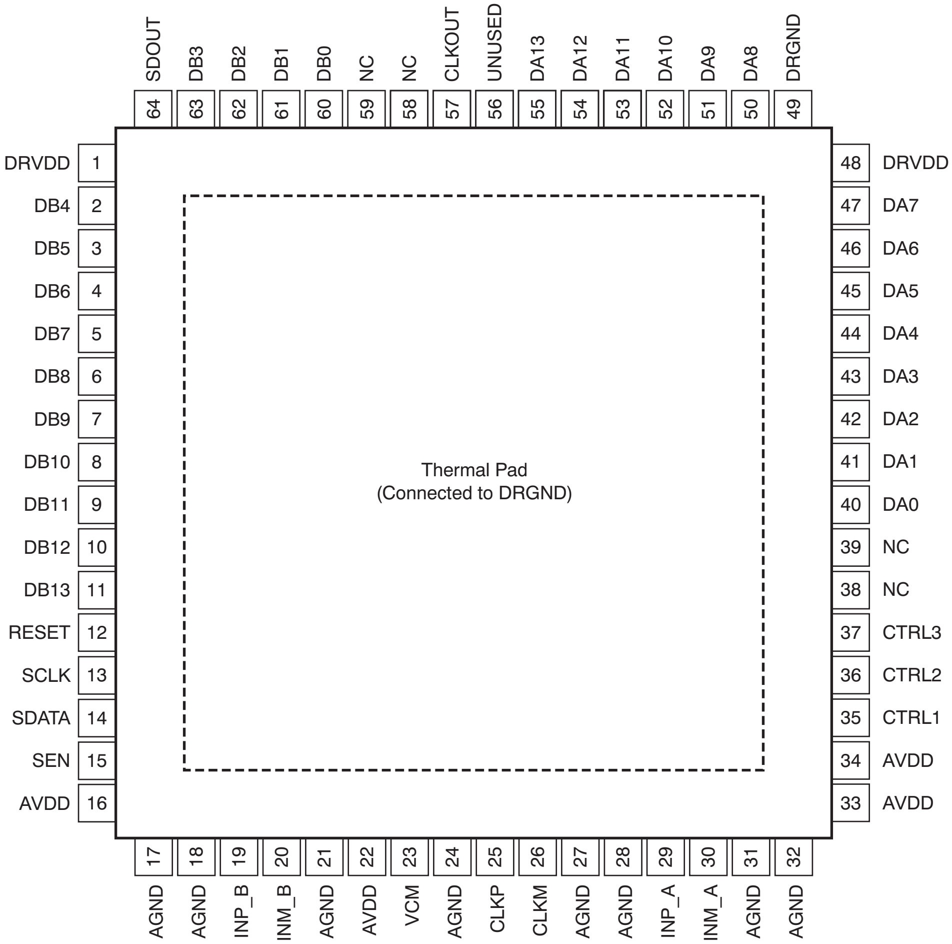
PIN CONFIGURATION: CMOS MODE

RGC PACKAGE[(2)]
QFN-64
(TOP VIEW)



(2) The PowerPAD is connected to DRGND.

NOTE: NC = do not connect; must float.

Figure 6. CMOS Mode

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Pin Descriptions: CMOS Mode

PIN NUMBER	PIN NAME	# OF PINS	FUNCTION	DESCRIPTION
1, 48	DRVDD	2	Input	Output buffer supply
12	RESET	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor.
13	SCLK	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150-kΩ pull-down resistor.
14	SDATA	1	Input	Serial interface data input; this pin has an internal 150-kΩ pull-down resistor.
15	SEN	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150-kΩ pull-up resistor to AVDD.
16, 22, 33, 34	AVDD	4	Input	Analog power supply
17, 18, 21, 24, 27, 28, 31, 32	AGND	8	Input	Analog ground
19	INP_B	1	Input	Differential analog positive input, channel B
20	INM_B	1	Input	Differential analog negative input, channel B
23	VCM	1	Output	This pin outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins
25	CLKP	1	Input	Differential clock positive input
26	CLKM	1	Input	Differential clock negative input
29	INP_A	1	Input	Differential analog positive input, channel A
30	INM_A	1	Input	Differential analog negative input, channel A
35	CTRL1	1	Input	Digital control input pins. Together, they control various power-down modes.
36	CTRL2	1	Input	Digital control input pins. Together, they control various power-down modes.
37	CTRL3	1	Input	Digital control input pins. Together, they control various power-down modes.
49, PAD	DRGND	2	Input	Output buffer ground
56	UNUSED	1	—	This pin is not used in the CMOS interface
57	CLKOUT	1	Output	CMOS output clock
64	SDOUT	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state.
Refer to Figure 6	DA0 to DA11	12	Output	Channel A ADC output data bits, CMOS levels
Refer to Figure 6	DA12 to DA13	2	Output	Channel A ADC output data bits, CMOS levels
Refer to Figure 6	DB0 to DB11	12	Output	Channel B ADC output data bits, CMOS levels
Refer to Figure 6	DB12 to DB13	2	Output	Channel B ADC output data bits, CMOS levels
—	NC	4	—	Do not connect, must be floated

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FUNCTIONAL BLOCK DIAGRAM

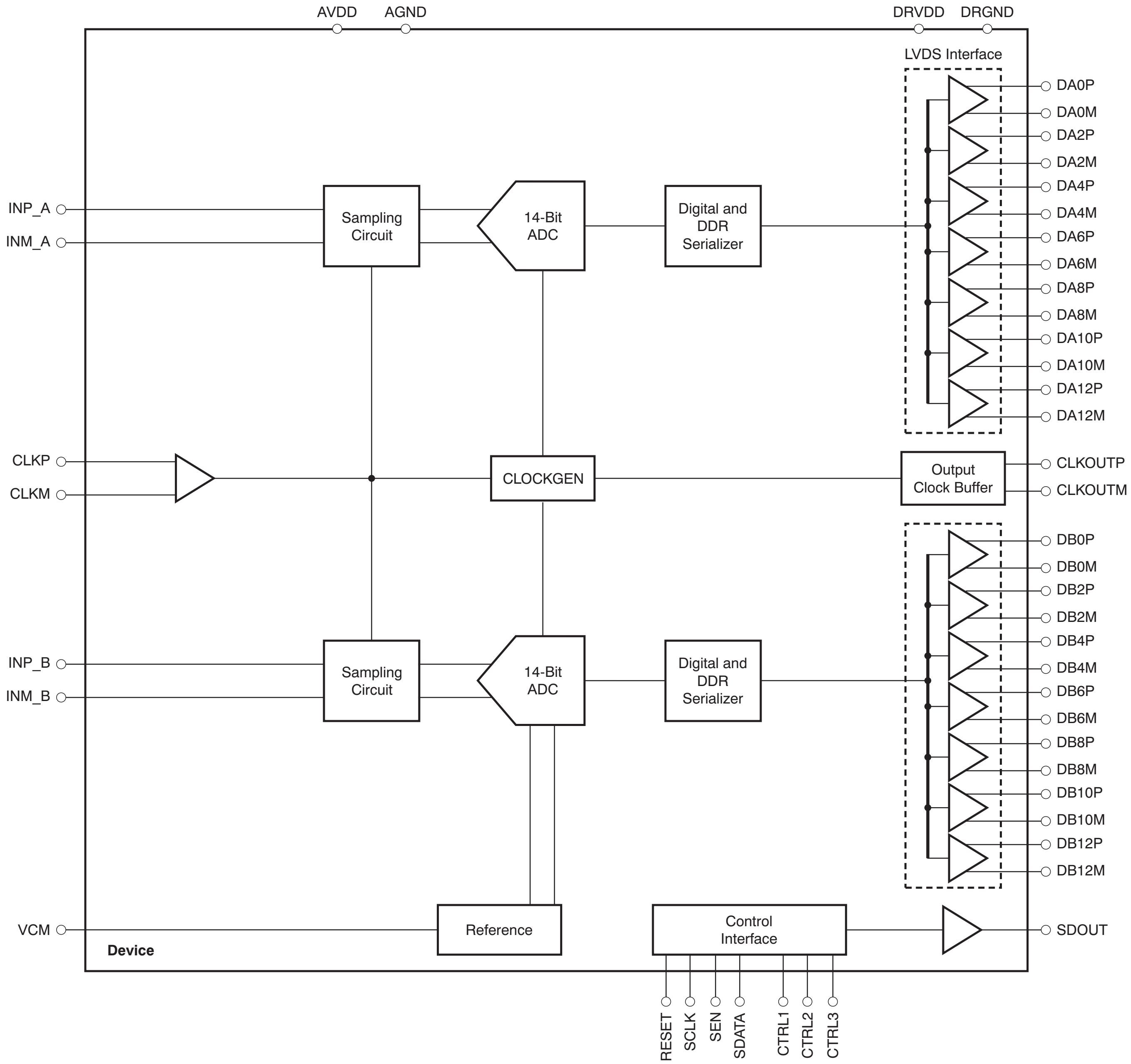

Figure 7. Block Diagram

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DEVICE CONFIGURATION

The ADS4249 can be configured independently using either parallel interface control or serial interface programming.

PARALLEL CONFIGURATION ONLY

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 5 to Table 8). There is no need to apply a reset and SDATA can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. Table 5 describes the modes controlled by the parallel pins.

Table 5. Parallel Pin Definition

PIN	CONTROL MODE
SCLK	Low-speed mode selection
SEN	Output data format and output interface selection
CTRL1	Together, these pins control the power-down modes
CTRL2	
CTRL3	

SERIAL INTERFACE CONFIGURATION ONLY

To enable this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Serial Register Map* section describes the register programming and the register reset process in more detail.

USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this option, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see Table 8). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to '1'. After reset, the RESET pin must be kept low. The *Serial Register Map* section describes register programming and the register reset process in more detail.

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PARALLEL CONFIGURATION DETAILS

The functions controlled by each parallel pin are described in Table 6, Table 7, and Table 8. A simple way of configuring the parallel pins is shown in Figure 8.

Table 6. SCLK Control Pin

VOLTAGE APPLIED ON SCLK	DESCRIPTION
Low	Low-speed mode is disabled
High	Low-speed mode is enabled

Table 7. SEN Control Pin

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 (+50mV/0mV)	Twos complement and parallel CMOS output
(3/8) AVDD (±50mV)	Offset binary and parallel CMOS output
(5/8) 2AVDD (±50mV)	Offset binary and DDR LVDS output
AVDD (0mV/–50mV)	Twos complement and DDR LVDS output

Table 8. CTRL1, CTRL2, and CTRL3 Pins

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Global power-down
High	Low	High	Channel A standby, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data are multiplexed and output on the DB[13:0] pins. See the *Multiplexed Mode of Operation* section in the Application Information for further details.

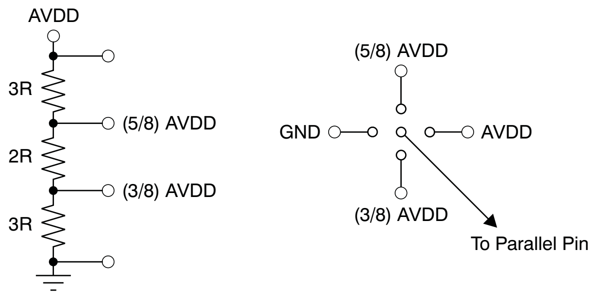

Figure 8. Simple Scheme to Configure the Parallel Pins

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SERIAL INTERFACE DETAILS

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. Initialization can be accomplished in one of two ways:

1. Through a hardware reset by applying a high pulse on the RESET pin (of width greater than 10 ns), as shown in Figure 9 and Table 9; or
2. By applying a software reset. When using the serial interface, set the RESET bit high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low. See Table 10 and Figure 10 for reset timing.

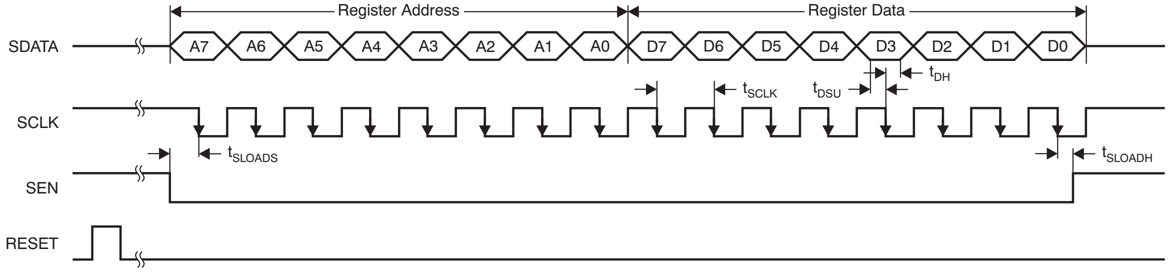

Figure 9. Serial Interface Timing

Table 9. Serial Interface Timing Characteristics(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to $1/t_{SCLK}$)	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, and DRVDD = 1.8 V, unless otherwise noted.

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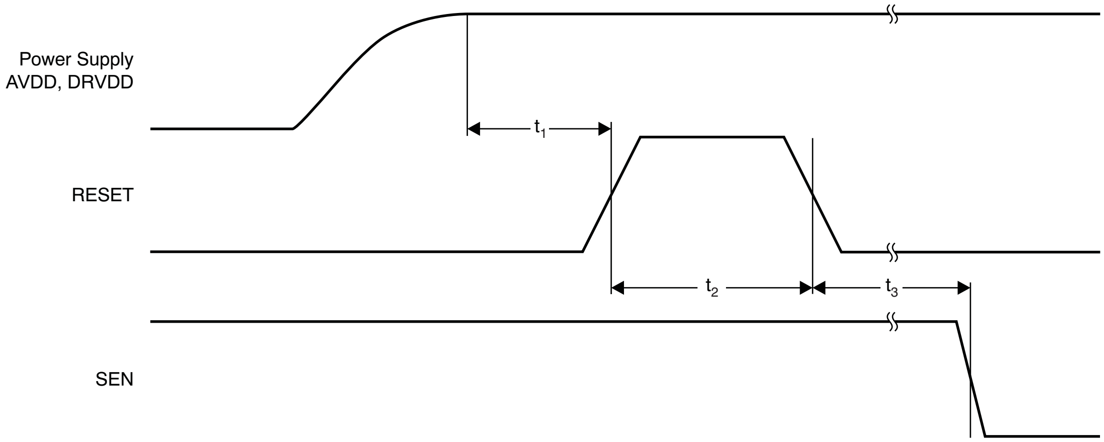

NOTE: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 10. Reset Timing Diagram

Table 10. Reset Timing (Only when Serial Interface is Used)[1]

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

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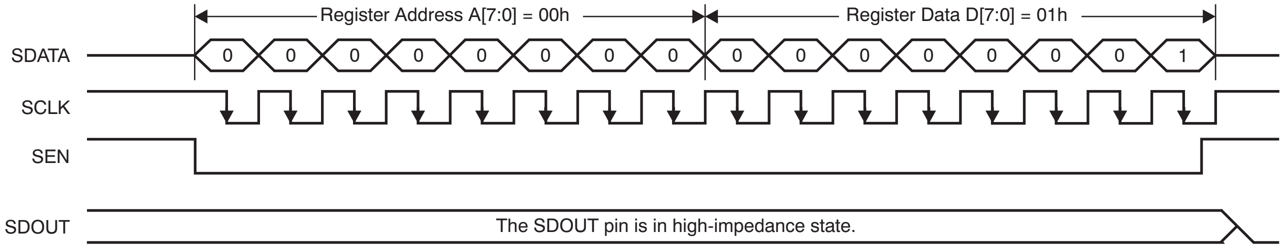
Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To use readback mode, follow this procedure:

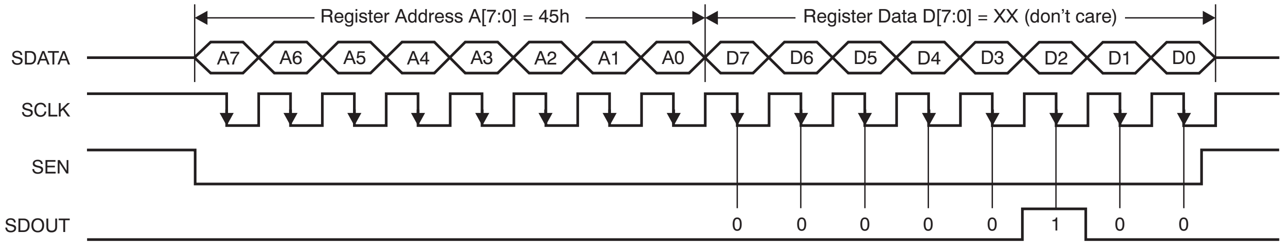
1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

The serial register readout works with both CMOS and LVDS interfaces on pin 64. See Figure 11 for serial readout timing diagram.

When READOUT is disabled, the SDOUT pin is in high-impedance state.



a) Enable serial readout (READOUT = 1)



The SDOUT pin functions as serial readout (READOUT = 1).

b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)

Figure 11. Serial Readout Timing Diagram

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SERIAL REGISTER MAP

Table 11 summarizes the functions supported by the serial interface.

Table 11. Serial Interface Register Map(1)

REGISTER ADDRESS	**REGISTER DATA**							
A[7:0] (Hex)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00	0	0	0	0	0	0	RESET	READOUT
01	LVDS SWING						0	0
03	0	0	0	0	0	0	HIGH PERF MODE 2	HIGH PERF MODE 1
25	CH A GAIN				0	CH A TEST PATTERNS		
29	0	0	0	DATA FORMAT		0	0	0
2B	CH B GAIN				0	CH B TEST PATTERNS		
3D	0	0	ENABLE OFFSET CORR	0	0	0	0	0
3F	0	0	CUSTOM PATTERN D[13:8]					
40	CUSTOM PATTERN D[7:0]							
41	LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	DIS OBUF	
42	CLKOUT FALL POSN		CLKOUT RISE POSN		EN DIGITAL	0	0	0
45	STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0
4A	0	0	0	0	0	0	0	HIGH FREQ MODE CH B
58	0	0	0	0	0	0	0	HIGH FREQ MODE CH A
BF	CH A OFFSET PEDESTAL						0	0
C1	CH B OFFSET PEDESTAL						0	0
CF	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
EF	0	0	0	EN LOW SPEED MODE	0	0	0	0
F1	0	0	0	0	0	0	EN LVDS SWING	
F2	0	0	0	0	LOW SPEED MODE CH A	0	0	0
2	0	HIGH PERF MODE3	0	0	0	0	0	0
D5	0	0	0	HIGH PERF MODE4	HIGH PERF MODE5	0	0	0
D7	0	0	0	0	HIGH PERF MODE6	HIGH PERF MODE7	0	0
DB	0	0	HIGH PERF MODE8	0	0	0	0	LOW SPEED MODE CH B

(1) Multiple functions in a register can be programmed in a single write operation. All registers default to '0' after reset.

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DESCRIPTION OF SERIAL REGISTERS

Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] **Always write '0'**

Bit 1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the SDOUT pin is placed in a high-impedance state.
1 = Serial readout enabled; the SDOUT pin functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the *Serial Register Readout* section.

Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] **LVDS SWING: LVDS swing programmability**

These bits program the LVDS swing. Set the EN LVDS SWING bit to '1' before programming swing.
000000 = Default LVDS swing; ±350 mV with external 100-Ω termination
011011 = LVDS swing ±410 mV
110010 = LVDS swing ±465 mV
010100 = LVDS swing ±570 mV
111110 = LVDS swing ±200 mV
001111 = LVDS swing ±125 mV

Bits[1:0] **Always write '0'**

Register Address 03h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH PERF MODE 2	HIGH PERF MODE 1

Bits[7:2] **Always write '0'**

Bits[1:0] **HIGH PERF MODE[2:1]: High-performance mode**

00 = Default performance
01 = Do not use
10 = Do not use
11 = Obtain best performance across sample clock and input signal frequencies

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Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
CH A GAIN				0	CH A TEST PATTERNS		

Bits[7:4] **CH A GAIN: Channel A gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel A.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

Bit 3 **Always write '0'**

Bits[2:0] **CH A TEST PATTERNS: Channel A data capture**

These bits verify data capture for channel A.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
The output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

Register Address 29h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	DATA FORMAT		0	0	0

Bits[7:5] **Always write '0'**

Bits[4:3] **DATA FORMAT: Data format selection**

00 = Twos complement
01 = Twos complement
10 = Twos complement
11 = Offset binary

Bits[2:0] **Always write '0'**

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Register Address 2Bh (Default = 00h)

7	6	5	4	3	2	1	0
CH B GAIN				0	CH B TEST PATTERNS		

Bits[7:4] **CH B GAIN: Channel B gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel B.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

Bit 3 **Always write '0'**

Bits[2:0] **CH B TEST PATTERNS: Channel B data capture**

These bits verify data capture for channel B.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
The output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

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Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	ENABLE OFFSET CORR	0	0	0	0	0

Bits[7:6] **Always write '0'**

Bit 5 **ENABLE OFFSET CORR: Offset correction setting**

This bit enables the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits[4:0] **Always write '0'**

Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8

Bits[7:6] **Always write '0'**

Bits[5:0] **CUSTOM PATTERN D[13:8]**

These are the six upper bits of the custom pattern available at the output instead of ADC data. The ADS4249 custom pattern is 14-bit.

Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0

Bits[7:0] **CUSTOM PATTERN D[7:0]**

These are the eight lower bits of the custom pattern available at the output instead of ADC data. The ADS4249 custom pattern is 14-bit; use the CUSTOM PATTERN D[13:0] register bits.

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Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	DIS OBUF	

Bits[7:6] **LVDS CMOS: Interface selection**

These bits select the interface.
00 = DDR LVDS interface
01 = DDR LVDS interface
10 = DDR LVDS interface
11 = Parallel CMOS interface

Bits[5:4] **CMOS CLKOUT STRENGTH**

These bits control the strength of the CMOS output clock.
00 = Maximum strength (recommended)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bits[3:2] **Always write '0'**

Bits[1:0] **DIS OBUF**

These bits power down data and clock output buffers for both the CMOS and LVDS output interface. When powered down, the output buffers are in 3-state.
00 = Default
01 = Power-down data output buffers for channel B
10 = Power-down data output buffers for channel A
11 = Power-down data output buffers for both channels as well as the clock output buffer

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Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
CLKOUT FALL POSN		CLKOUT RISE POSN		EN DIGITAL	0	0	0

Bits[7:6] **CLKOUT FALL POSN**

In LVDS mode:
00 = Default
01 = The falling edge of the output clock advances by 450 ps
10 = The falling edge of the output clock advances by 150 ps
11 = The falling edge of the output clock is delayed by 550 ps
In CMOS mode:
00 = Default
01 = The falling edge of the output clock is delayed by 150 ps
10 = Do not use
11 = The falling edge of the output clock advances by 100 ps

Bits[5:6] **CLKOUT RISE POSN**

In LVDS mode:
00 = Default
01 = The rising edge of the output clock advances by 450 ps
10 = The rising edge of the output clock advances by 150 ps
11 = The rising edge of the output clock is delayed by 250 ps
In CMOS mode:
00 = Default
01 = The rising edge of the output clock is delayed by 150 ps
10 = Do not use
11 = The rising edge of the output clock advances by 100 ps

Bit 3 **EN DIGITAL: Digital function enable**

0 = All digital functions disabled
1 = All digital functions (such as test patterns, gain, and offset correction) enabled

Bits[2:0] **Always write '0'**

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Register Address 45h (Default = 00h)

7	6	5	4	3	2	1	0
STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0

Bit 7 **STBY: Standby setting**

0 = Normal operation
1 = Both channels are put in standby; wakeup time from this mode is fast (typically 50 µs).

Bit 6 **LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting**

0 = LVDS output clock buffer at default strength to be used with 100-Ω external termination
1 = LVDS output clock buffer has double strength to be used with 50-Ω external termination

Bit 5 **LVDS DATA STRENGTH**

0 = All LVDS data buffers at default strength to be used with 100-Ω external termination
1 = All LVDS data buffers have double strength to be used with 50-Ω external termination

Bits[4:3] **Always write '0'**

Bit 2 **PDN GLOBAL**

0 = Normal operation
1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (typically 100 µs).

Bits[1:0] **Always write '0'**

Register Address 4Ah (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH B

Bits[7:1] **Always write '0'**

Bit 0 **HIGH FREQ MODE CH B: High-frequency mode for channel B**

0 = Default
1 = Use this mode for high input frequencies greater than 200 MHz

Register Address 58h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH A

Bits[7:1] **Always write '0'**

Bit 0 **HIGH FREQ MODE CH A: High-frequency mode for channel A**

0 = Default
1 = Use this mode for high input frequencies greater than 200 MHz

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Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
CH A OFFSET PEDESTAL						0	0

Bits[7:4] **CH A OFFSET PEDESTAL: Channel A offset pedestal selection**

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+31 by adding pedestal D7-D2.

Program bits D[7:2]

011111 = Midcode+31
011110 = Midcode+30
011101 = Midcode+29
…
000010 = Midcode+2
000001 = Midcode+1
000000 = Midcode
111111 = Midcode-1
111110 = Midcode-2
…
100000 = Midcode-32

Bits[3:0] **Always write '0'**

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Register Address C1h (Default = 00h)

7	6	5	4	3	2	1	0
CH B OFFSET PEDESTAL						0	0

Bits[7:4] **CH B OFFSET PEDESTAL: Channel B offset pedestal selection**

When offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits; see the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+31 by adding pedestal D7-D2.

Program Bits D[7:2]

011111 = Midcode+31
011110 = Midcode+30
011101 = Midcode+29
…
000010 = Midcode+2
000001 = Midcode+1
000000 = Midcode
111111 = Midcode-1
111110 = Midcode-2
…
100000 = Midcode-32

Bits[3:0] **Always write '0'**

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Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 **FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.
0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)
1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the *Offset Correction* section.

Bit 6 **Always write '0'**

Bits[5:2] **OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the *Offset Correction* section.

Bits[1:0] **Always write '0'**

Register Address EFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	EN LOW SPEED MODE	0	0	0	0

Bits[7:5] **Always write '0'**

Bit 4 **EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits**

This bit enables the control of the low-speed mode using the LOW SPEED MODE CH B and LOW SPEED MODE CH A register bits.
0 = Low-speed mode is disabled
1 = Low-speed mode is controlled by serial register bits

Bits[3:0] **Always write '0'**

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Register Address F1h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN LVDS SWING	

Bits[7:2] **Always write '0'**

Bits[1:0] **EN LVDS SWING: LVDS swing enable**

These bits enable LVDS swing control using the LVDS SWING register bits.
00 = LVDS swing control using the LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using the LVDS SWING register bits is enabled

Register Address F2h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	LOW SPEED MODE CH A	0	0	0

Bits[7:4] **Always write '0'**

Bit 3 **LOW SPEED MODE CH A: Channel A low-speed mode enable**

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel A
1 = Low-speed mode is enabled for channel A

Bits[2:0] **Always write '0'**

Register Address 2h (Default = 00h)

7	6	5	4	3	2	1	0
0	HIGH PERF MODE3	0	0	0	0	0	0

Bit 7 **Always write '0'**

Bit 6 **HIGH PERF MODE3**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

Bits[5:0] **Always write '0'**

Register Address D5h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	HIGH PERF MODE4	HIGH PERF MODE5	0	0	0

Bits[7:5] **Always write '0'**

Bit 4 **HIGH PERF MODE4**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

Bit 3 **HIGH PERF MODE5**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

Bits[2:0] **Always write '0'**

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Register Address D7h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	HIGH PERF MODE6	HIGH PERF MODE7	0	0

Bits[7:4] **Always write '0'**

Bit 3 **HIGH PERF MODE6**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

Bit 2 **HIGH PERF MODE7**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

Bits[1:0] **Always write '0'**

Register Address DBh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	HIGH PERF MODE8	0	0	0	0	LOW SPEED MODE CH B

Bits[7:6] **Always write '0'**

Bit 5 **HIGH PERF MODE8**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS).

Bits[4:1] **Always write '0'**

Bit 0 **LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel B
1 = Low-speed mode is enabled for channel B

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TYPICAL CHARACTERISTICS: ADS4249

At T_A = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

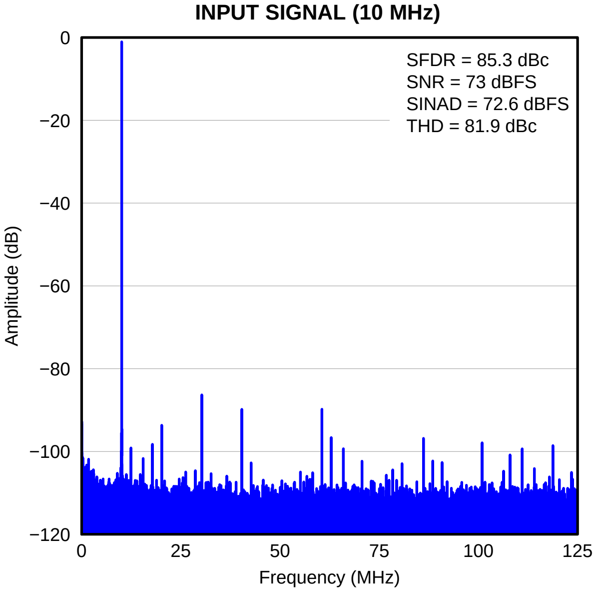

Figure 12.

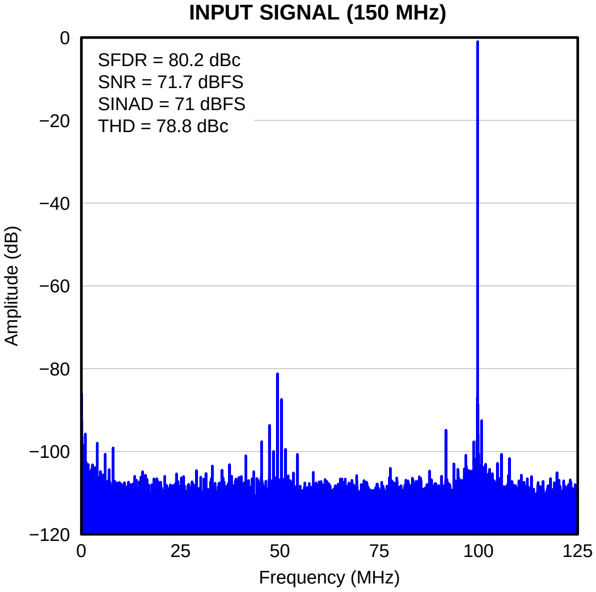

Figure 13.

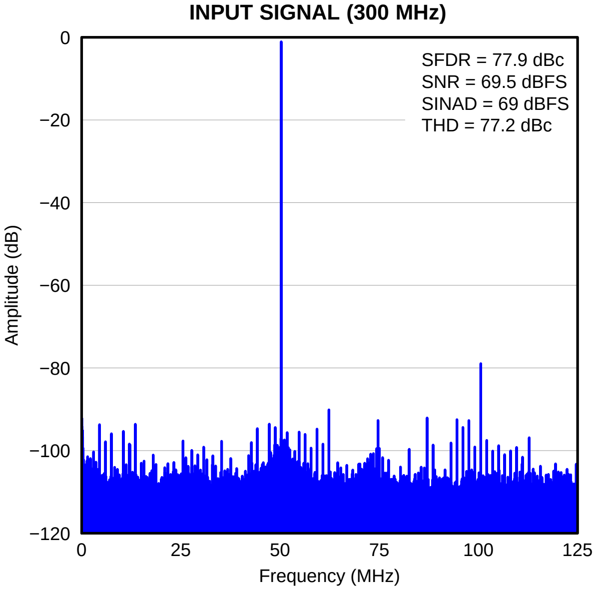

Figure 14.

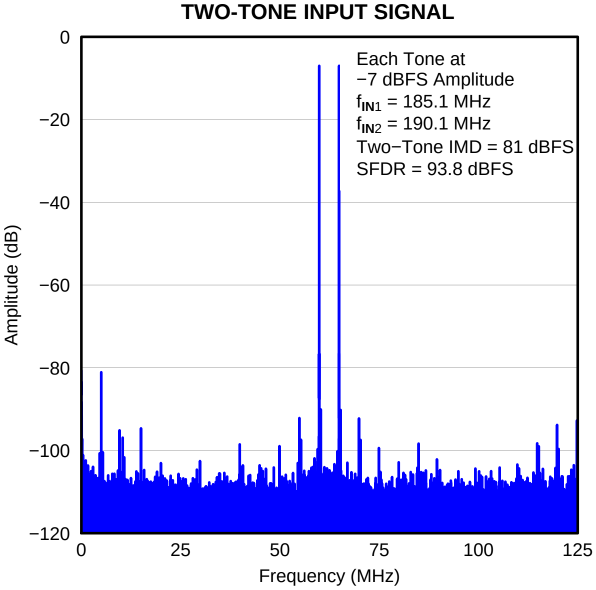

Figure 15.

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TYPICAL CHARACTERISTICS: ADS4249 (continued)

At T_A = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

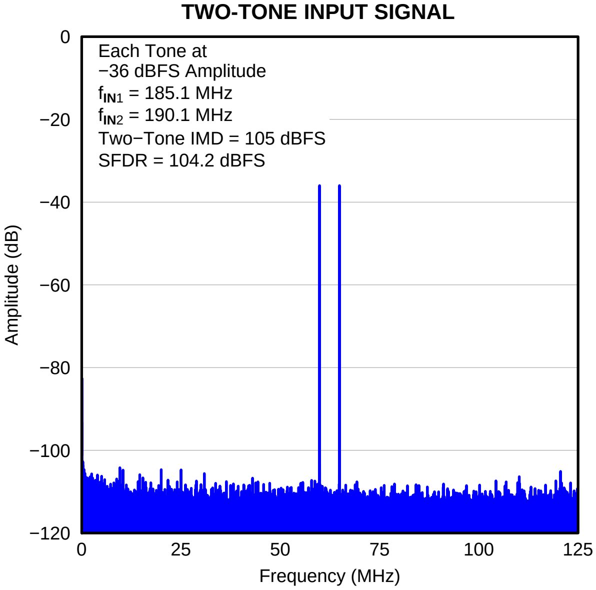

Figure 16.

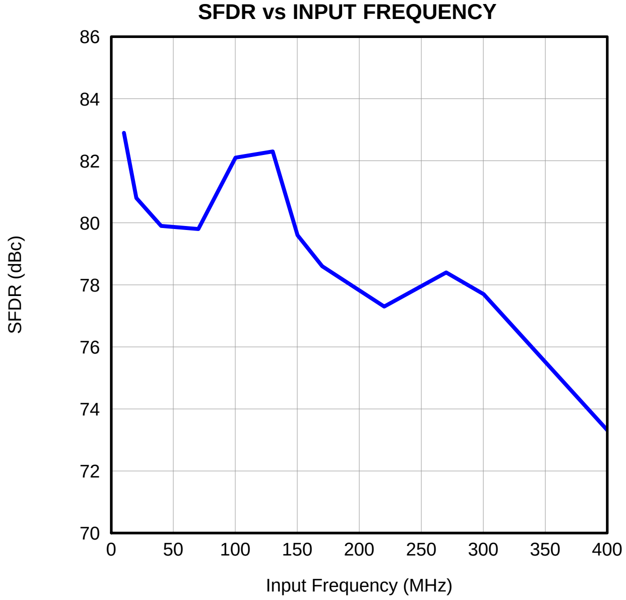

Figure 17.

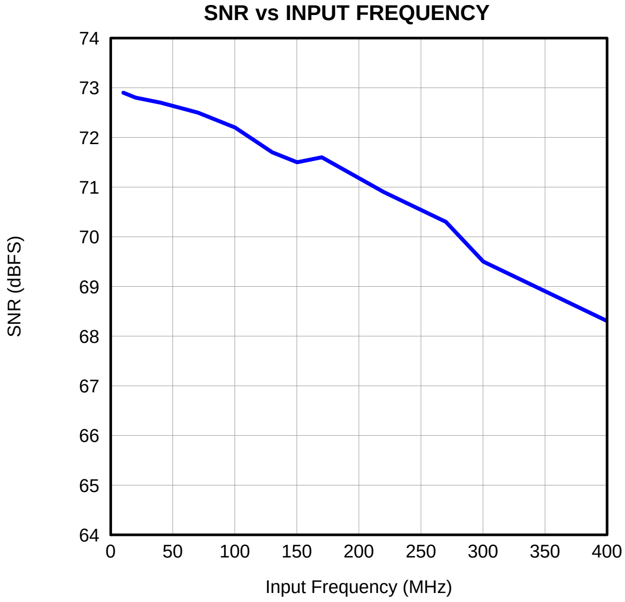

Figure 18.

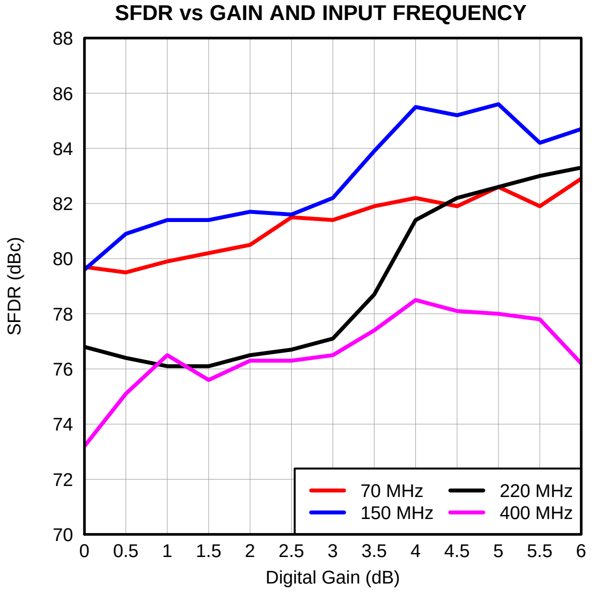

Figure 19.

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TYPICAL CHARACTERISTICS: ADS4249 (continued)

At T_A = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

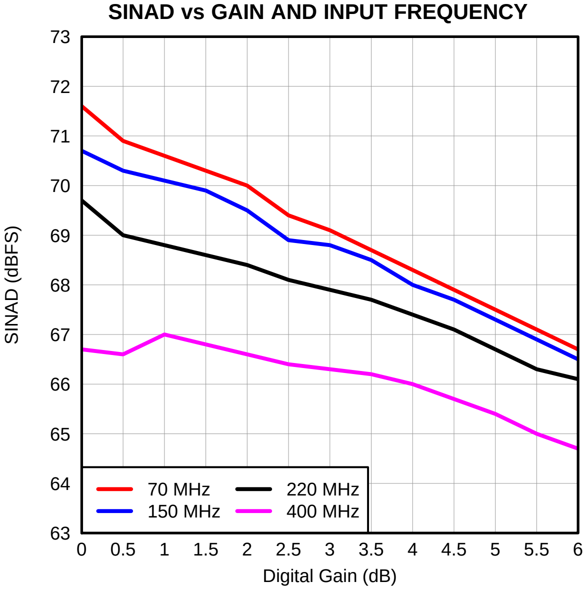

Figure 20.

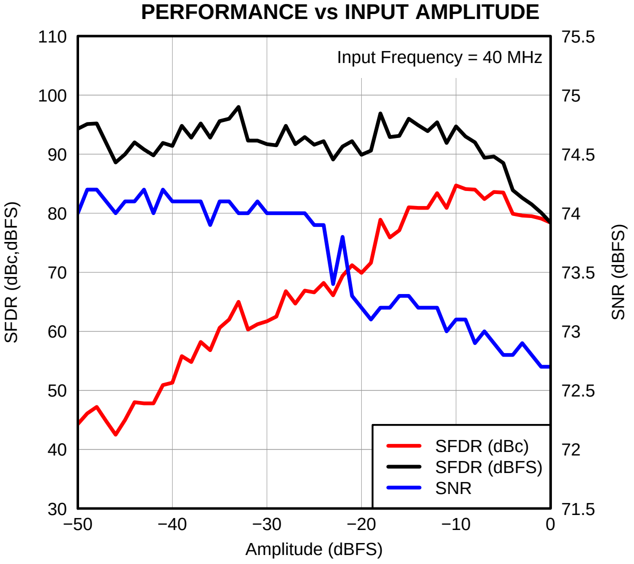

Figure 21.

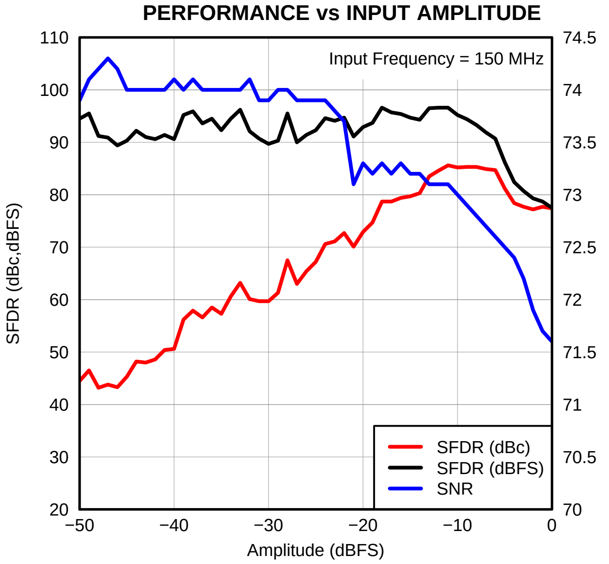

Figure 22.

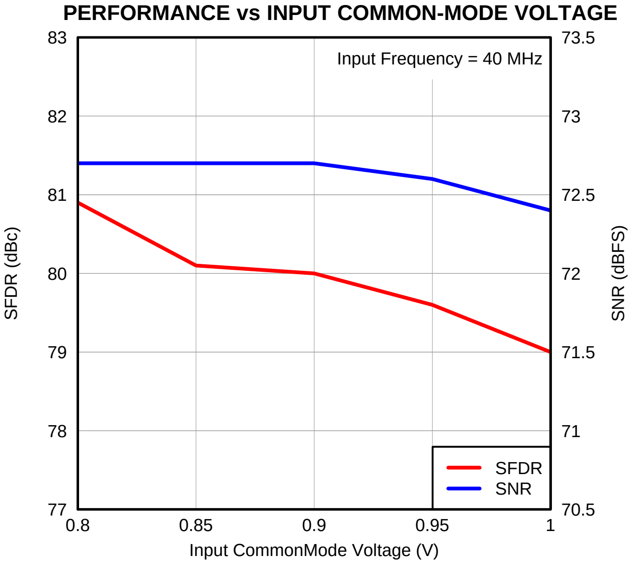

Figure 23.

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TYPICAL CHARACTERISTICS: ADS4249 (continued)

At T_A = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

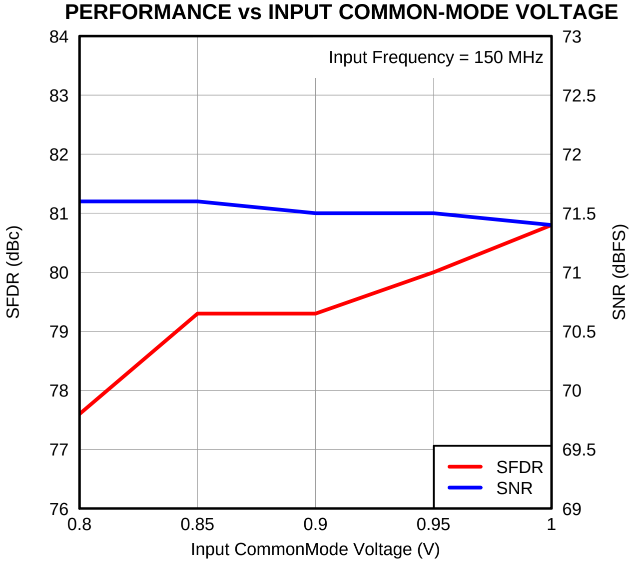

Figure 24.

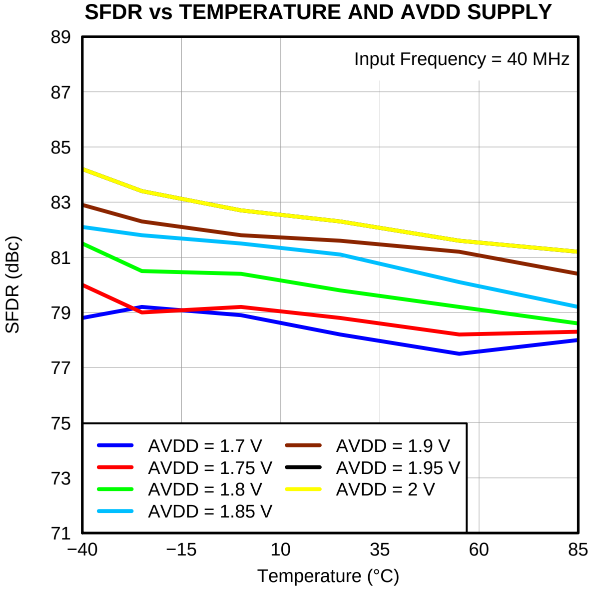

Figure 25.

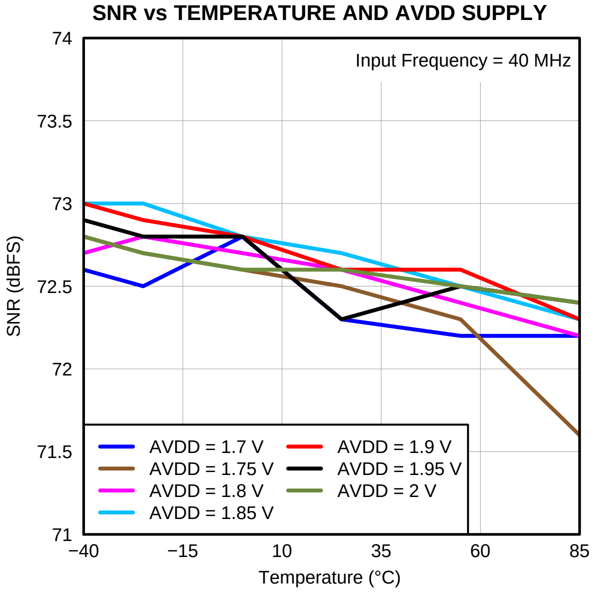

Figure 26.

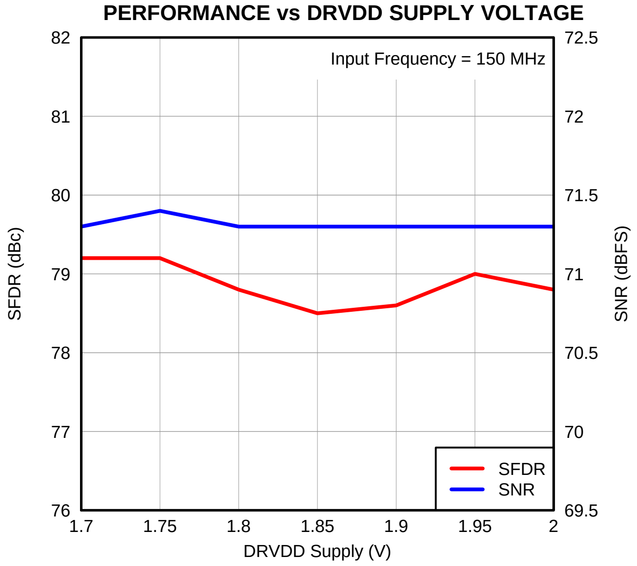

Figure 27.

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TYPICAL CHARACTERISTICS: ADS4249 (continued)

At T_A = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

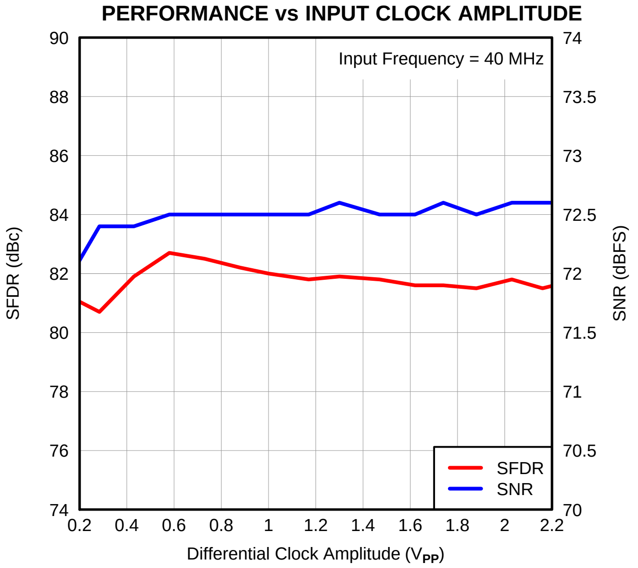

Figure 28.

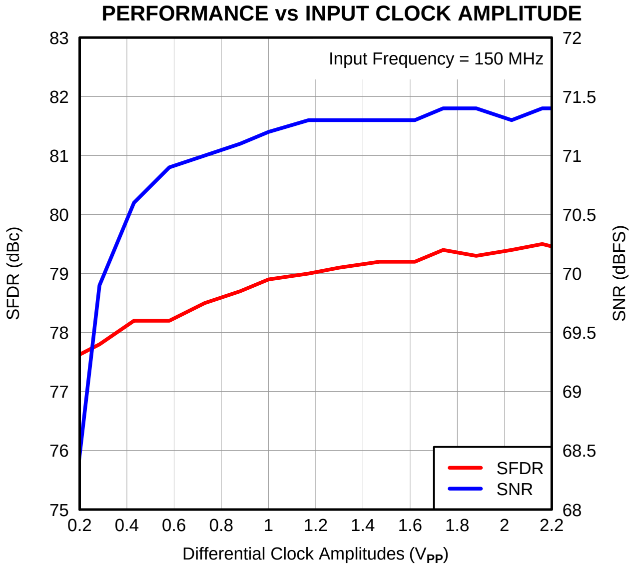

Figure 29.

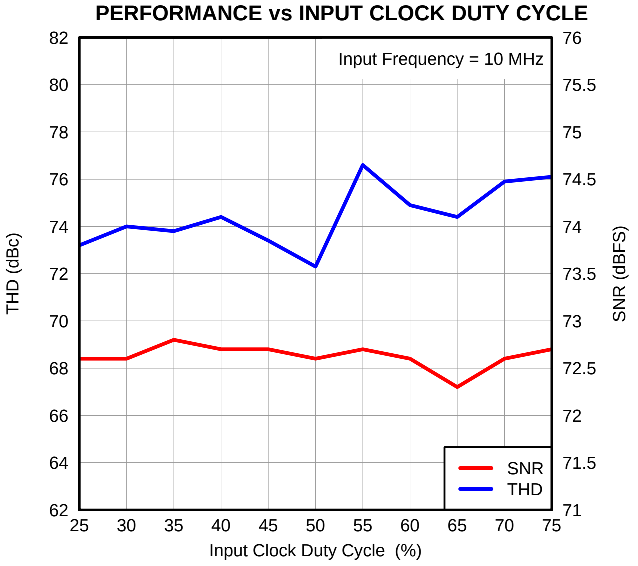

Figure 30.

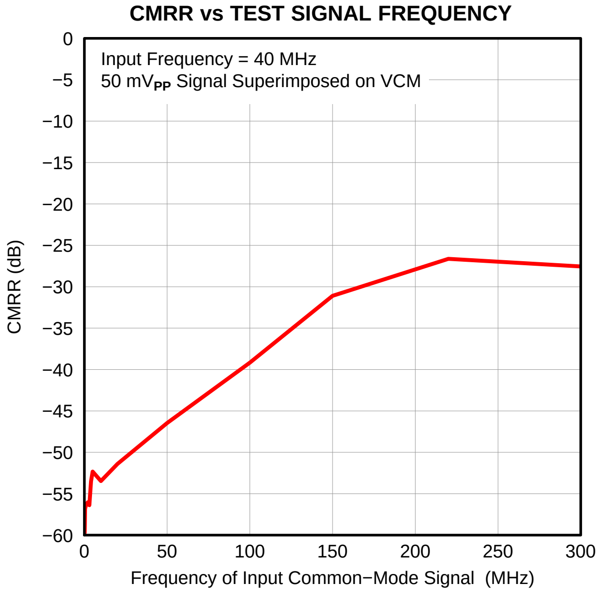

Figure 31.

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TYPICAL CHARACTERISTICS: ADS4249 (continued)

At T_A = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

CMRR SPECTRUM

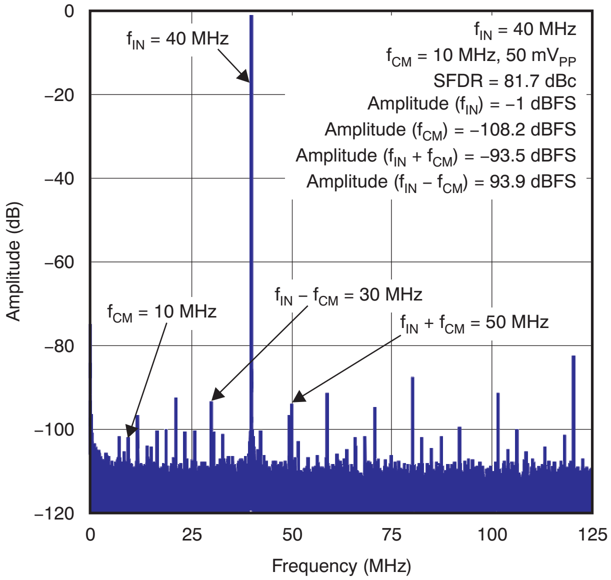

Figure 32.

PSRR vs TEST SIGNAL FREQUENCY

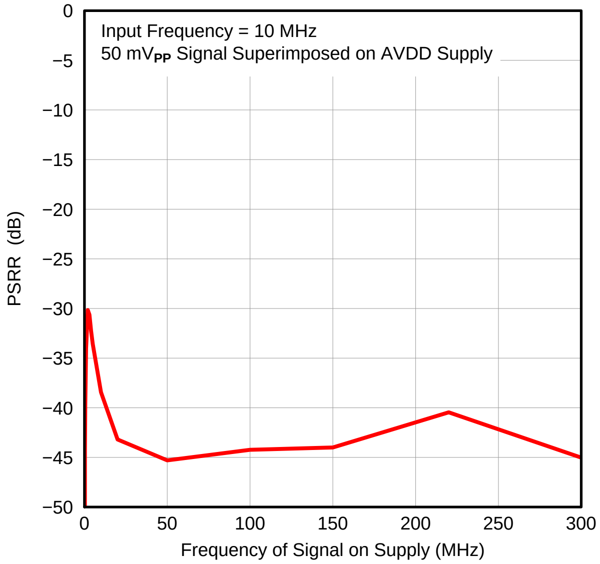

Figure 33.

ZOOMED VIEW of PSRR SPECTRUM

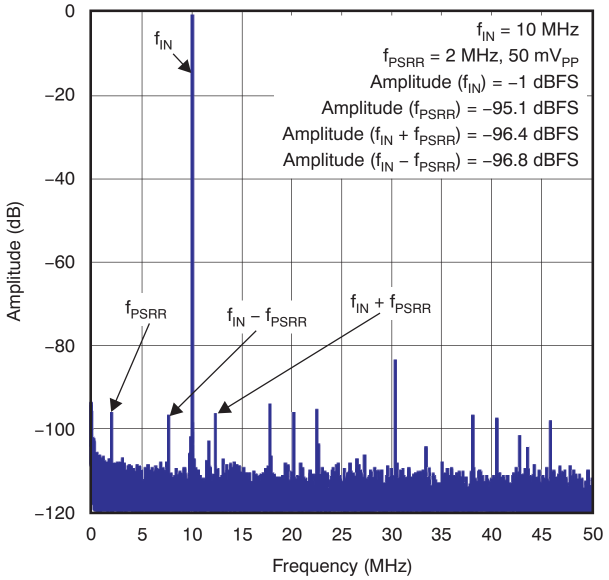

Figure 34.

ANALOG POWER vs SAMPLING FREQUENCY

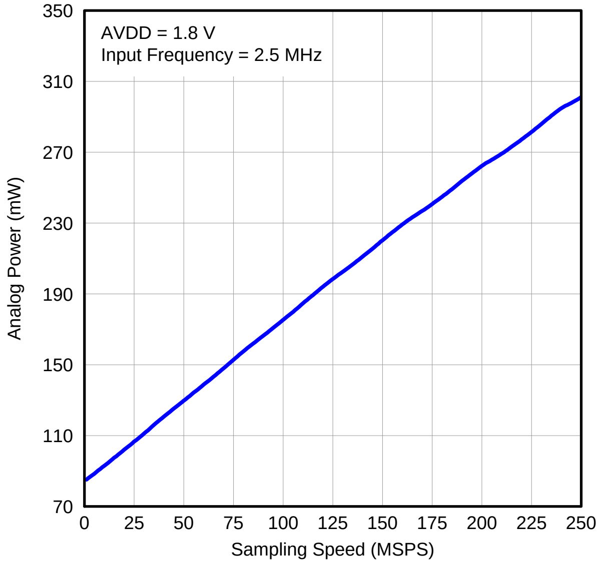

Figure 35.

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TYPICAL CHARACTERISTICS: ADS4249 (continued)

At T_A = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

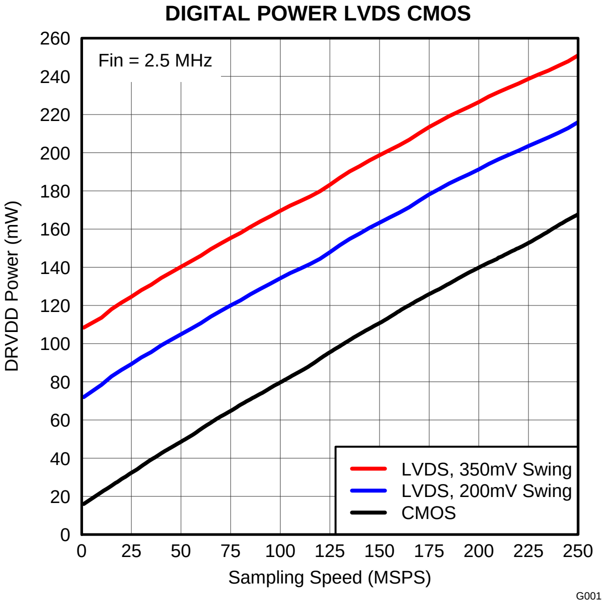

Figure 36.

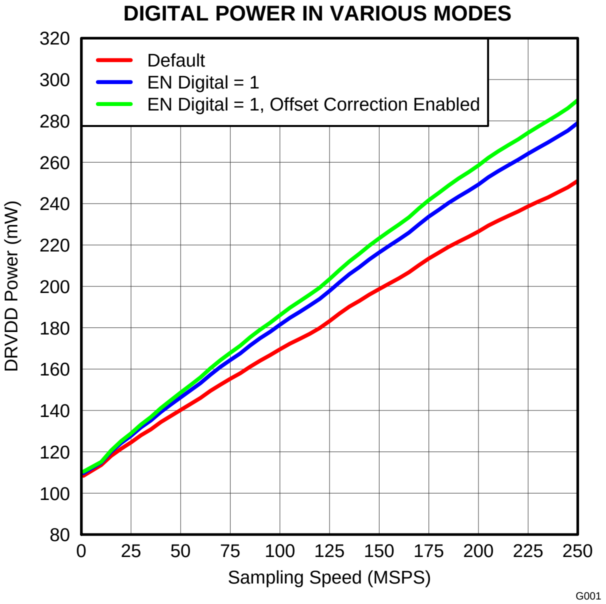

Figure 37.

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TYPICAL CHARACTERISTICS: Contour

All graphs are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

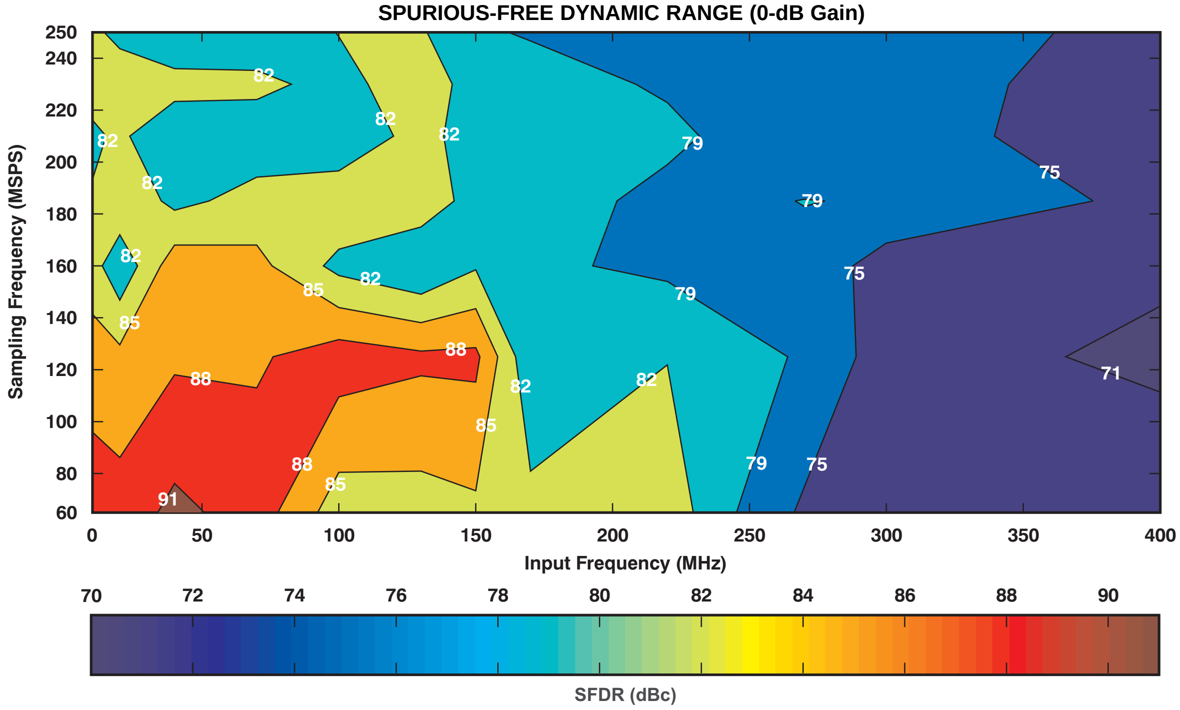

Figure 38.

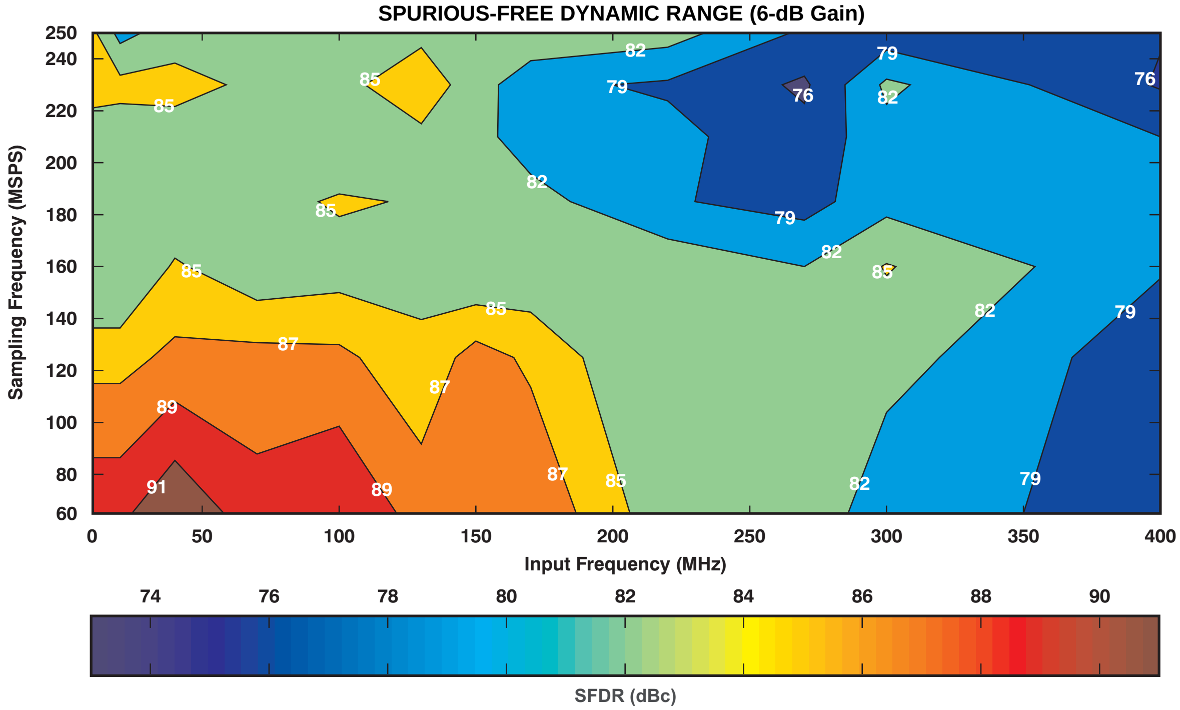

Figure 39.

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TYPICAL CHARACTERISTICS: Contour (continued)

All graphs are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

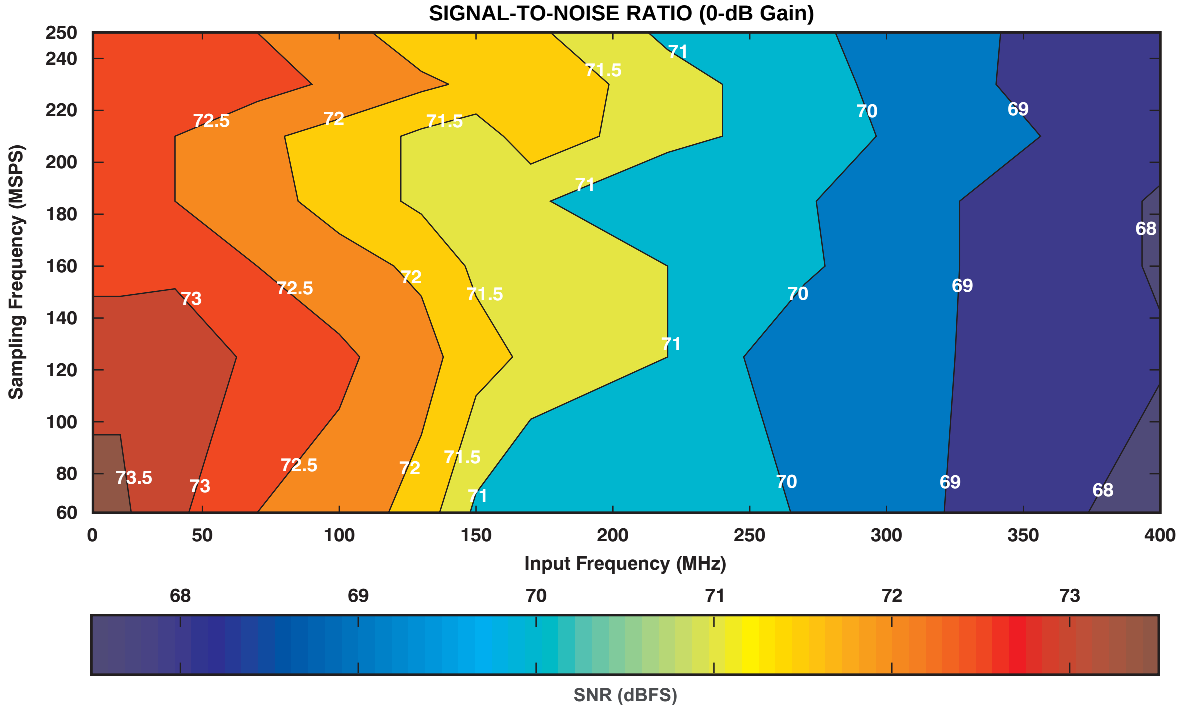
SIGNAL-TO-NOISE RATIO (0-dB Gain)

Figure 40.

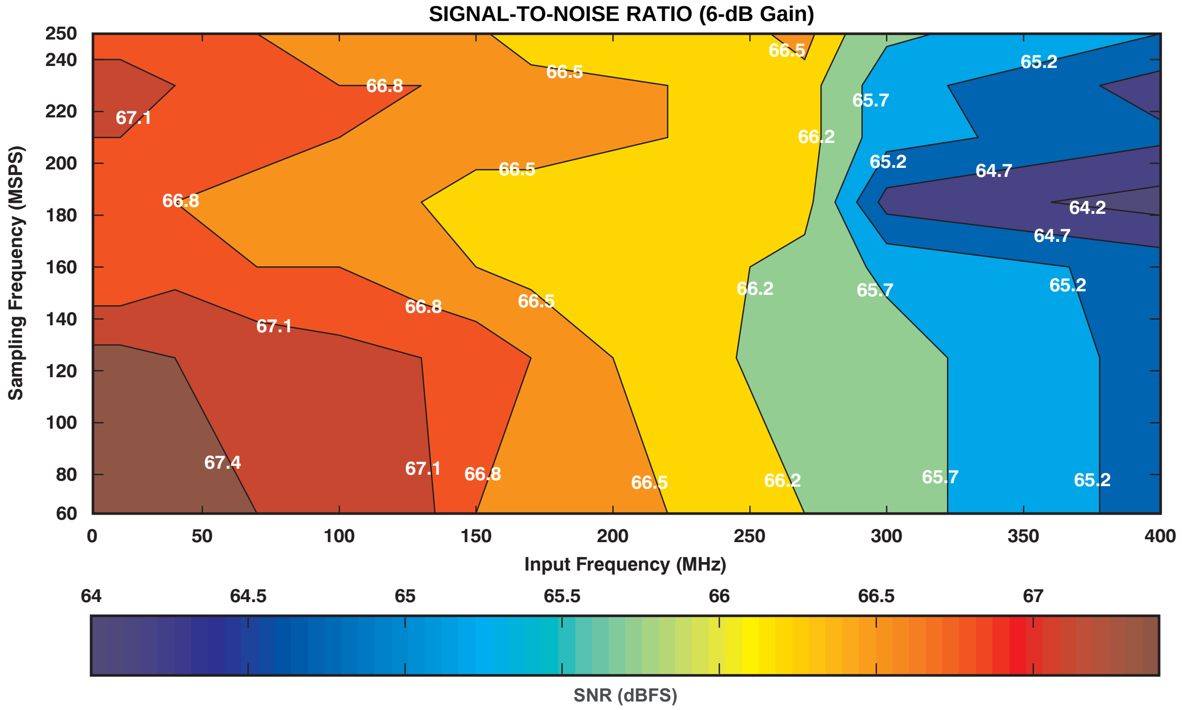
SIGNAL-TO-NOISE RATIO (6-dB Gain)

Figure 41.

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APPLICATION INFORMATION

THEORY OF OPERATION

The ADS4249 belongs to TI's ultralow-power family of dual-channel, 12-/14-bit analog-to-digital converters (ADCs). At every rising edge of the input clock, the analog input signal of each channel is simultaneously sampled. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled/held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference between the stage input and the quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and digitally processed to create the final code after a data latency of 16 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary twos complement format. The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to approximately 400 MHz (with 2-V_{PP} amplitude) or approximately 600 MHz (with 1-V_{PP} amplitude).

ANALOG INPUT

The analog input consists of a switched-capacitor-based, differential sample-and-hold (S/H) architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). Figure 42 shows an equivalent circuit for the analog input.

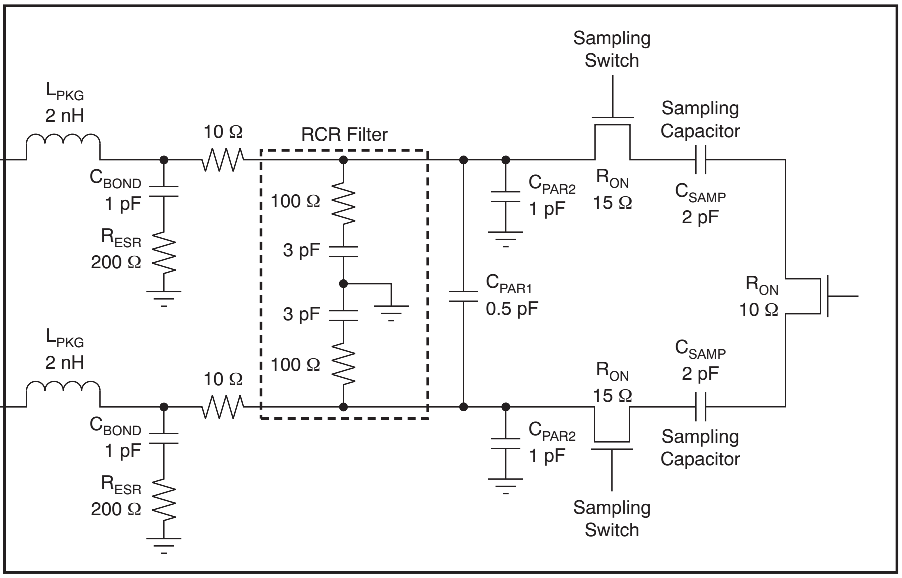

Figure 42. Analog Input Equivalent Circuit

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Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This operation improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics.

SFDR performance can be limited as a result of several reasons, including the effects of sampling glitches; nonlinearity of the sampling circuit; and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these factors generally plays a dominant part in limiting performance. At very high input frequencies (greater than approximately 300 MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, glitches could limit performance, primarily at low input frequencies (up to approximately 200 MHz). It is also necessary to present low impedance (less than 50 Ω) for the common-mode switching currents. This configuration can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM pin).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches must then be supplied by the external drive circuit. This tradeoff has limitations as a result of the presence of the package bond-wire inductance.

In the ADS4249, the R-C component values have been optimized while supporting high input bandwidth (up to 550 MHz). However, in applications with input frequencies up to 200 MHz to 300 MHz, the filtering of the glitches can be improved further using an external R-C-R filter; see Figure 45 and Figure 46.

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. Furthermore, the ADC input impedance must be considered. Figure 43 and Figure 44 show the impedance ($Z_{IN} = R_{IN} \| C_{IN}$) looking into the ADC input pins.

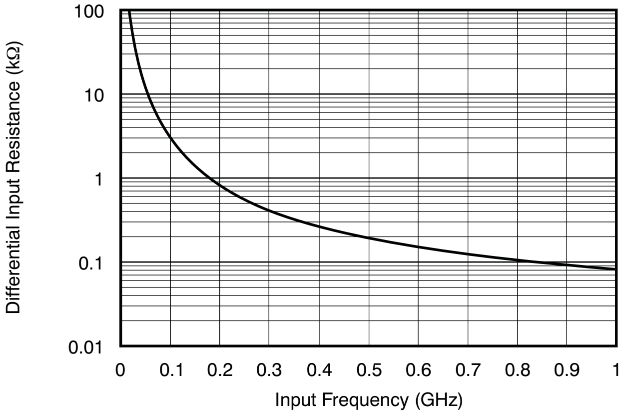

Figure 43. ADC Analog Input Resistance (R_{IN}) Across Frequency

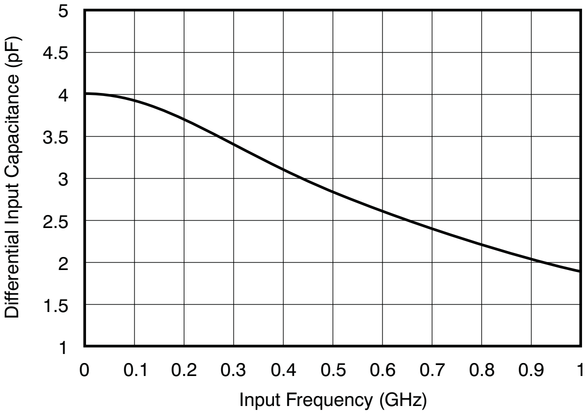

Figure 44. ADC Analog Input Capacitance (C_{IN}) Across Frequency

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Driving Circuit

Three example driving circuit configurations are shown in Figure 45, Figure 46, and Figure 47. They are optimized for low bandwidth (low input frequencies), high bandwidth (higher input frequencies), and very high bandwidth (very high input frequencies), respectively. Note that three of the drive circuits have been terminated by 50 Ω near the ADC side. The termination is accomplished by a 25-Ω resistor from each input to the 0.95-V common-mode (VCM) from the device. This architecture allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch; good performance is obtained for high-frequency input signals. For example, ADT1-1WT transformers can be used for the first two configurations (Figure 45 and Figure 46) while ADTL2-18 transformers can be used for the third configuration (Figure 47). An optional termination resistor pair may be required between the two transformers, as shown in Figure 45, Figure 46, and Figure 47. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (in the case of 50-Ω source impedance).

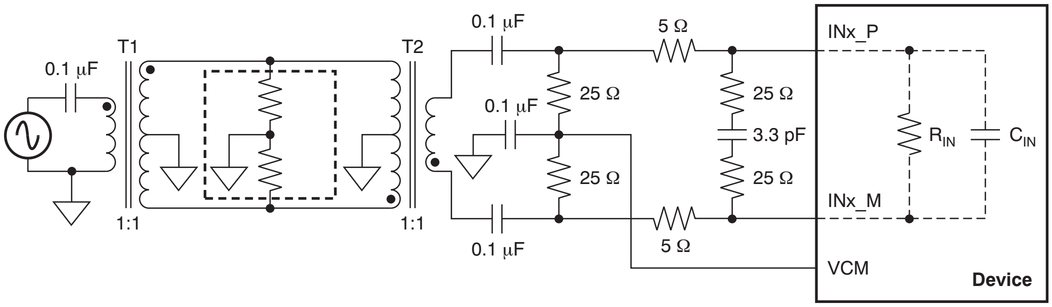

Figure 45. Drive Circuit with Low Bandwidth (for Low Input Frequencies Less Than 150 MHz)

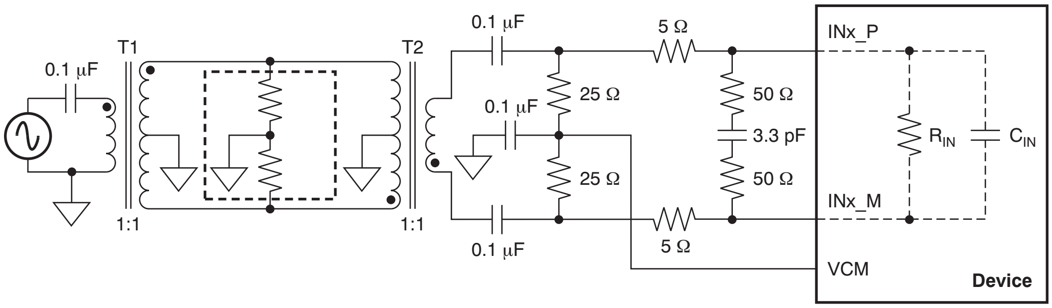

Figure 46. Drive Circuit with High Bandwidth (for High Input Frequencies Greater Than 150 MHz and Less Than 270 MHz)

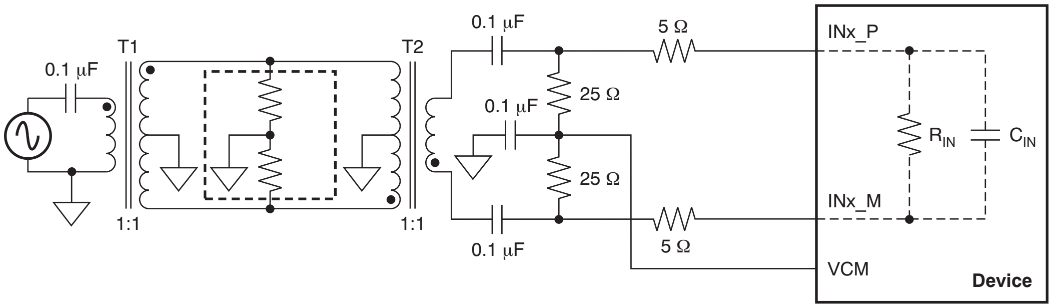

Figure 47. Drive Circuit with Very High Bandwidth (Greater than 270 MHz)

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All of these examples show 1:1 transformers being used with a 50-Ω source. As explained in the *Drive Circuit Requirements* section, this configuration helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is 200 Ω. The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

In almost all cases, either a band-pass or low-pass filter is required to obtain the desired dynamic performance, as shown in Figure 48. Such filters present low source impedance at the high frequencies corresponding to the sampling glitch and help avoid performance losses associated with the high source impedance.

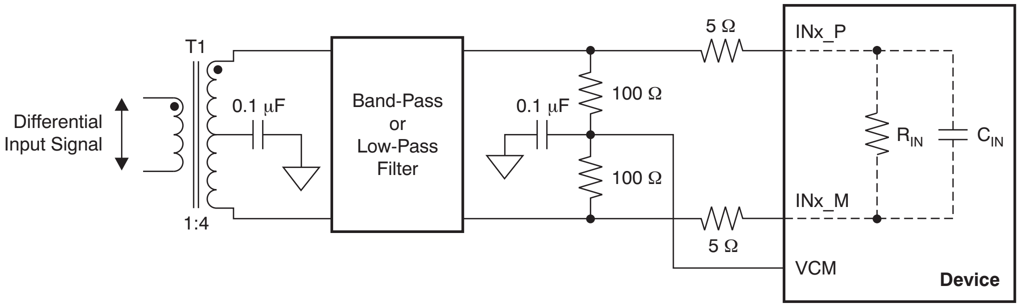

Figure 48. Drive Circuit with a 1:4 Transformer

CLOCK INPUT

The ADS4249 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources are shown in Figure 49, Figure 50 and Figure 51. The internal clock buffer is shown in Figure 52.

(1) R_T = termination resister, if necessary.

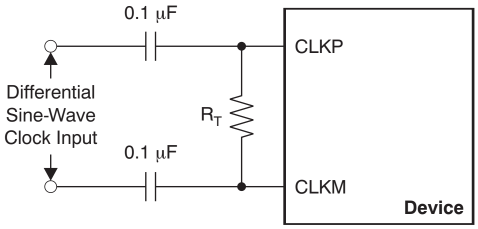

Figure 49. Differential Sine-Wave Clock Driving Circuit

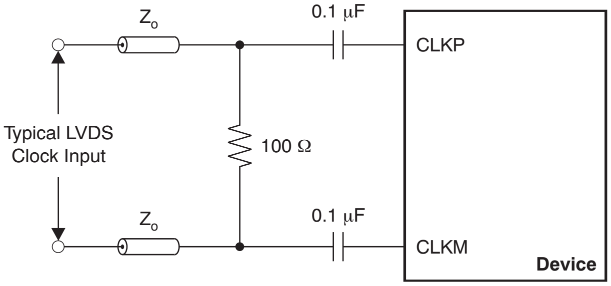

Figure 50. LVDS Clock Driving Circuit

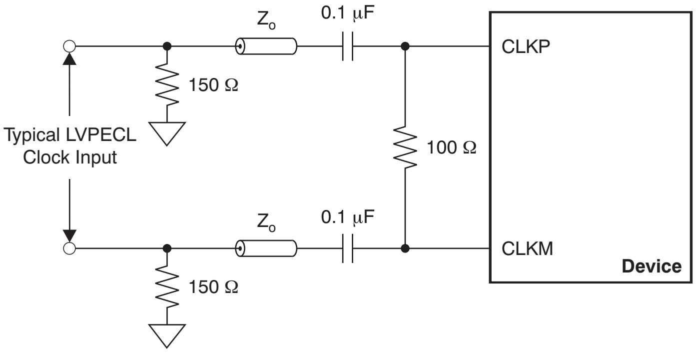

Figure 51. LVPECL Clock Driving Circuit

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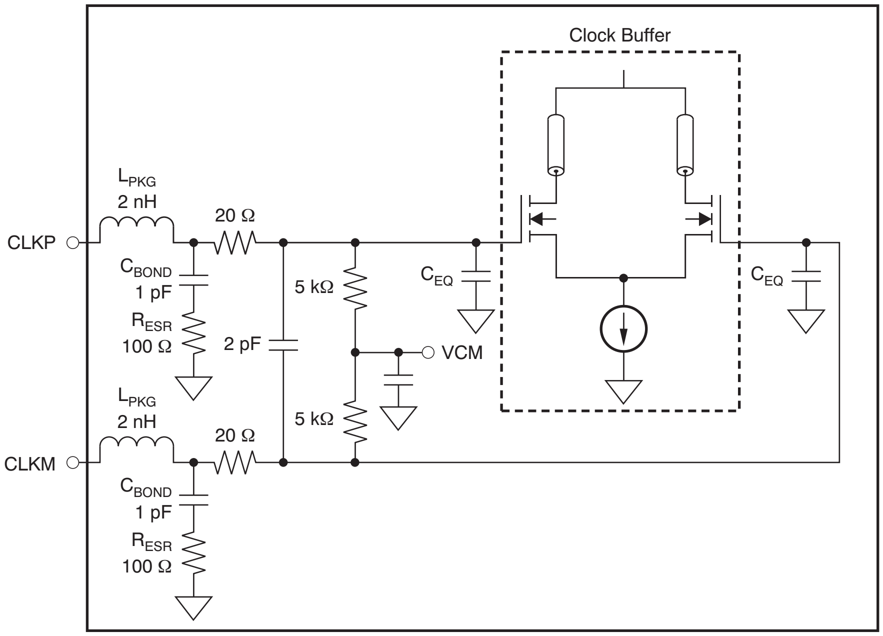

NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 52. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-μF capacitor, as shown in Figure 53. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

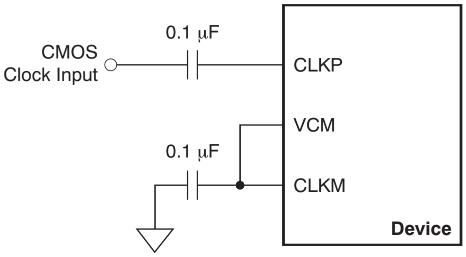

Figure 53. Single-Ended Clock Driving Circuit

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DIGITAL FUNCTIONS

The device has several useful digital functions (such as test patterns, gain, and offset correction). These functions require extra clock cycles for operation and increase the overall latency and power of the device. These digital functions are disabled by default after reset and the raw ADC output is routed to the output data pins with a latency of 16 clock cycles. Figure 54 shows more details of the processing after the ADC. In order to use any of the digital functions, the EN DIGITAL bit must be set to '1'. After this, the respective register bits must be programmed as described in the following sections and in the *Serial Register Map* section.

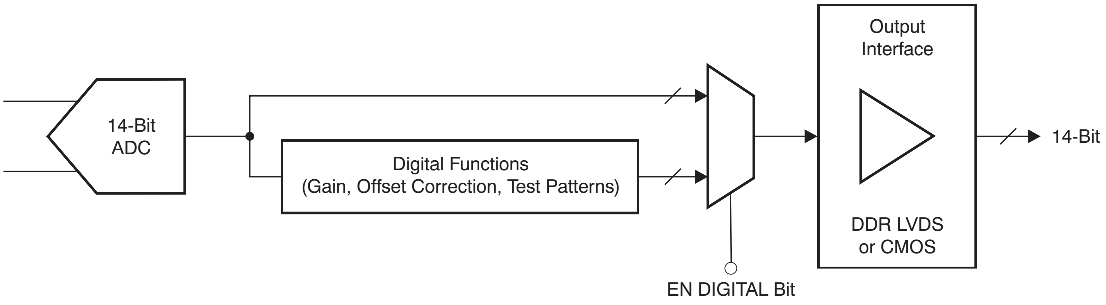

Figure 54. Digital Processing Block

GAIN FOR SFDR/SNR TRADE-OFF

The ADS4249 includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 12.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 12. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	2
1	Fine, programmable	1.78
2	Fine, programmable	1.59
3	Fine, programmable	1.42
4	Fine, programmable	1.26
5	Fine, programmable	1.12
6	Fine, programmable	1

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OFFSET CORRECTION

The ADS4249 has an internal offset corretion algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 13.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 0. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

Table 13. Time Constant of Offset Correction Algorithm

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (ms)(1)
0000	1 M	4
0001	2 M	8
0010	4 M	16
0011	8 M	32
0100	16 M	64
0101	32 M	128
0110	64 M	256
0111	128 M	512
1000	256 M	1024
1001	512 M	2048
1010	1 G	4096
1011	2 G	8192
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 250 MSPS.

POWER-DOWN

The ADS4249 has two power-down modes: global power-down and channel standby. These modes can be set using either the serial register bits or using the control pins CTRL1 to CTRL3 (as shown in Table 14).

Table 14. Power-Down Settings

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Default
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Global power-down
High	Low	High	Channel A powered down, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data is multiplexed and output on DB[13:0] pins

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Global Power-Down

In this mode, the entire chip (including ADCs, internal reference, and output buffers) are powered down, resulting in reduced total power dissipation of approximately 20 mW when the CTRL pins are used and 3mW when the PDN GLOBAL serial register bit is used. The output buffers are in high-impedance state. The wake-up time from global power-down to data becoming valid in normal mode is typically 100 µs.

Channel Standby

In this mode, each ADC channel can be powered down. The internal references are active, resulting in a quick wake-up time of 50 µs. The total power dissipation in standby is approximately 240 mW at 250 MSPS.

Input Clock Stop

In addition to the previous modes, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 160 mW.

DIGITAL OUTPUT INFORMATION

The ADS4249 provides 14-bit digital data for each channel and an output clock synchronized with the data.

Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit or by setting the proper voltage on the SEN pin in parallel configuration mode.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 55.

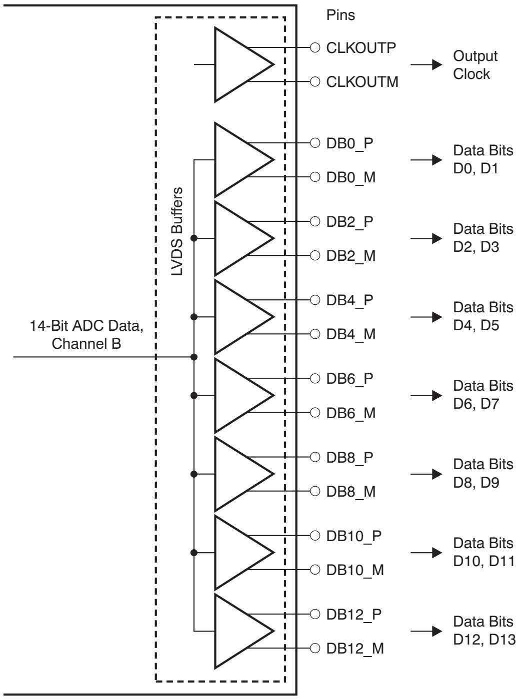

Figure 55. LVDS Interface

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Even data bits (D0, D2, D4, etc.) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, etc.) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in Figure 56.

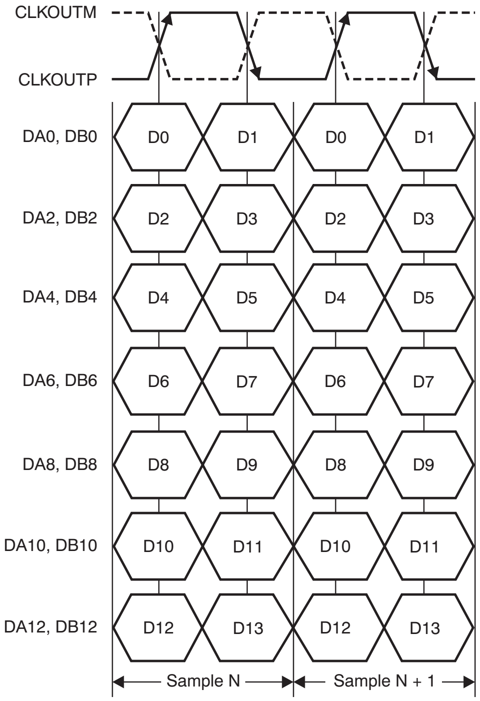
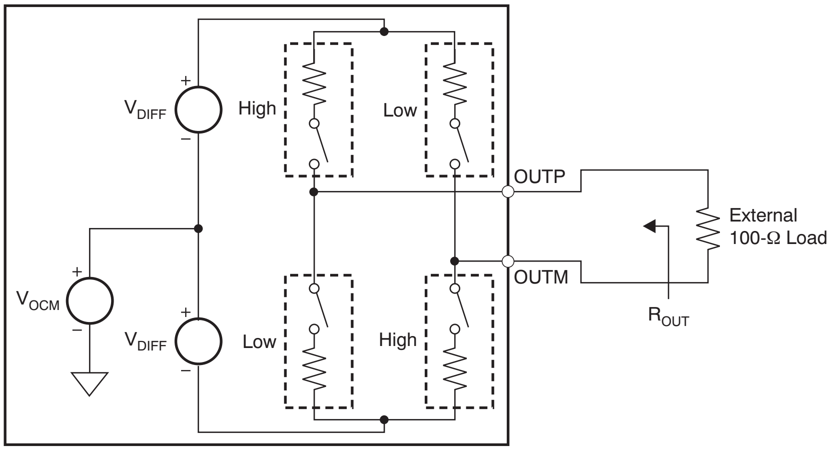


Figure 56. DDR LVDS Interface Timing

LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 57. After reset, the buffer presents an output impedance of 100Ω to match with the external 100-Ω termination.



NOTE: Default swing across 100-Ω load is ±350 mV. Use the LVDS SWING bits to change the swing.

Figure 57. LVDS Buffer Equivalent Circuit

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The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination, as shown in Figure 58. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

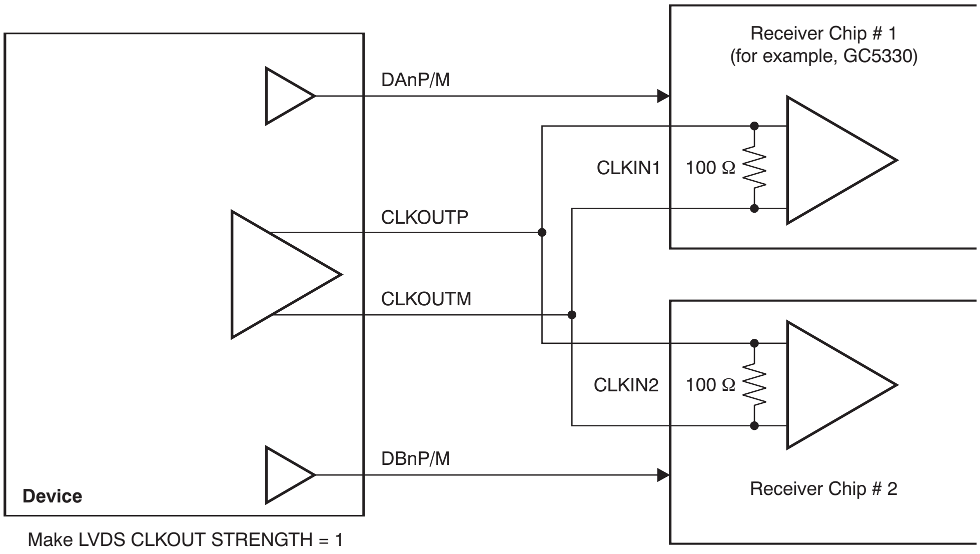

Figure 58. LVDS Buffer Differential Termination

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Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle, as Figure 59 shows. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. It is recommended to minimize the load capacitance of the data and clock output pins by using short traces to the receiver. Furthermore, match the output data and clock traces to minimize the skew between them.

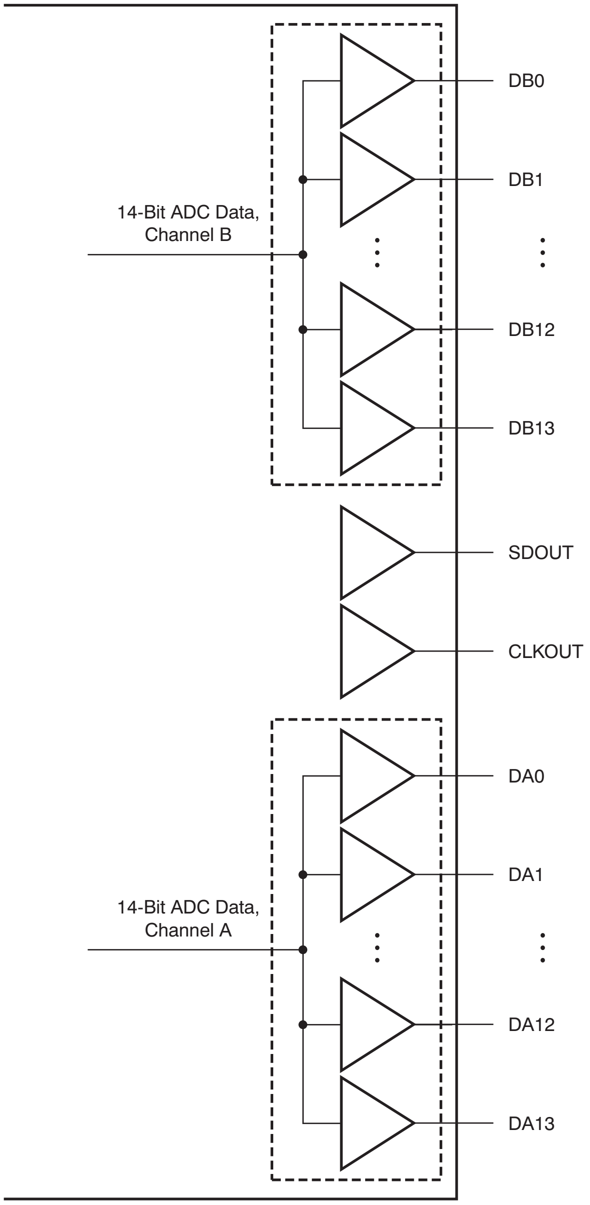

Figure 59. CMOS Outputs

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CMOS Interface Power Dissipation

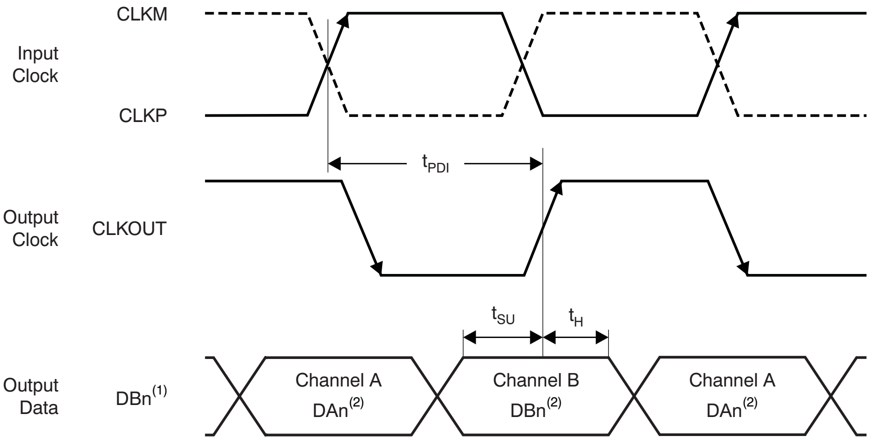
With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal. This relationship is shown by the formula:

Digital current as a result of CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$,

where C_L = load capacitance, $N \times F_{AVG}$ = average number of output bits switching.

Multiplexed Mode of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DB[11:0] pins), as shown in Figure 60. The channel A output pins (DA[11:0]) are in 3-state. Because the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 80 MSPS). This mode can be enabled using the POWER-DOWN MODE register bits or using the CTRL[3:1] parallel pins.



(1) In multiplexed mode, both channels outputs come on the channel B output pins.

(2) Dn = bits D0, D1, D2, etc.

Figure 60. Multiplexed Mode Timing Diagram

Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit or by controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 3FFFh for the ADS4249 in offset binary output format; the output code is 1FFFh for the ADS4249 in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 2000h for the ADS4249 in twos complement output format.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

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Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy (E_{GREF}) and error as a result of the channel (E_{GCHAN}). Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$\mathrm{SNR} = 10\mathrm{Log}^{10} \frac{P_S}{P_N} \tag{1}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$\mathrm{SINAD} = 10\mathrm{Log}^{10} \frac{P_S}{P_N + P_D} \tag{2}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

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Effective Number of Bits (ENOB) – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (3)$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10} \frac{P_S}{P_N} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \quad \text{(Expressed in dBc)} \quad (5)$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \quad \text{(Expressed in dBc)} \quad (6)$$

Crosstalk (only for multi-channel ADCs) – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

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BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS4226 Evaluation Module* (SLAU333) for details on layout and grounding.

Supply Decoupling

Because the ADS4249 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically connected internally to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

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Routing Analog Inputs

It is advisable to route differential analog input pairs (INP_x and INM_x) close to each other. To minimize the possibility of coupling from a channel analog input to the sampling clock, the analog input pairs of both channels should be routed perpendicular to the sampling clock; see the *ADS4226 Evaluation Module* (SLAU333) for reference routing. Figure 61 shows a snapshot of the PCB layout from the ADS42xxEVM.

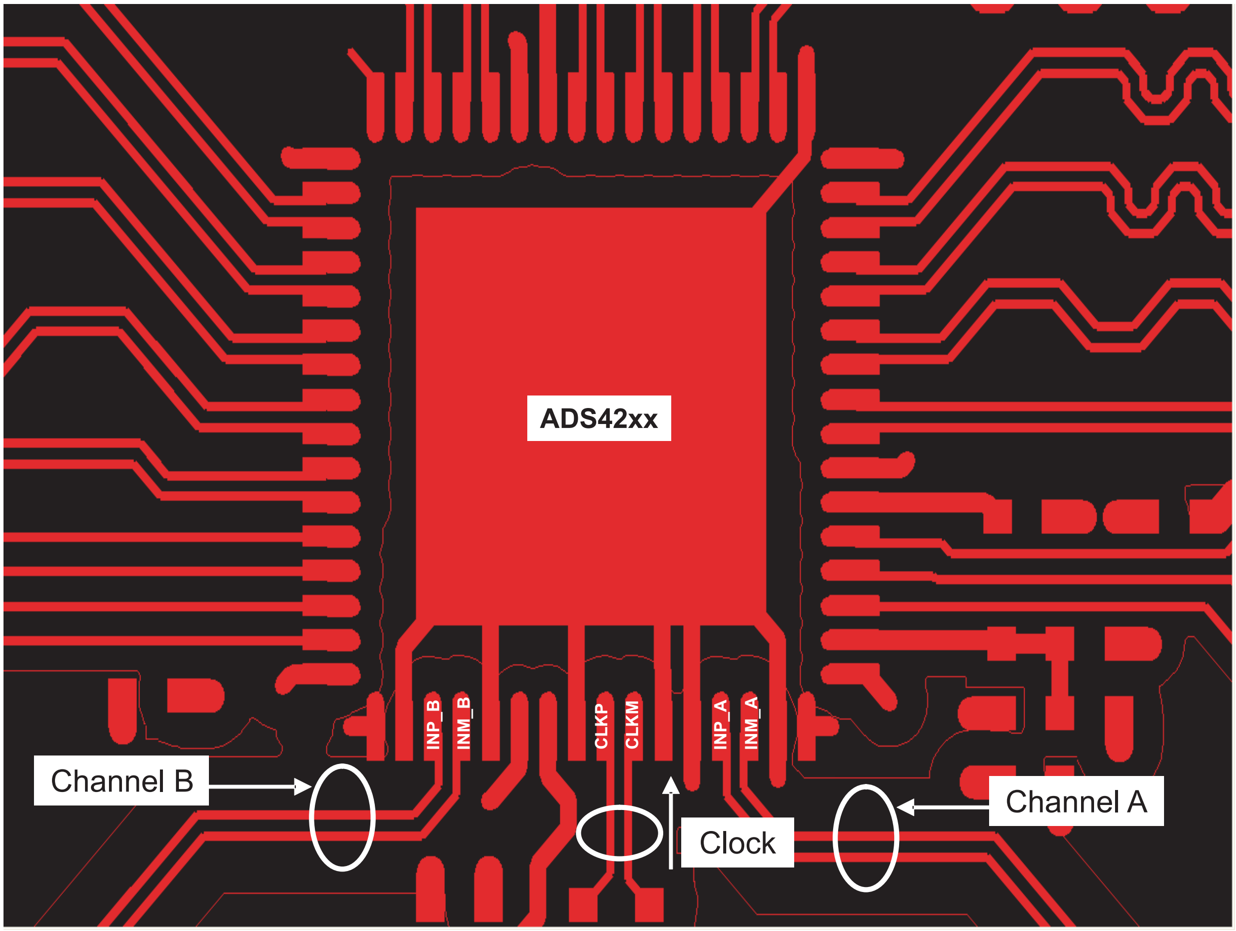

Figure 61. ADS42xxEVM PCB Layout

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2011) to Revision C **Page**

Changes from Revision A (September 2011) to Revision B **Page**

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
ADS4249IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS4249IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS4249IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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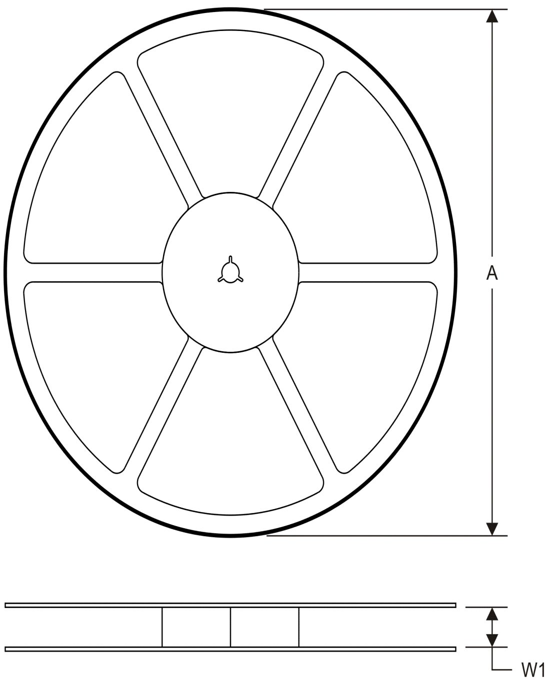
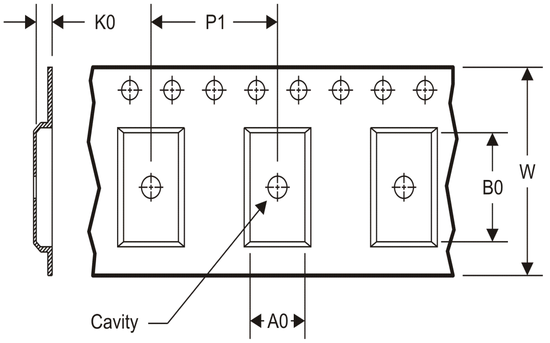
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS4249IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS4249IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

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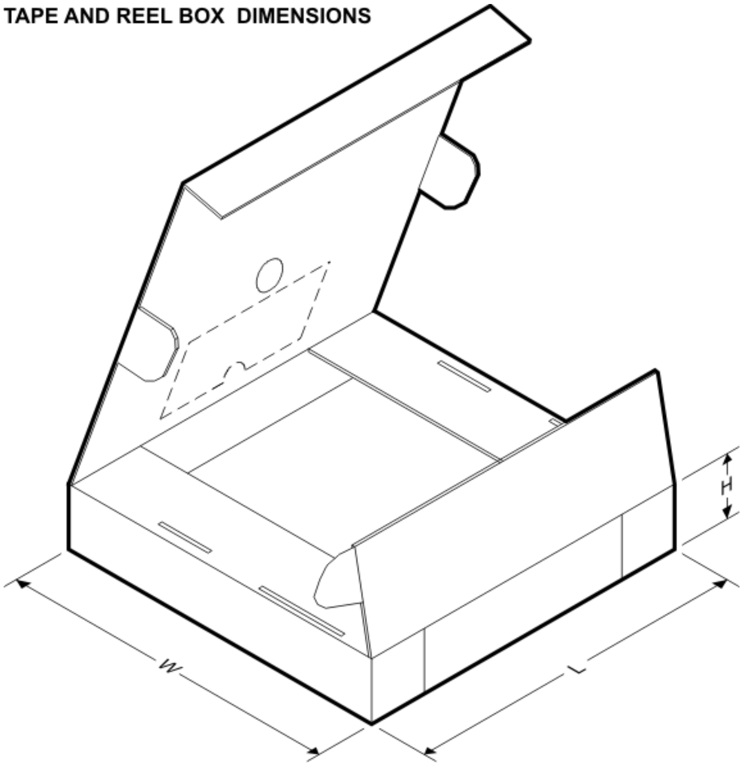
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS4249IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS4249IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

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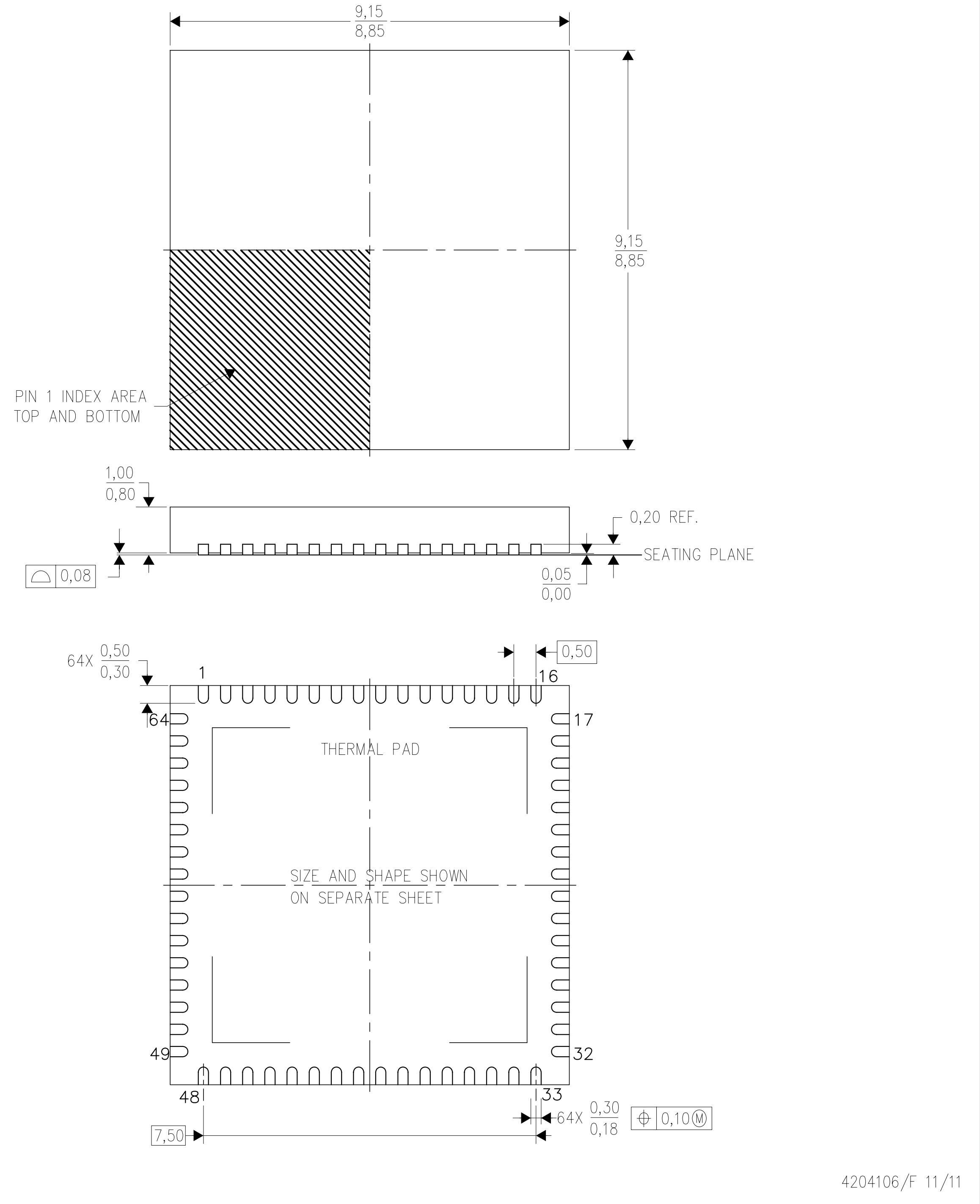
RGC(S–PVQFN–N64)   CUSTOM DEVICE   PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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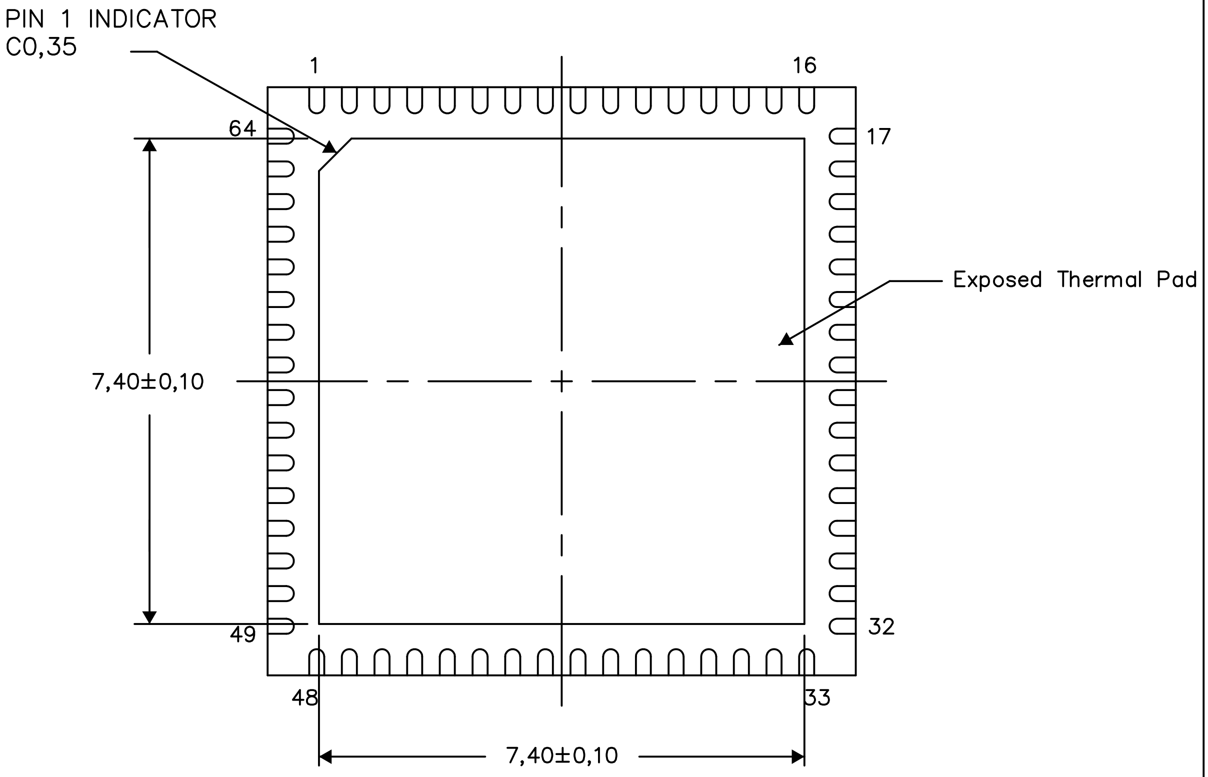
RGC (S-PVQFN-N64) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206192-4/S 06/12

NOTE: A. All linear dimensions are in millimeters

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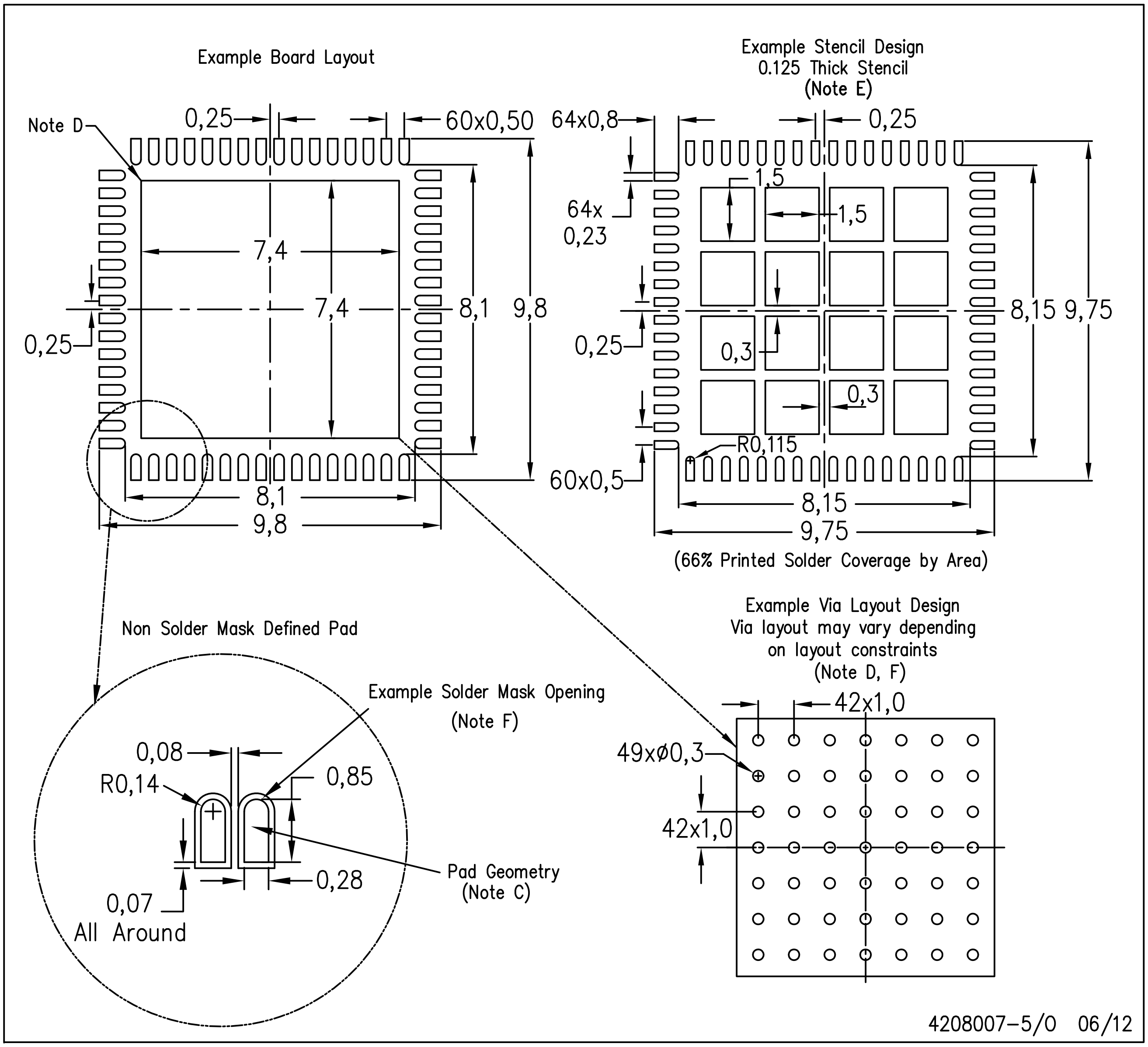
RGC (S-PVQFN-N64) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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