1/3-Inch CMOS Digital Image Sensor

MT9M031 Advance Data Sheet

For the latest data sheet revision, refer to Aptina's Web site:www.aptina.com

Features

- Superior low-light performance
- HD video (720p60)
- Global shutter
- Video/Single Frame mode
- Flexible row-skip modes
- On-chip AE and statistics engine
- Parallel and serial output
- Support for external LED or flash
- Auto black level calibration
- Context switching

Applications

- Scene processing
- Scanning and machine vision
- 720p60 video applications

General Description

Aptina's MT9M031 is a 1/3-inch CMOS digital image sensor with an active-pixel array of 1280H x 960V. It includes sophisticated camera functions such as auto exposure control, windowing, scaling, row skip mode, and both video and single frame modes. It is designed for low light performance and features a global shutter for accurate capture of moving scenes. It is programmable through a simple two-wire serial interface. The MT9M031 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including scanning and HD video.

Table 1: Key Parameters

Parameter		Typical Value
Optical format		1/3-inch (6 mm)
Active pixels		1280 x 960 = 1.2 Mp
Pixel size		3.75µm
Color filter array		RGB Bayer or Monochrome
Shutter type		Global shutter
Input clock range		6 – 50 MHz
Output pixel clock (maximum)		74.25 MHz
Output	Serial	HiSPi
	Parallel	12-bit

Table 1: Key Parameters (continued)

Parameter		Typical Value
Frame rate	Full resolution	45 fps
	720p	60 fps
Responsivity (Monochrome)		8.5V/lux-sec
SNR_{MAX}		40 dB
Dynamic range		61.3 dB
Supply voltage	I/O	1.8 or 2.8 V
	Digital	1.8 V
	Analog	2.8 V
	HiSPi	0.4 V
Power consumption		<400 mW
Operating temperature (ambient)		–30°C to +70°C
Package options		10 x 10 mm 48 iLCC
		Bare die

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9M031I12STC ES Color	iLCC Engineering Samples
MT9M031I12STC Color	iLCC Production
MT9M031I12STM ES Mono	iLCC Engineering Samples
MT9M031I12STM Mono	iLCC Production
MT9M031I12STCV ES Color	HiSPi, iLCC Engineering Samples
MT9M031I12STCV Color	HiSPi, iLCC Production
MT9M031I12STMV ES Mono	HiSPi, iLCC Engineering Samples
MT9M031I12STMV Mono	HiSPi ,iLCC Production
MT9M031I12STCD ES Color	Demo Kit Engineering Samples
MT9M031I12STMD ES Mono	Demo Kit Engineering Samples
MT9M031I12STCH ES Color	Head Board Engineering Samples
MT9M031I12STMH ES Mono	Head Board Engineering Samples
MT9M031I12STCVD ES Color	HiSPi, Demo Kit Engineering Samples
MT9M031I12STMVD ES Mono	HiSPi, Demo Kit Engineering Samples
MT9M031I12STCVH ES Color	HiSPi, Head Board Engineering Samples
MT9M031I12STMVH ES Mono	HiSPi, Head Board Engineering Samples

Table of Contents

List of Figures

List of Tables

General Description

The Aptina® MT9M031 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a full-resolution image at 45 frames per second (fps). It outputs 12-bit raw data, using either the parallel or serial (HiSPi) output ports. The device may be operated in video (master) mode or in frame trigger mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock. A dedicated FLASH pin can be programmed to control external LED or flash exposure illumination.

The MT9M031 includes additional features to allow application-specific tuning: windowing, adjustable auto-exposure control, auto black level correction, optional defective pixel correction, on-board temperature sensor, and row skip and digital binning modes.

The sensor is designed to operate in a wide temperature range (–30°C to +70°C).

Figure 1: Block Diagram

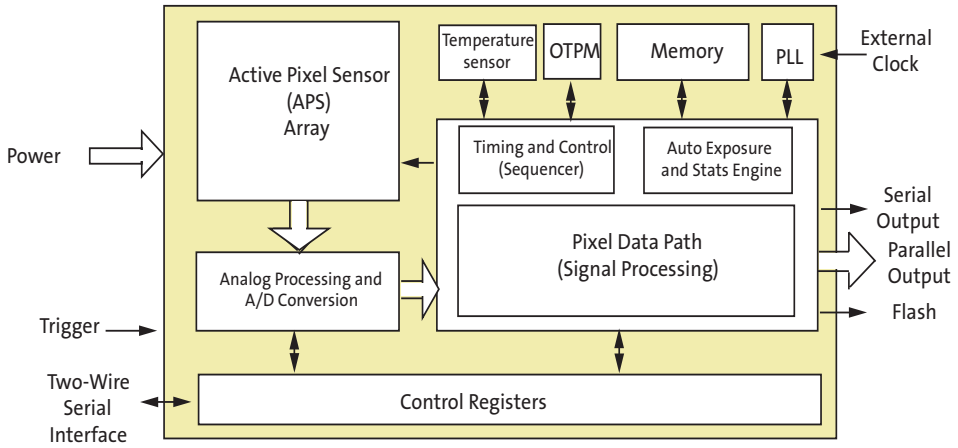


Figure 2: 48 iLCC Package, Parallel Output

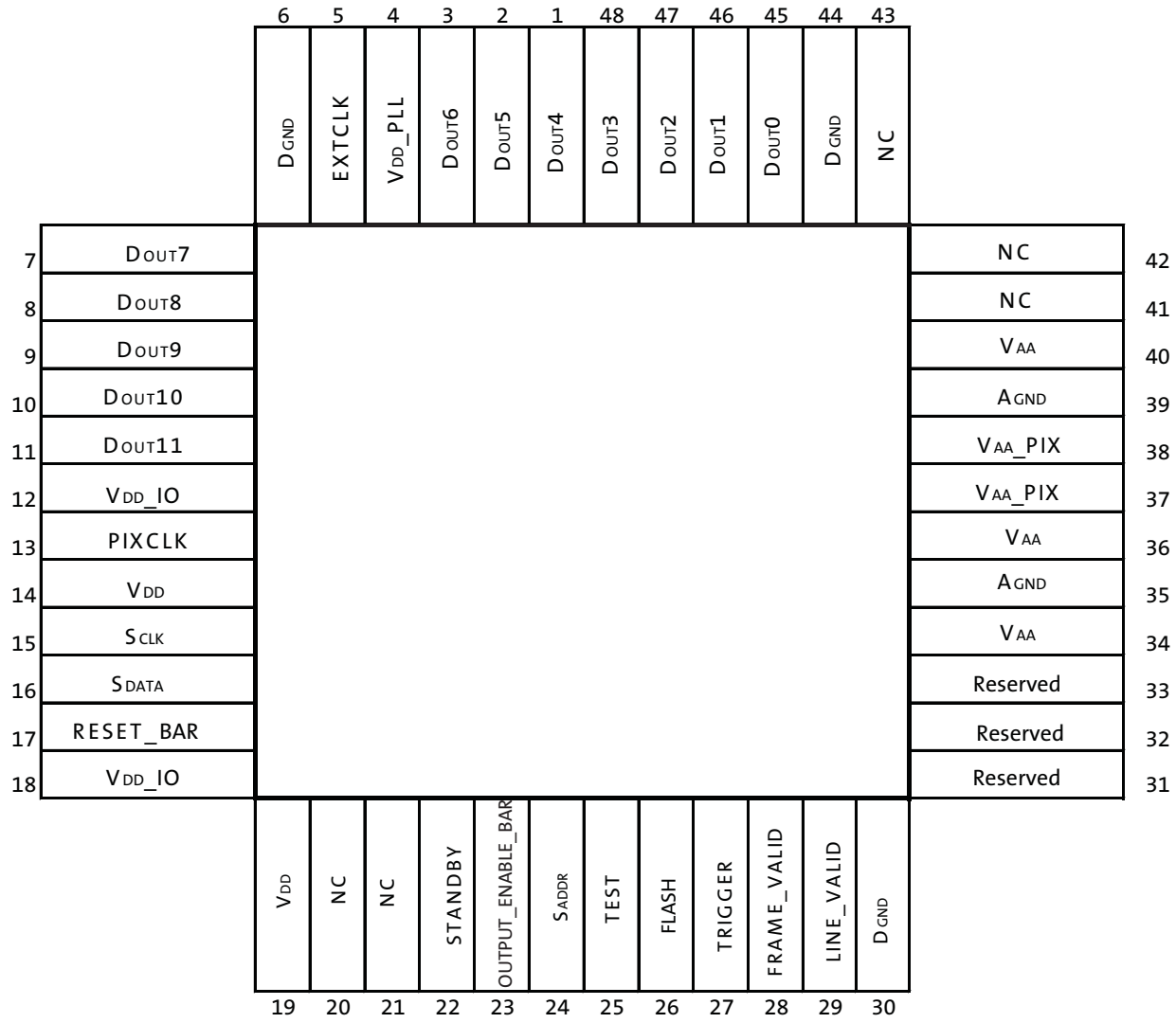


Table 3: Pin Descriptions

Pin Number	Name	Type	Description
1	DOUT4	Output	Parallel pixel data output.
2	DOUT5	Output	Parallel pixel data output.
3	DOUT6	Output	Parallel pixel data output.
4	VDD_PLL	Power	PLL power.
5	EXTCLK	Input	External input clock.
6	DGND	Power	Digital ground.
7	DOUT7	Output	Parallel pixel data output.
8	DOUT8	Output	Parallel pixel data output.
9	DOUT9	Output	Parallel pixel data output.
10	DOUT10	Output	Parallel pixel data output.
11	DOUT11	Output	Parallel pixel data output (MSB).
12	VDD_IO	Power	I/O supply power.
13	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.
14	VDD	Power	Digital power.
15	SCLK	Input	Two-Wire Serial clock input.
16	SDATA	I/O	Two-Wire Serial data I/O.
17	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
18	VDD_IO	Power	I/O supply power.
19	VDD	Power	Digital power.
20	NC		
21	NC		
22	STANDBY	Input	Standby-mode enable pin (active HIGH).
23	OUTPUT_ENABLE_BAR	Input	Output enable (active LOW).
24	SADDR	Input	Two-Wire Serial address select.
25	TEST	Input	Manufacturing test enable pin (connect to DGND).
26	FLASH	oUTPUT	Flash output control.
27	TRIGGER	Input	Exposure synchronization input.
28	FRAME_VALID	Output	Asserted when DOUT frame data is valid.
29	LINE_VALID	Output	Asserted when DOUT line data is valid.
30	DGND	Power	Digital ground
31	Reserved		
32	Reserved		
33	Reserved		
34	VAA	Power	Analog power.
35	AGND	Power	Analog ground.
36	VAA	Power	Analog power.
37	VAA_PIX	Power	Pixel power.
38	VAA_PIX	Power	Pixel power.
39	AGND	Power	Analog ground.
40	VAA	Power	Analog power.
41	NC		
42	NC		
43	NC		
44	DGND	Power	Digital ground.
45	DOUT0	Output	Parallel pixel data output (LSB)

Table 3: Pin Descriptions (continued)

Pin Number	Name	Type	Description
46	DOUT1	Output	Parallel pixel data output.
47	DOUT2	Output	Parallel pixel data output.
48	DOUT3	Output	Parallel pixel data output.

Figure 3: 48 iLCC Package, HiSPi Output

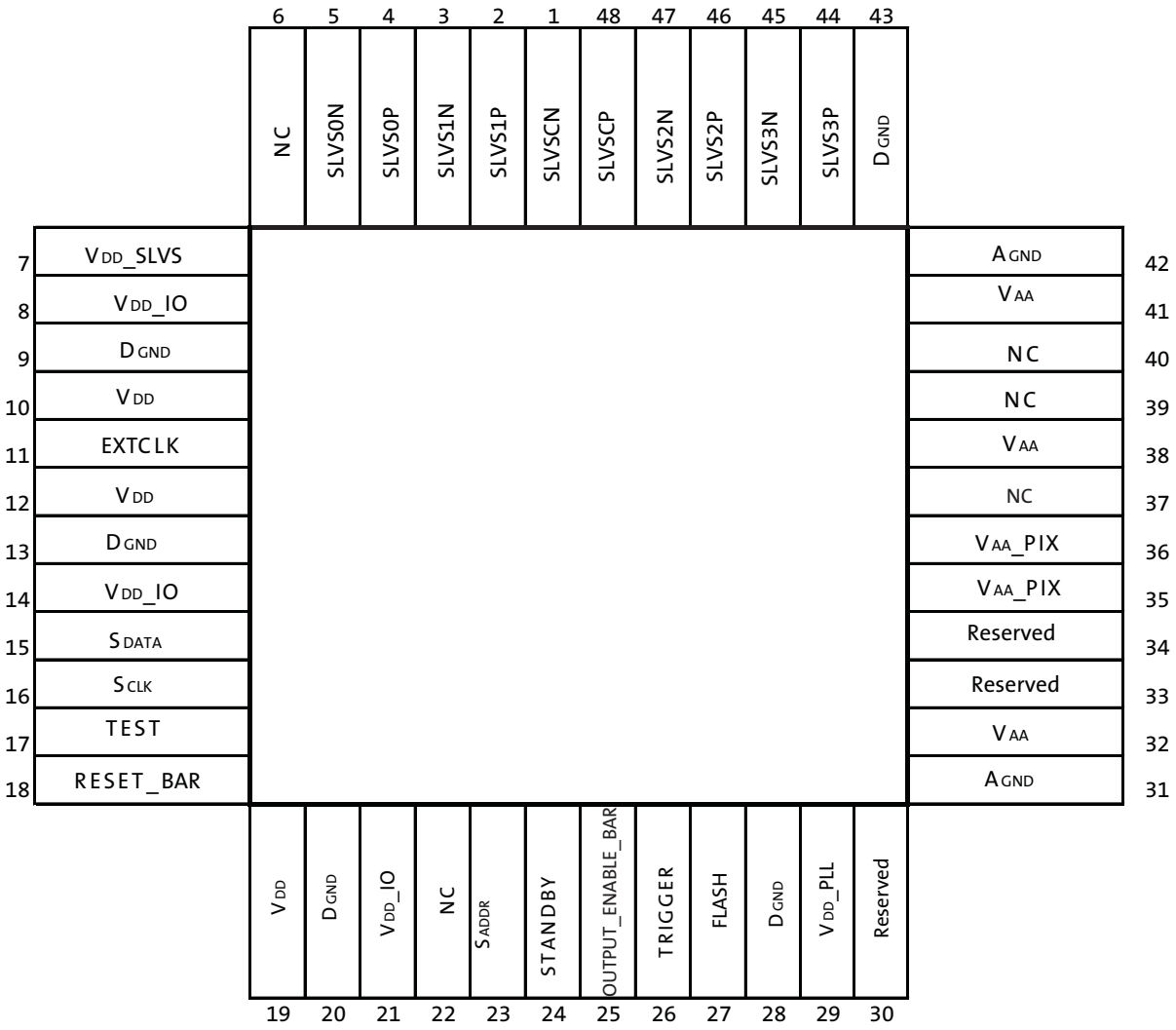


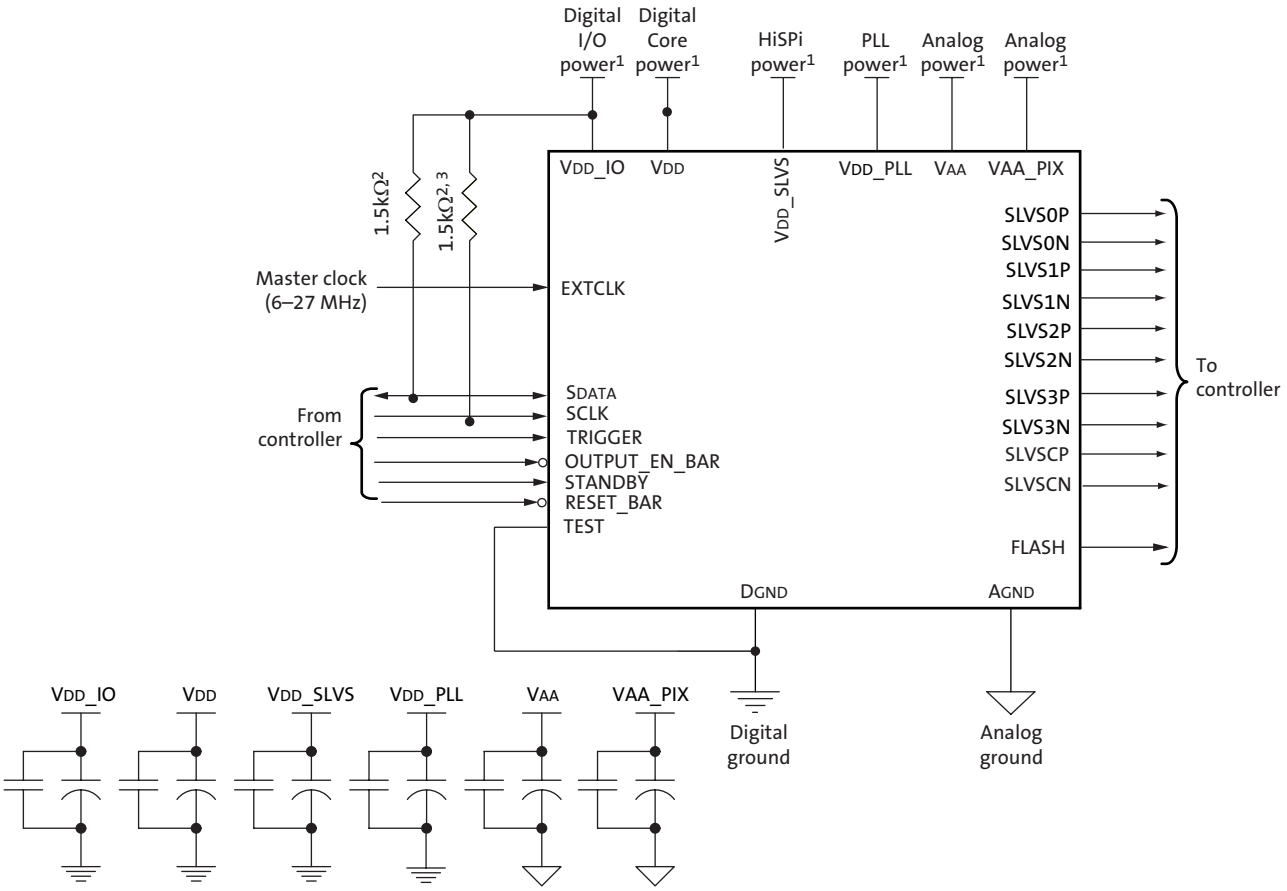
Table 4: Pin Descriptions, 48 iLCC

Pin Number	Name	Type	Description
1	SLVSCN	Output	HiSPi serial DDR clock differential N.
2	SLVS1P	Output	HiSPi serial data, lane 1, differential P.
3	SLVS1N	Output	HiSPi serial data, lane 1, differential N.
4	SLVS0P	Output	HiSPi serial data, lane 0, differential P.
5	SLVS0N	Output	HiSPi serial data, lane 0, differential N.
6	NC		
7	VDD_SLVS	Power	
8	VDD_IO	Power	I/O supply power.
9	DGND	Power	Digital ground.
10	VDD	Power	Digital power.
11	EXTCLK	Input	External input clock.
12	VDD	Power	Digital power.
13	DGND		Digital ground.
14	VDD_IO	Power	I/O supply power.
15	SDATA	I/O	Two-Wire Serial data I/O.
16	SCLK	Input	Two-Wire Serial clock input.
17	TEST		Manufacturing test enable pin (connect to DGND).
18	RESET_BAR	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
19	VDD	Power	Digital power.
20	DGND	Power	Digital ground.
21	VDD_IO	Power	I/O supply power.
22	NC		
23	SADDR	Input	Two-Wire Serial address select.
24	STANDBY	Input	Standby-mode enable pin (active HIGH).
25	OUTPUT_ENABLE_BAR		Output enable (active LOW).
26	TRIGGER	Input	Exposure synchronization input.
27	FLASH	Output	Flash output control.
28	DGND	Power	
29	VDD_PLL	Power	PLL power.
30	RESERVED		
31	AGND	Power	Analog ground.
32	VAA	Power	Analog power.
33	Reserved		
34	Reserved		
35	VAA_PIX	Power	Pixel power.
36	VAA_PIX	Power	Pixel power.
37	NC		
38	VAA	Power	Analog power.
39	NC		
40	NC		
41	VAA	Power	Analog power.
42	AGND	Power	Analog ground.
43	DGND	Power	Digital ground.
44	SLVS3P	Output	HiSPi serial data, lane 3, differential N.
45	SLVS3N	Output	HiSPi serial data, lane 3, differential P.

Table 4: Pin Descriptions, 48 iLCC (continued)

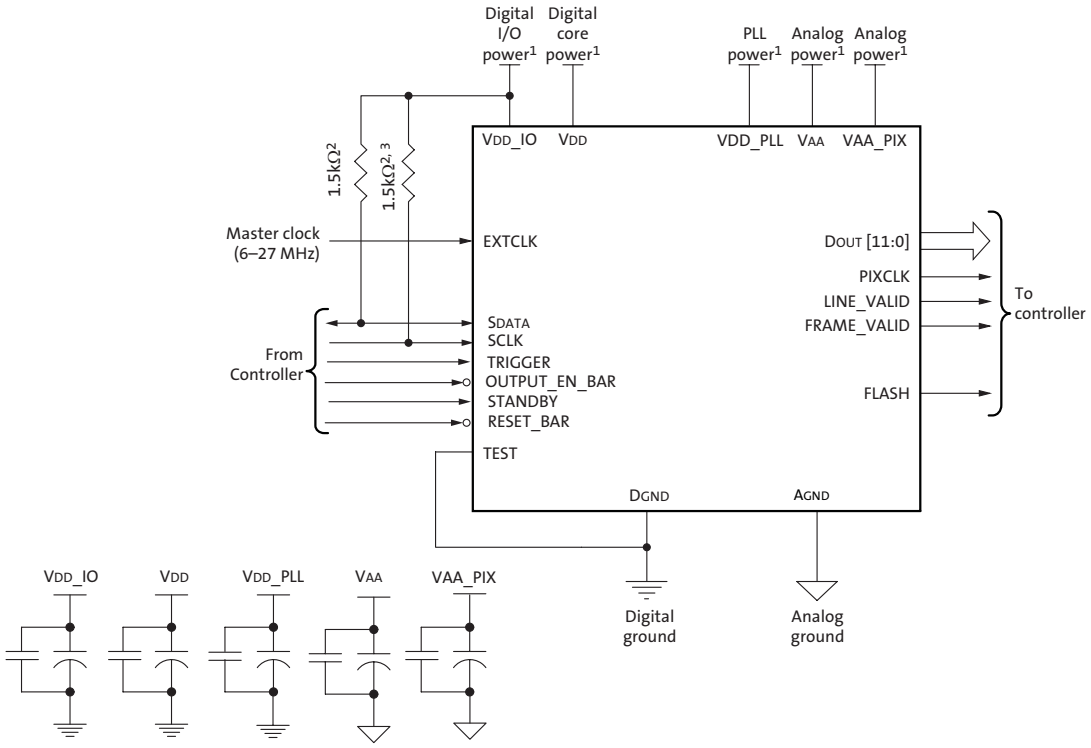
Pin Number	Name	Type	Description
46	SLVS2P	Output	HiSPi serial data, lane 2, differential P.
47	SLVS2N	Output	HiSPi serial data, lane 2, differential PN
48	SLVSCP	Output	HiSPi serial DDR clock differential P.

Figure 4: Typical Configuration: Serial Four-Lane HiSPi Interface



Notes:
1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. Aptina recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Check the MT9M031 demo headboard schematics for circuit recommendations.
6. Aptina recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.

Figure 5: Typical Configuration: Parallel Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. Aptina recommends a resistor value of 1.5kΩ, but it may be greater for slower two-wire speed.
3. This pull-up resistor is not required if the controller drives a valid logic level on SCLK at all times.
4. The serial interface output pads can be left unconnected if the parallel output interface is used.
5. Aptina recommends that 0.1µF and 10µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Check the MT9M031 demo headboard schematics for circuit recommendations.
6. Aptina recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.

Pixel Data Format

Pixel Array Structure

The MT9M031 pixel array is configured as 1412 columns by 1028 rows, (see Figure 6). The dark pixels are optically black and are used internally to monitor black level. Of the right 108 columns, 64 are dark pixels used for row noise correction. Of the top 24 rows of pixels, 12 of the dark rows are used for black level correction. There are 1296 columns by 976 rows of optically active pixels. While the sensor's format is 1280 x 960, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

Figure 6: Pixel Array Description

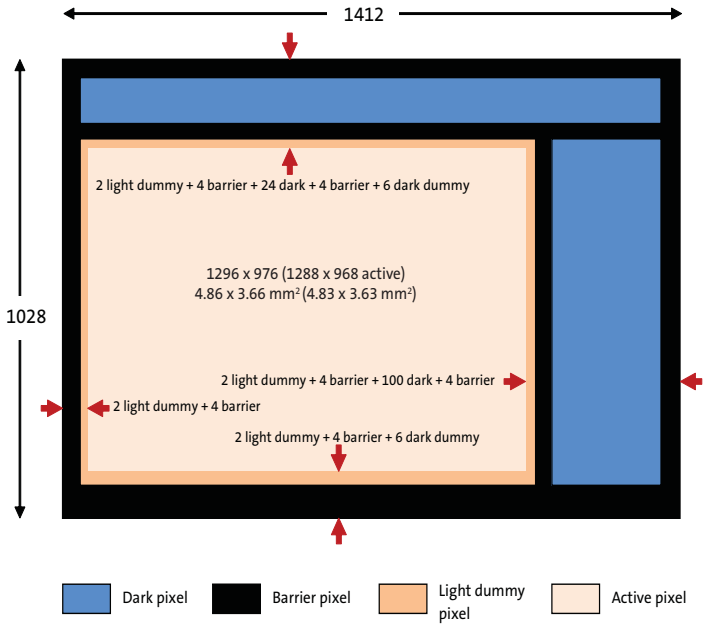
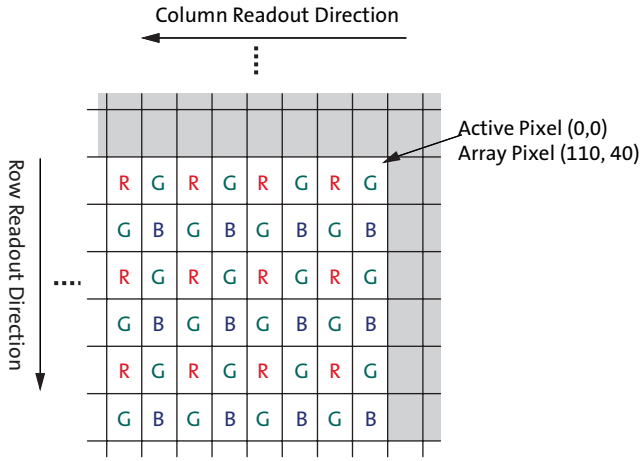


Figure 7: Pixel Color Pattern Detail (Top Right Corner)

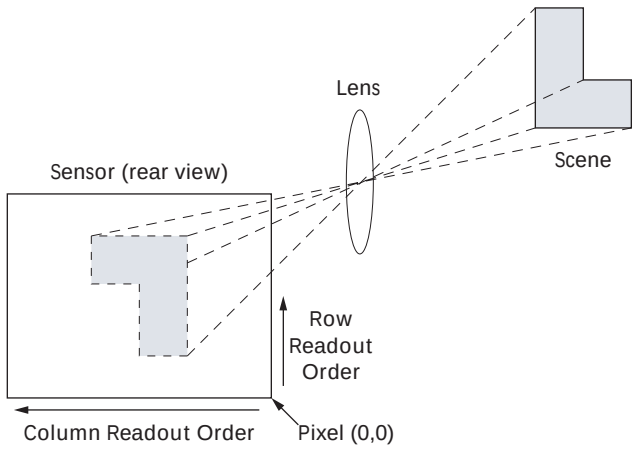


Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 7). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (110, 40).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 8. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 8 on page 14.

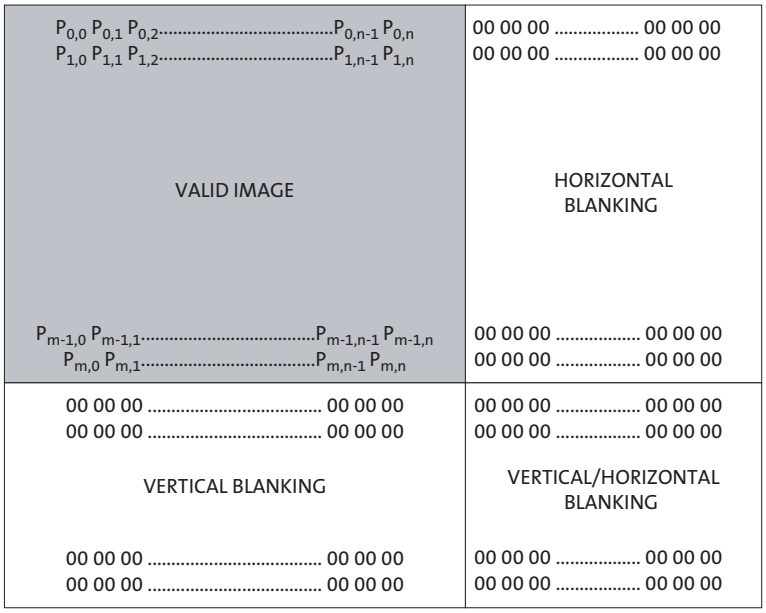
Figure 8: Imaging a Scene



Output Data Format

The MT9M031 image data is read out in a progressive scan. Valid image data is surrounded by horizontal and vertical blanking (see Figure 9). The amount of horizontal row time (in clocks) is programmable through R0x300C. The amount of vertical frame time (in rows) is programmable through R0x300A. Line_Valid (LV) is HIGH during the shaded region of Figure 9. Optional Embedded Register setup information and Histogram statistic information are available in first 2 and last row of image data.

Figure 9: Spatial Illustration of Image Readout



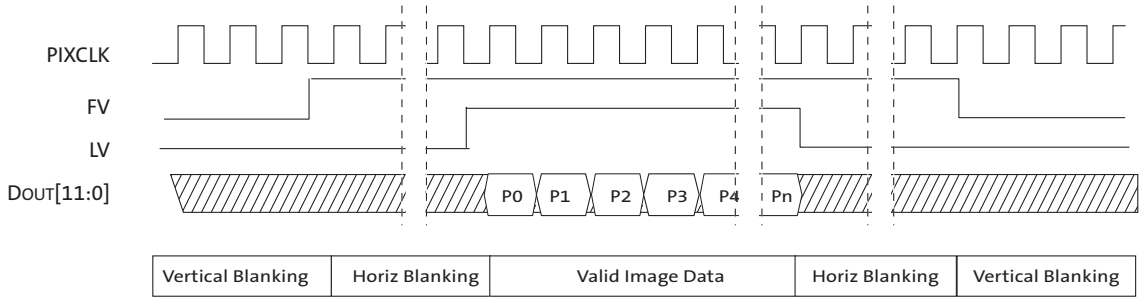
Readout Sequence

Typically, the readout window is set to a region including only active pixels. The user has the option of reading out dark regions of the array, but if this is done, consideration must be given to how the sensor reads the dark regions for its own purposes.

Parallel Output Data Timing

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 968 rows of 1284 columns each. The FV and LV signals indicate the boundaries between frames and lines, respectively. PIXCLK can be used as a clock to latch the data. For each PIXCLK cycle, with respect to the falling edge, one 12-bit pixel datum outputs on the DOUT pins. When both FV and LV are asserted, the pixel is valid. PIXCLK cycles that occur when FV is de-asserted are called vertical blanking. PIXCLK cycles that occur when only LV is de-asserted are called horizontal blanking.

Figure 10: Default Pixel Output Timing



LV and FV

The timing of the FV and LV outputs is closely related to the row time and the frame time.

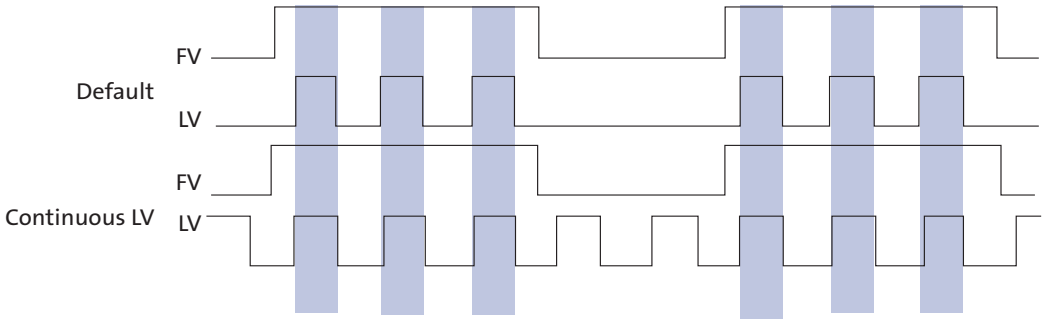
FV will be asserted for an integral number of row times, which will normally be equal to the height of the output image.

LV will be asserted during the valid pixels of each row. The leading edge of LV will be offset from the leading edge of FV by 6 PIXCLKs. Normally, LV will only be asserted if FV is asserted; this is configurable as described below.

LV Format Options

The default situation is for LV to be de-asserted when FV is de-asserted. By configuring R0x306E[1:0], the LV signal can take two different output formats. The formats for reading out four lines and two vertical blanking lines are shown in Figure 11.

Figure 11: LV Format Options

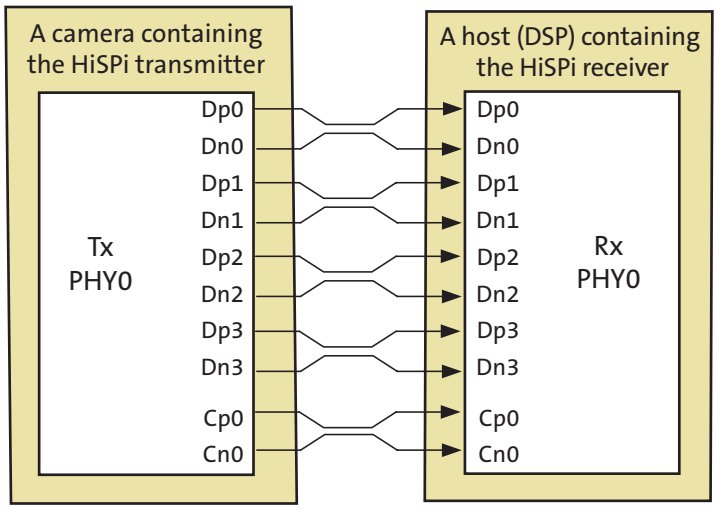


The timing of an entire frame is shown in Figure 14: “Line Timing and FRAME_VALID/ LINE_VALID Signals,” on page 18.

Serial Output Data Timing

The MT9M031 also uses Aptina's High-Speed Serial Pixel Interface (“HiSpi”). The physical interface comprises differential serial data lines and a differential clock line. The protocol layer formats the data and synchronization signals separately, with Sync codes defined for active image boundaries. Figure 12 shows the configuration between the HiSPi transmitter and the receiver.

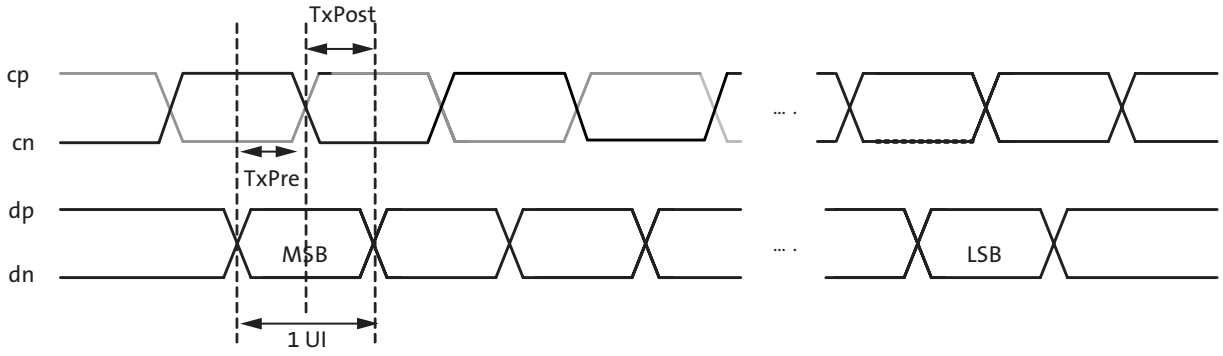
Figure 12: HiSPi Transmitter and Receiver Interface Block Diagram



HiSPi Physical Layer

The HiSPi physical layer is partitioned into blocks of four data lanes and an associated clock lane. Depending on the operating mode and data rate, it can configure from two to three lanes. Dp3 and Dn3 are not supported by the MT9M031 but pins are connected on the package. The PHY will serialize a 12-bit data word and transmit each bit of data centered on a rising edge of the clock, the second on the following edge of clock. Figure 13 shows bit transmission. In this example, the word is transmitted in order of MSB to LSB. The receiver latches data at the rising and falling edge of the clock.

Figure 13: Timing Diagram



Frame Time

The pixel clock (PIXCLK) represents the time needed to sample 1 pixel from the array. The sensor outputs data at the maximum rate of 1 pixel per PIXCLK. One row time (t_{ROW}) is the period from the first pixel output in a row to the first pixel output in the next row. The row time and frame time are defined by equations in Table 5.

Figure 14: Line Timing and FRAME_VALID/LINE_VALID Signals

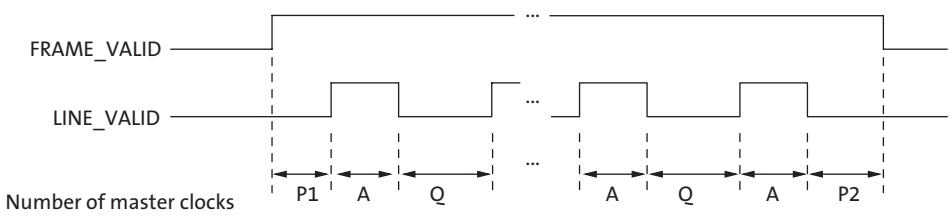


Table 5: Frame Time (Example Based on 1280 x 960, 45 Frames Per Second)

Parameter	Name	Equation	Default Timing at 74.25 MHz
A	Active data time	Context A: R0x3008 - R0x3004 + 1 Context B: R0x308E - R0x308A + 1	1280 pixel clocks = 17.23µs
P1	Frame start blanking	6 (fixed)	6 pixel clocks = 0.08µs
P2	Frame end blanking	6 (fixed)	6 pixel clocks = 0.08µs
Q	Horizontal blanking	R0x300C - A	370 pixel clocks = 4.98µs
A+Q (tROW)	Line (Row) time	R0x300C	1650 pixel clocks = 22.22µs
V	Vertical blanking	Context A: (R0x300A-1(R0x3006-R0x3002+1)) x (A + Q) Context B: ((R0x30AA-1(R0x3090-R0x308C+1)) x (A + Q)	49,500 pixel clocks = 666.66µs
Nrows x (A + Q)	Frame valid time	Context A: ((R0x3006-R0x3002+1)*(A+Q))-Q+P1+P2 Context B: ((R0x3090-R0x308C+1)*(A+Q))-Q+P1+P2	1,584,000 pixel clocks = 21.33ms
F	Total frame time	V + (Nrows x (A + Q))	1,633,500 pixel clocks = 22.22ms

Sensor timing is shown in terms of pixel clock cycles (see Figure 9 on page 15). The recommended pixel clock frequency is 74.25 MHz. The vertical blanking and the total frame time equations assume that the integration time (coarse integration time plus fine integration time) is less than the number of active lines plus the blanking lines:

Window Height + Vertical Blanking *(EQ 1)*

If this is not the case, the number of integration lines must be used instead to determine the frame time, (see Table 6). In this example, it is assumed that the coarse integration time control is programmed with 2000 rows and the fine shutter width total is zero.

For Master mode, if the integration time registers exceed the total readout time, then the vertical blanking time is internally extended automatically to adjust for the additional integration time required. This extended value is **not** written back to the frame_length_lines register. The frame_length_lines register can be used to adjust frame-to-frame readout time. This register does not affect the exposure time but it may extend the readout time.

Table 6: Frame Time: Long Integration Time

Parameter	Name	Equation (Number of Pixel Clock Cycles)	Default Timing at 74.25 MHz
F'	Total frame time (long integration time)	Context A: (R0x3012 x (A + Q)) + R0x3014 + P1 + P2 Context B: (R0x3016 x (A + Q)) + V R0x3018 + P1 + P2	3,300,012 pixel clocks = 44.44ms

Note: The MT9M031 uses column parallel analog-digital converters; thus short line timing is not possible. The minimum total line time is 1650 columns (horizontal width + horizontal blanking). The minimum horizontal blanking is 370.

Two-Wire Serial Register Interface

The two-wire serial interface bus enables read/write access to control and status registers within the MT9M031. This interface is designed to be compatible with the electrical characteristics and transfer protocols of the I^2C specification.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two-wire serial interface specification allow the slave device to drive SCLK LOW; the MT9M031 uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements:

1. a (repeated) start condition
2. a slave address/data direction byte
3. an (a no) acknowledge bit
4. a message byte
5. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Stop Condition

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The default slave addresses used by the MT9M031 are 0x20 (write address) and 0x21 (read

address) in accordance with the specification. Alternate slave addresses of 0x30 (write address) and 0x31 (read address) can be selected by enabling and asserting the SADDR input.

An alternate slave address can also be programmed through R0x31FC.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No-Acknowledge Bit

The no-acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

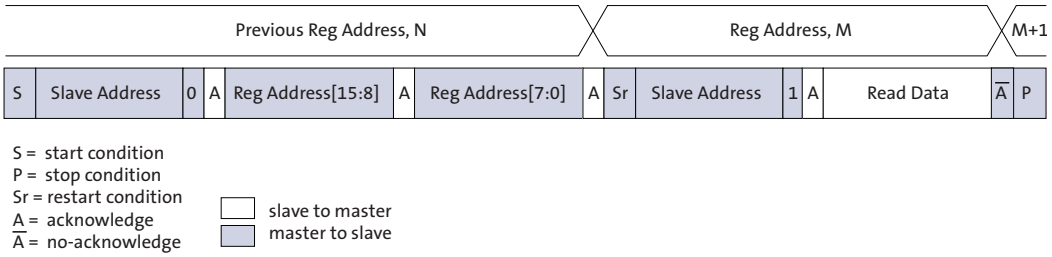
If the request was a WRITE, the master then transfers the 16-bit register address to which the WRITE should take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8-bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

This sequence (Figure 15 on page 22) starts with a dummy WRITE to the 16-bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8-bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. Figure 15 shows how the internal register address maintained by the MT9M031 is loaded and incremented as the sequence proceeds.

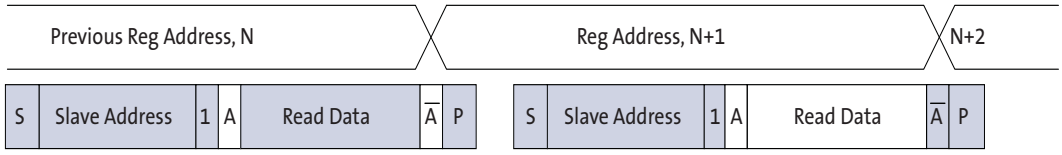
Figure 15: Single READ from Random Location



Single READ from Current Location

This sequence (Figure 16) performs a read using the current value of the MT9M031 internal register address. The master terminates the READ by generating a no-acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

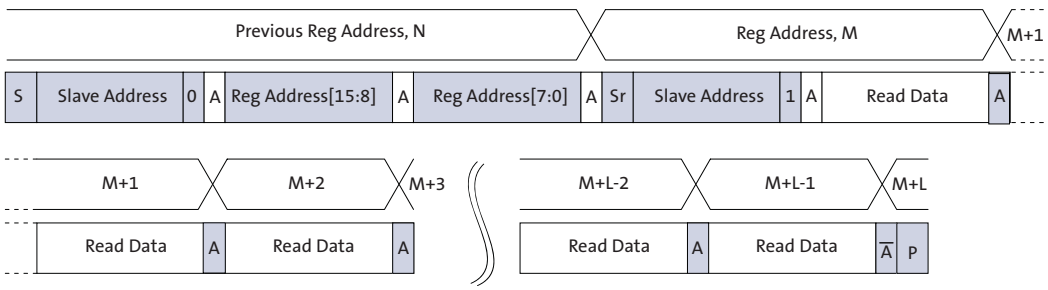
Figure 16: Single READ from Current Location



Sequential READ, Start from Random Location

This sequence (Figure 17) starts in the same way as the single READ from random location (Figure 15). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

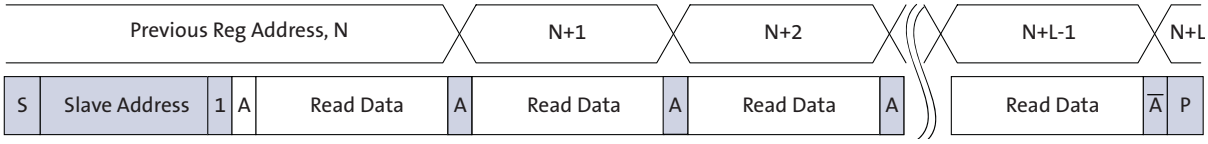
Figure 17: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 18) starts in the same way as the single READ from current location (Figure 16 on page 22). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

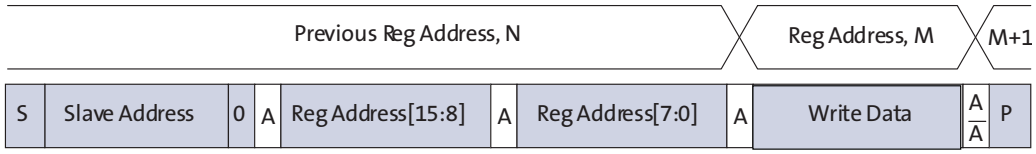
Figure 18: Sequential READ, Start from Current Location



Single WRITE to Random Location

This sequence (Figure 19) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

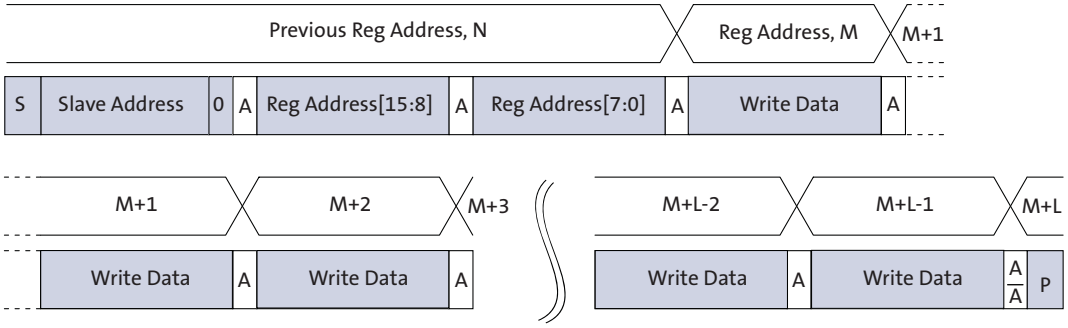
Figure 19: Single WRITE to Random Location



Sequential WRITE, Start at Random Location

This sequence (Figure 20) starts in the same way as the single WRITE to random location (Figure 19). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 20: Sequential WRITE, Start at Random Location



Real-Time Context Switching

In the MT9M031, the user may switch between two full register sets (listed in Table 7) by writing to a context switch change bit in R0x30B0[13]. This context switch will change all registers (no shadowing) at the frame start time and have the new values apply to the immediate next exposure and readout time.

Table 7: Real-Time Context-Switchable Registers

Register Description	Register Number	
	Context A	Context B
Y_Addr_Start	R0x3002	R0x308C
X_Addr_Start	R0x3004	R0x308A
Y_Addr_End	R0x3006	R0x3090
X_Addr_End	R0x3008	R0x308E
Coarse_Integration_Time	R0x3012	R0x3016
Fine_Integration_Time	R0x3014	R0x3018
Y_Odd_Inc	R0x30A6	R0x30A8
Green1_Gain (GreenR)	R0x3056	R0x30BC
Blue_Gain	R0x3058	R0x30BE
Red_Gain	R0x305A	R0x30C0
Green2_Gain (GreenB)	R0x305C	R0x30C2
Global_Gain	R0x305E	R0x30C4
Frame_Length_Lines	R0x300A	R0x30AA
Digital_Binning	R0x3032[1:0]	R0x3032[5:4]
Resampling in RGB mode	R0x306E[4]	R0x306E[4]
Operation_Mode_Ctrl	0x3082	0x3084

Feature Description

Note: See the MT9M031 Register Reference for additional details.

Operational Modes

The MT9M031 works in master (video) or trigger (single frame) modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two-wire serial interface for both modes.

Master Mode

In master mode, the exposure period occurs simultaneously with the frame readout (see Figures 21 and 22). This makes master mode the fastest mode of operation. When exposure time is greater than the frame length, the number of vertical blank rows is increased automatically to accommodate the exposure time.

Figure 21: Master Mode Synchronization Waveforms #1

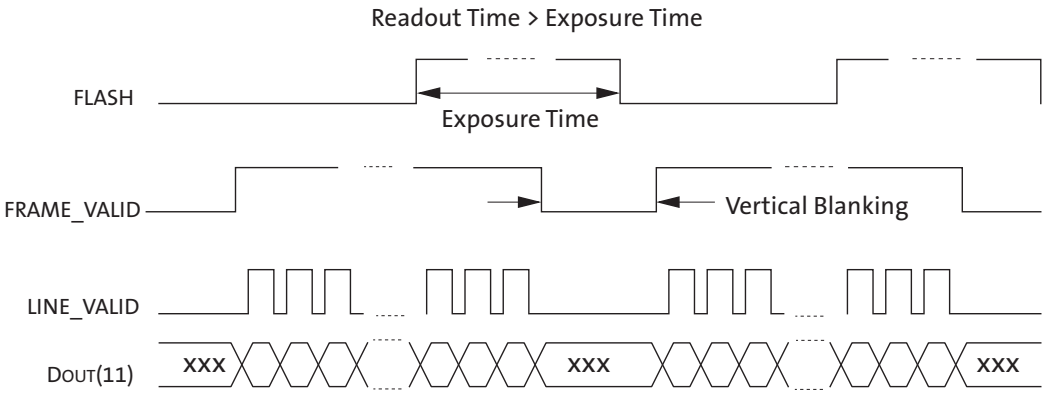
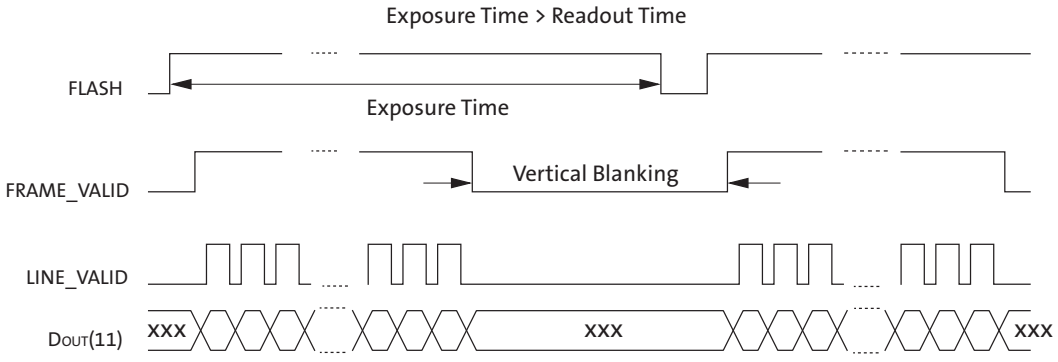


Figure 22: Master Mode Synchronization Waveforms #2



Trigger Mode

In trigger mode, the sensor accepts an input trigger signal which initiates exposure, and is immediately followed by readout. Figure 23 shows the interface signals used in trigger mode. The start of the exposure period is determined by the externally applied TRIGGER pulse that is input to the MT9M031. The exposure time is preprogrammed at R0x3012 and R0x3014 (for context A) or R0x3016 and R0x3018 (for context B) through the two-

wire serial interface. After the frame's exposure period is complete, the readout process commences by outputting the syncs and data. Trigger mode allows the sensor to capture a single image or a sequence of images. The frame rate may only be controlled by changing the period of the user supplied TRIGGER pulse train. If the TRIGGER input is left in the asserted state, the sensor will automatically initiate a new frame acquisition sequence upon completion of the current frame. The frame synchronization waveforms for trigger mode are shown in Figures 24 and Figure .

Figure 23: Trigger Mode Interface Signals

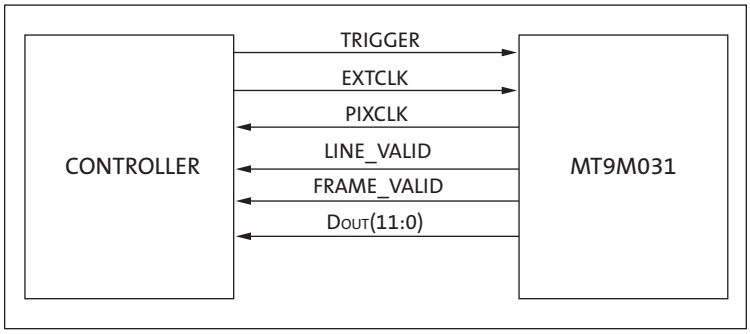
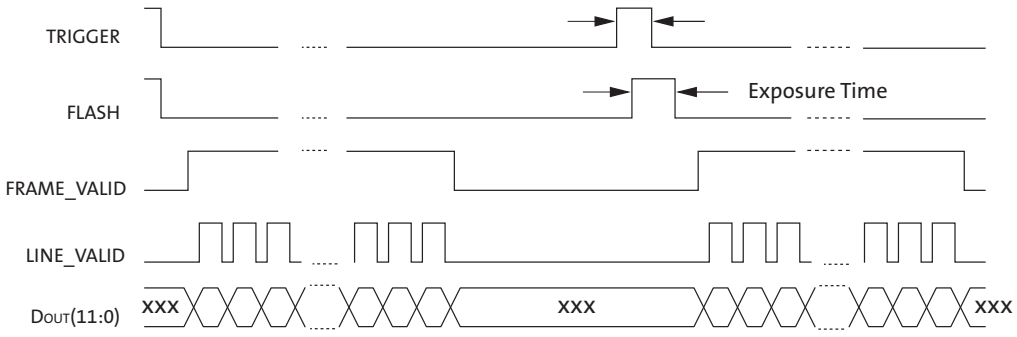


Figure 24: Trigger Mode Frame Synchronization Waveforms



Features

See the MT9M031 Register Reference for additional details.

Reset

The MT9M031 may be reset by using RESET_BAR (active LOW) or the reset register.

Hard Reset of Logic

The RESET_BAR pin can be connected to an external RC circuit for simplicity. The recommended RC circuit uses a 10kΩ resistor and a 0.1µF capacitor. The rise time for the RC circuit is 1µs maximum.

Soft Reset of Logic

Soft reset of logic is controlled by the R0x301A Reset register. Bit 0 is used to reset the digital logic of the sensor while preserving the existing two-wire serial interface configuration. Furthermore, by asserting the soft reset, the sensor aborts the current frame it is processing and starts a new frame. This bit is a self-resetting bit and also returns to "0" during two-wire serial interface reads.

Clocks

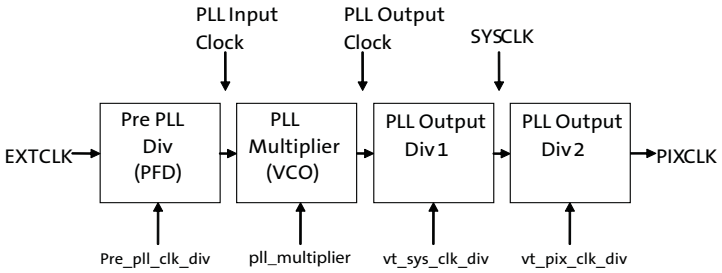
The MT9M031 requires one clock input (EXTCLK).

PLL-Generated Master Clock

The PLL contains a prescaler to divide the input clock applied on EXTCLK, a VCO to multiply the prescaler output, and two divider stages to generate the output clock. The clocking structure is shown in Figure 25 on page 27. PLL control registers can be programmed to generate desired master clock frequency.

Note: The PLL control registers must be programmed while the sensor is in the software Standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is undefined.

Figure 25: PLL-Generated Master Clock PLL Setup



The PLL is enabled by default on the MT9M031. To configure and use the PLL:

1. Bring the MT9M031 up as normal; make sure that ^{f}EXTCLK is between 6 and 50MHz and ensure the sensor is in software standby (R0x301A-B[2]= 0). PLL control registers must be set in software standby.

2. Set PLL_Multiplier, Pre_PLL_Clk_Div, Vt_Sys_Clk_Div, and Vt_Pix_Clk_Div based on the desired input (^{f}EXTCLK) and output (^{f}PIXCLK) frequencies. Determine the M, N, P1, and P2 values to achieve the desired fPIXCLK using this formula:

   $^{f}PIXCLK = (^{f}EXTCLK \times M) / (N \times P1 \times P2)$
   where
   M = PLL_Multiplier
   N = Pre_PLL_Clk_Div
   P1 = Vt_Sys_Clk_Div
   P2 = Vt_PIX_Clk_Div
3. Wait 1ms to ensure that the VCO has locked.
4. Set R0x301A-B[2]=1 to enable streaming and to switch from EXTCLK to the PLL-generated clock.

Note: The PLL can be bypassed at any time (sensor will run directly off EXTCLK) by setting R0x30B0-1[15]=1. However, only the parallel data interface is supported with the PLL bypassed. The PLL is always bypassed in software standby mode.

Spread-Spectrum Clocking

To facilitate improved EMI performance, the external clock input allows for spread spectrum sources, with no impact on image quality. Limits of the spread spectrum input clock are:

- 5% maximum clock modulation
- 35 kHz maximum modulation frequency
- Accepts triangle wave modulation, as well as sine or modified triangle modulations.

Stream/Standby Control

The sensor goes into standby mode by setting stream register R0x301A[2] to 0. Once the sensor detects that standby is asserted, it completes the current line or frame (depending on R0x301A[4] value) before disabling the digital logic, internal clocks, and analog power enable signal. To release the sensor out from the standby mode, reset stream register back to 1. See “Power-On Reset and Standby Timing” on page 44 for more information on standby.

Window Control

Registers X_Addr_Start, X_Addr_End, Y_Addr_Start, and Y_Addr_End control the size and starting coordinates of the image window.

The exact window height and width out of the sensor is determined by the difference between the Y address start and end registers or the X address start and end registers, respectively. Minimum and maximum window sizes are defined by R0x1180 through R0x1186.

The MT9M031 allows different window sizes for context A and context B.

Blanking Control

Horizontal blank and vertical blank times are controlled by the Line_length_Pck and Frame_Length_Lines registers, respectively.

- Horizontal blanking is specified in terms of pixel clocks. It is calculated by subtracting the X window size from the Line_Length_Pck register. The minimum horizontal blanking is 370 pixel clocks.

- Vertical blanking is specified in terms of numbers of lines. It is calculated by subtracting the Y window size from the Frame_Length_Lines register. The minimum allowed value for ten vertical blanking is 25 lines.

The actual imager timing can be calculated using Table 5 on page 18 and Table 6 on page 19, which describe the Line Timing and FV/LV signals.

When in HDR mode, the maximum size is 1280 x 960.

Readout Modes

By default, the resolution of the output image is the full width and height of the FOV as defined above. The output resolution can be reduced by digital binning.

Digital Binning

All of the pixels in the FOV contribute to the output image in digital binning mode. This can result in a more pleasing output image with reduced artifacts. It also improves low-light performance. For RGB and monochrome mode, the digital binning factor is set by the register DIGITAL_BINNING (R0x3032). For Context A, use bits [1:0], for Context B, use bits [5:4]. Available settings are: 00 = No binning; 01 = Horizontal binning; 10 = Horizontal and vertical binning. For RGB mode, resampling must be enabled by setting bit 4 of register 0x306E.

Skipping

Skipping reduces resolution by using only selected pixels from the FOV in the output image. In skip mode, entire rows of pixels are not sampled, resulting in a lower resolution output image. A skip 2X mode skips one Bayer pair of pixels for every pair output. Skipping is set by R0x30A6 (context A) and R0x30A8 (context B). The maximum supported skip is 64 rows. Both Bayer and monochrome skip modes are supported.

Figure 26: Pixel Readout (no skipping)

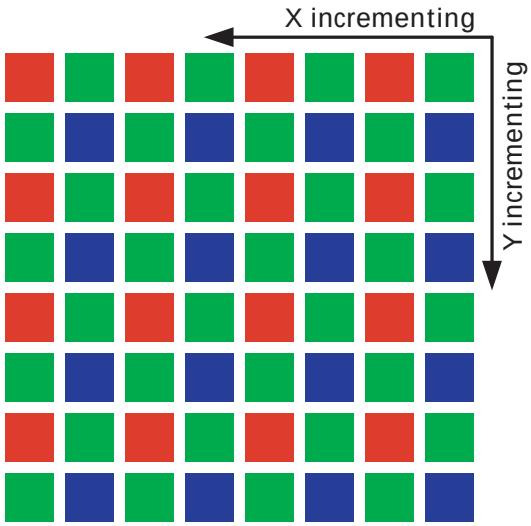


Figure 27: Pixel Readout (Row Skip 2X Bayer)

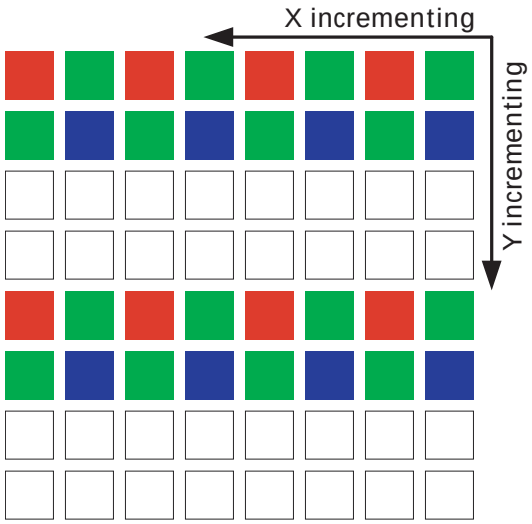
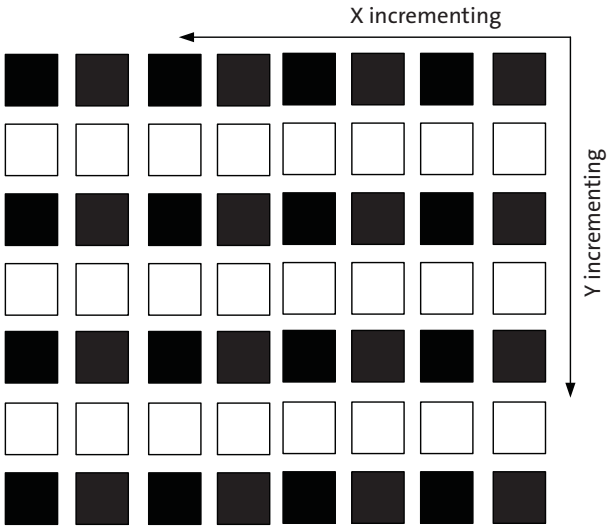


Figure 28: Pixel Readout (Row Skip 2X Monochrome)



Mirror

Column Mirror Image

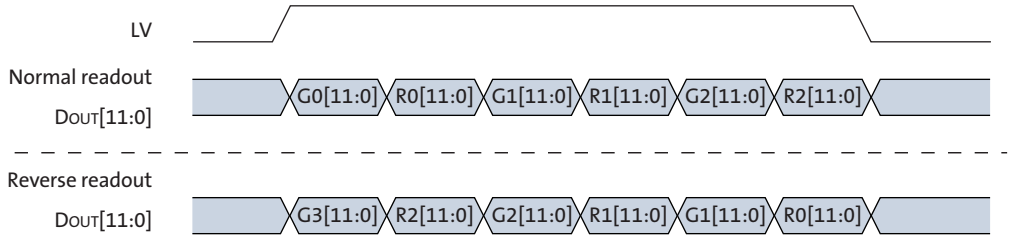
By setting R0x3040[14] = 1, the readout order of the columns is reversed, as shown in Figure 29. The starting color, and therefore the Bayer pattern, is preserved when mirroring the columns.

When using horizontal mirror mode, the user must retrigger column correction. Use R0x30D4[15] to disable and enable column correction.

To retrigger column correction:

1. Set horizontal mirror.
2. Disable column correction.
3. Enable column correction.

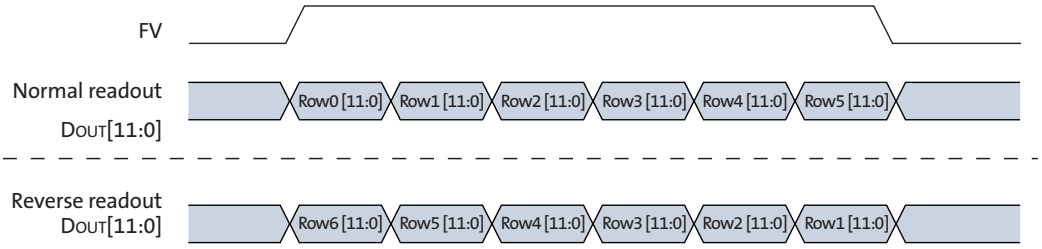
Figure 29: Six Pixels in Normal and Column Mirror Readout Modes



Row Mirror Image

By setting R0x3040[15] = 1, the readout order of the rows is reversed as shown in Figure 30. The starting Bayer color pixel is maintained in this mode by a 1-pixel shift in the imaging array.

Figure 30: Six Rows in Normal and Row Mirror Readout Modes



Maintaining a Constant Frame Rate

Maintaining a constant frame rate while continuing to have the ability to adjust certain parameters is the desired scenario. This is not always possible, however, because register updates are synchronized to the read pointer, and the shutter pointer for a frame is usually active during the readout of the previous frame. Therefore, any register changes that could affect the row time or the set of rows sampled causes the shutter pointer to start over at the beginning of the next frame.

By default, the following register fields cause a "bubble" in the output rate (that is, the vertical blank increases for one frame) if they are written in video mode, even if the new value would not change the resulting frame rate. The following list shows only a few examples of such registers; a full listing can be seen in the MT9M031 Register Reference.

- X_Addr_Start
- X_Addr_End
- Y_Addr_Start
- Y_Addr_End
- Frame_Length_Lines
- Line_Length_Pclk
- Coarse_Integration_Time
- Fine_Integration_Time
- Read_Mode

The size of this bubble is (Integration_Time × ^{t}ROW), calculating the row time according to the new settings.

The Coarse_Integration_Time and Fine_Integration_Time fields may be written to without causing a bubble in the output rate under certain circumstances. Because the shutter sequence for the next frame often is active during the output of the current frame, this would not be possible without special provisions in the hardware. Writes to these registers take effect two frames after the frame they are written, which allows the integration time to increase without interrupting the output or producing a corrupt frame (as long as the change in integration time does not affect the frame time).

Synchronizing Register Writes to Frame Boundaries

Changes to most register fields that affect the size or brightness of an image take effect on the frame after the one during which they are written. These fields are noted as "synchronized to frame boundaries" in the MT9M031 Register Reference. To ensure that a register update takes effect on the next frame, the write operation must be completed after the leading edge of FV and before the trailing edge of FV.

As a special case, in single frame mode, register writes that occur after FV but before the next trigger will take effect immediately on the next frame, as if there had been a Restart. However, if the trigger for the next frame occurs during FV, register writes take effect as with video mode.

Fields not identified as being frame-synchronized are updated immediately after the register write is completed. The effect of these registers on the next frame can be difficult to predict if they affect the shutter pointer.

Restart

To restart the MT9M031 at any time during the operation of the sensor, write a "1" to the Restart register (R0x301A[1] = 1). This has two effects: first, the current frame is interrupted immediately. Second, any writes to frame-synchronized registers and the shutter width registers take effect immediately, and a new frame starts. The current row completes before the new frame is started, so the time between issuing the Restart and the beginning of the next frame can vary by about ^{t}ROW.

Exposure

Total integration time is the result of Coarse_Integration_Time and Fine_Integration_Time registers, and depends also on whether manual or automatic exposure is selected.

The actual total integration time, ^{t}INT is defined as:

$$^{t}INT = {}^{t}INTCoarse + {}^{t}INTFine \quad \text{(EQ 2)}$$

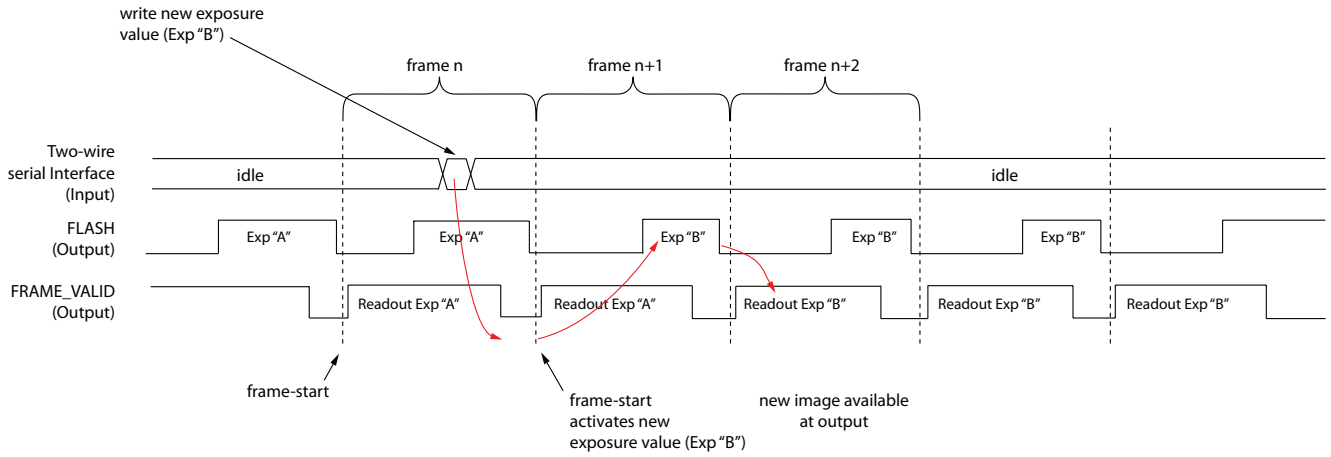
= (number of lines of integration x line time) + (number of pixels of integration x pixel time)

where:

- Number of Lines of Integration (Auto Exposure Control: Enabled)
  When automatic exposure control (AEC) is enabled, the number of lines of integration may vary from frame to frame, with the limits controlled by R0x311E (minimum auto exposure time) and R0x311C (maximum auto exposure time).
- Number of Lines of Integration (Auto Exposure Control: Disabled)
  If AEC is disabled, the number of lines of integration equals the value in R0x3012 (context A) or R0x3016 (context B).
- Number of Pixels of Integration
  The number of fine shutter width pixels is independent of AEC mode (enabled or disabled):
  - Context A: the number of pixels of integration equals the value in R0x3014.
  - Context B: the number of pixels of integration equals the value in R0x3018.

Typically, the value of the Coarse_Integration_Time register is limited to the number of lines per frame (which includes vertical blanking lines), such that the frame rate is not affected by the integration time. Figure 31 on page 34 describes the frame latency when integration is changed.

Figure 31: Latency When Changing Integration



Exposure Indicator

The exposure indicator is controlled by:

The MT9M031 provides an output pin, FLASH, to indicate when the exposure takes place. When R0x3046[8]is set, FLASH is HIGH during exposure. By using R0x3046[7], the polarity of the FLASH pin can be inverted.

Automatic Exposure Control

The integrated automatic exposure control (AEC) is responsible for ensuring that optimal settings of exposure and gain are computed and updated every other frame. AEC can be enabled or disabled by R0x3100[0].

When AEC is disabled (R0x3100[0] = 0), the sensor uses the manual exposure value in coarse and fine shutter width registers and the manual gain value in the gain registers.

When AEC is enabled (R0x3100[0]=1), the target luma value is set by R0x3102. For the MT9M031 this target luma has a default value of 0x0500 or about half scale. The maximum auto exposure value is limited by R0x311C; the minimum auto exposure is limited by R0x311E. These values are in units of line-times.

The exposure control measures current scene luminosity by accumulating a histogram of pixel values while reading out a frame. It then compares the current luminosity to the desired output luminosity. Finally, the appropriate adjustments are made to the exposure time and gain. All pixels are used, regardless of color or mono mode.

Gain

Analog, column, and digital gain are available on the sensor. Column gain is controlled by R0x30B0 bits 4 and 5. Column gain is equal to 1x when the register is set to 0x80, 2x when set to 0x90, 4x when set to 0xA0, and 8x when set to 0xB0. When Bit 13 is set to 0, Context A controls column gain and when set to 1 Context B controls column gain. Digital gain can be controlled globally by R0x305E (Context A) or R0x30C4 (Context B). There are also registers that allow individual control over each Bayer color (GreenR, GreenB, Red, Blue).

The format for digital gain setting is *xxx.yyyyy* where 0b00100000 represents a 1X gain setting and 0b00110000 represents a 1.5X gain setting.

Black Level Correction

Black level correction is handled automatically by the image sensor. No adjustments are provided except to enable or disable this feature. Setting R0x30EA[15] disables the automatic black level correction. Default setting is for automatic black level calibration to be enabled.

The automatic black level correction measures the average value of pixels from a set of optically black lines in the image sensor. The pixels are averaged as if they were light-sensitive and passed through the appropriate gain. This line average is then digitally low-pass filtered over many frames to remove temporal noise and random instabilities associated with this measurement. The new filtered average is then compared to a minimum acceptable level, low threshold, and a maximum acceptable level, high threshold. If the average is lower than the minimum acceptable level, the offset correction value is increased by a predetermined amount. If it is above the maximum level, the offset correction value is decreased by a predetermined amount. The high and low thresholds have been calculated to avoid oscillation of the black level from below to above the targeted black level.

Row-wise Noise Correction

Row (Line)-wise Noise Correction is handled automatically by the image sensor. No adjustments are provided except to enable or disable this feature. Clearing R0x3044[10] disables the row noise correction. Default setting is for row noise correction to be enabled.

Row-wise noise correction is performed by calculating an average from a set of optically black pixels at the start of each line and then applying each average to all the active pixels of the line.

Defective Pixel Correction

Defective Pixel Correction is intended to compensate for defective pixels by replacing their value with a value based on the surrounding pixels, making the defect less noticeable to the human eye. The defect pixel correction feature supports up to 200 defects. The locations of defective pixels are stored in a table on chip during the manufacturing process; this table is accessible through the two-wire serial interface. There is no provision for later augmenting the defect table entries.

The DPC algorithm is one-dimensional, calculating the resulting averaged pixel value based on nearby pixels within a row. The algorithm distinguishes between color and monochrome parts; for color parts, the algorithm uses nearest neighbor in the same color plane.

The feature may be enabled with other readout modes: windowing, digital binning, and horizontal/vertical flip. Pixel correction may be enabled or disabled, the default condition is disabled.

Test Patterns

The MT9M031 has the capability of injecting a number of test patterns into the top of the datapath to debug the digital logic. With one of the test patterns activated, any of the datapath functions can be enabled to exercise it in a deterministic fashion. Test patterns are selected by Test_Pattern_Mode register (R0x3070). Only one of the test patterns can be enabled at a given point in time by setting the Test_Pattern_Mode register according to Table 8. When test patterns are enabled the active area will receive the value specified

by the selected test pattern and the dark pixels will receive the value in Test_Pattern_Green (R0x3074 and R0x3078) for green pixels, Test_Pattern_Blue (R0x3076) for blue pixels, and Test_Pattern_Red (R0x3072) for red pixels.

Note: Turn off black level calibration (BLC) when Test Pattern is enabled.

Table 8: Test Pattern Modes

Test_Pattern_Mode	Test Pattern Output
0	No test pattern (normal operation)
1	Solid color test pattern
2	100% color bar test pattern
3	Fade-to-grey color bar test pattern
256	Walking 1s test pattern (12-bit)

Color Field

When the color field mode is selected, the value for each pixel is determined by its color. Green pixels will receive the value in Test_Pattern_Green, red pixels will receive the value in Test_Pattern_Red, and blue pixels will receive the value in Test_Pattern_Blue.

Vertical Color Bars

When the vertical color bars mode is selected, a typical color bar pattern will be sent through the digital pipeline.

Walking 1s

When the walking 1s mode is selected, a walking 1s pattern will be sent through the digital pipeline. The first value in each row is 1.

Electrical Specifications

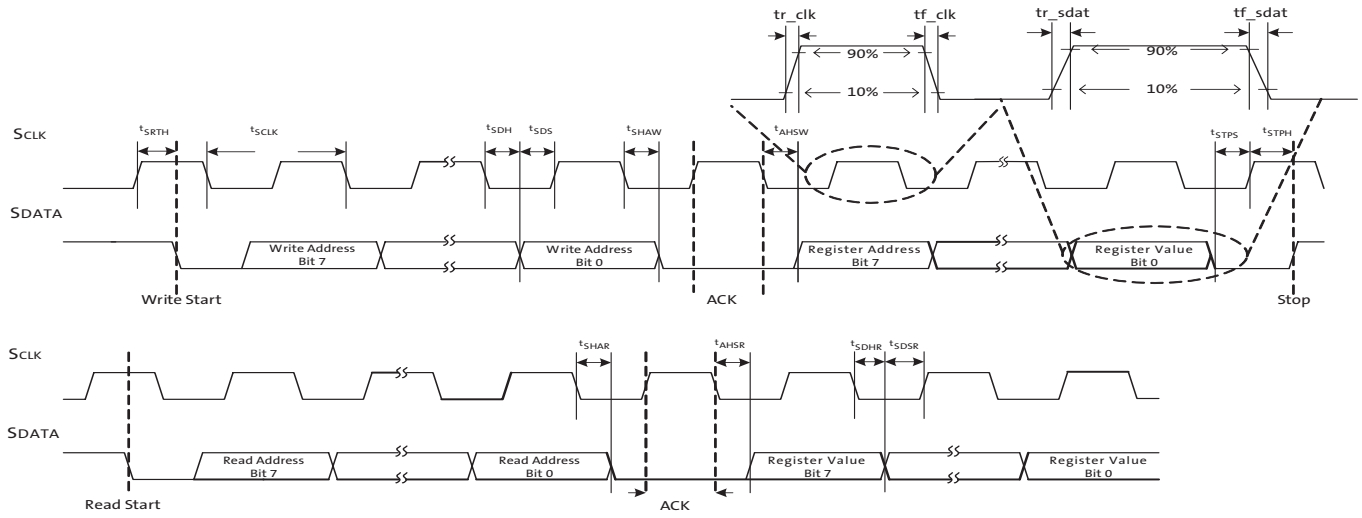
Unless otherwise stated, the following specifications apply to the following conditions:

VDD = 1.8V – 0.10/+0.15; VDD_IO = VDD_PLL = VAA = VAA_PIX = 2.8V ± 0.3V; VDD_SLVS = 0.4V – 0.1/+0.2; T_A = -30°C to +70°C; output load = 10pF; frequency = 74.25 MHz; HiSPi off.

Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 32 and Table 9.

Figure 32: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Table 9: Two-Wire Serial Bus Timing Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
^{f}SCLK	Serial interface input clock frequency				400	kHz
^{t}SCLK	Serial Input clock period				2.5	µsec
	SCLK duty cycle	When active	40	50	60	%
^{t}r_sclk	SCLK rise time			165		ns
^{t}f_sclk	SCLK fall time			6		ns
^{t}r_sdat	SDATA rise time	1.5 kΩ pull-up		180		ns
^{t}f_sdat	SDATA fall time			9		ns
^{t}SRTS	Start setup time	WRITE/READ	148	150	167	ns
^{t}SRTH	Start hold time	WRITE/READ	36.9	36	37.6	ns
^{t}SDSW	SDATA setup	WRITE	0	5	12	ns
^{t}SDHW	SDATA hold	WRITE	1.3	36	37	ns
^{t}ASW	ACK setup time	WRITE	146	146	148	ns
^{t}AHW	ACK hold time	WRITE	98.9	107	144	ns
^{t}STPS	Stop setup time	WRITE/READ		624		ns

Table 9: Two-Wire Serial Bus Timing Parameters (continued)

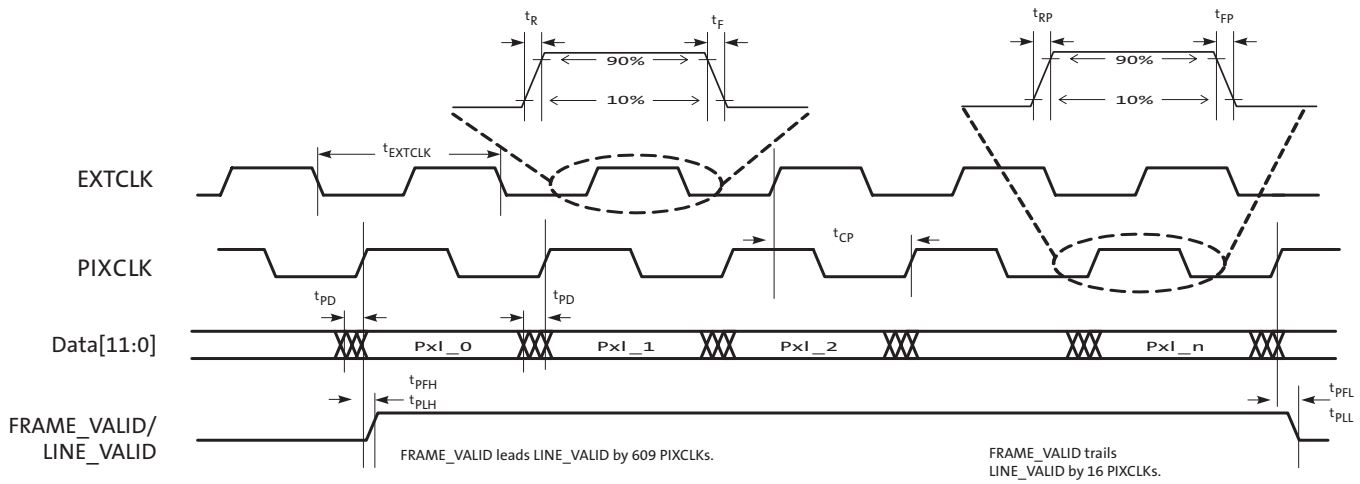
Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{STPH}	Stop hold time	WRITE/READ		1.61		ns
t_{ASR}	ACK setup time	READ	192	228	229	ns
t_{AHR}	ACK hold time	READ	247	284	287	ns
t_{SDSR}	SDATA setup	READ	654	655	690	ns
t_{SDHR}	SDATA hold	READ	560	595	596	ns
CIN_SI	Serial interface input pin capacitance			3.5		pF
CLOAD_SD	SDATA max load capacitance			15		pF
RSD	SDATA external pull-up resistor			1.5		kΩ

I/O Timing

By default, the MT9M031 launches pixel data, FV and LV with the rising edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV and LV using the falling edge of PIXCLK.

See Figure 33 on page 38 and Table 10 on page 38 for I/O timing (AC) characteristics.

Figure 33: I/O Timing Diagram



*PLL disabled for t_{CP}

Table 10: I/O Timing Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1}$	Input clock frequency	PLL enabled	6	–	50	MHz
$t_{EXTCLK1}$	Input clock period	PLL enabled	166	–	15.6	ns
$f_{EXTCLK2}$	Input clock frequency	PLL disabled	6	–	74.25	MHz
$t_{EXTCLK2}$	Input clock period	PLL disabled	125	–	13.4	ns
t_R	Input clock rise time		–	–	–	V/ns
t_F	Input clock fall time		–	–	–	V/ns
t_{RP}	Pixclk rise time		–	–	–	V/ns
t_{FP}	Pixclk fall time		–	–	–	V/ns

Table 10: I/O Timing Characteristics (continued)

Symbol	Definition	Condition	Min	Typ	Max	Unit
	Clock duty cycle		40	50	60	%
t(PIX JITTER)	Jitter on PIXCLK		–	–	1.03	ns
tJITTER2	Input clock jitter 74.25 MHz		–	–	–	ps
tCP	EXTCLK to PIXCLK propagation delay	Nominal voltages	–	–	–	ns
fPIXCLK	PIXCLK frequency	Default	6	–	74.25	MHz
tPD	PIXCLK to data valid	Default	–	–	–	ns
tPFH	PIXCLK to FV HIGH	Default	–	–	–	ns
tPLH	PIXCLK to LV HIGH	Default	–	–	–	ns
tPFL	PIXCLK to FV LOW	Default	–	–	–	ns
tPLL	PIXCLK to LV LOW	Default	–	–	–	ns
CLOAD	Output load capacitance		–	<10	–	pF
CIN	Input pin capacitance		–	2.5	–	pF

DC Electrical Characteristics

The DC electrical characteristics are shown in Table 11, Table 12 on page 41, and Table 13 on page 41.

Table 11: DC Electrical Characteristics

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		1.7	1.8	1.95	V
V_{DD_IO}	I/O digital voltage		–	1.8/2.8	–	V
V_{AA}	Analog voltage		2.5	2.8	3.1	V
V_{AA_PIX}	Pixel supply voltage		2.5	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage		2.5	2.8	3.1	V
V_{DD_SLVS}	HiSPi supply voltage		0.3	0.4	0.6	V
V_{IH}	Input HIGH voltage	V_{DD_IO} = 2.8V	–	–	–	V
		V_{DD_IO} = 1.8V	–	–	–	
V_{IL}	Input LOW voltage	V_{DD_IO} = 2.8V	–	–	–	V
		V_{DD_IO} = 1.8V	–	–	–	
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{DD_IO} or D_{GND}	–	–	–	µA
V_{OH}	Output HIGH voltage	V_{DD_IO} = 1.8V	–	–	–	V
		V_{DD_IO} = 2.8V	–	–	–	
V_{OL}	Output LOW voltage	V_{DD_IO} = 2.8V	–	–	–	V
I_{OH}	Output HIGH current	At specified V_{OH} = V_{DD_IO} - 400mv at 1.7V V_{DD_IO}	–	–	–	mA
I_{OL}	Output LOW current	At specified V_{OL} = 400mv at 1.7V V_{DD_IO}	–	–	–	mA
I_{OZ}	Tri-state output leakage current	V_{IN} = V_{DD_IO} or GND	–	–	–	µA

Table 12: Power Consumption

Mode	Full Resolution (45 fps)	Unit
Streaming	<400	mW

Caution **Stresses greater than those listed in Table 12 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.**

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Symbol
V_{SUPPLY}	Power supply voltage (all supplies)	–0.3	4.5	V	V_{SUPPLY}
I_{SUPPLY}	Total power supply current	–	200	mA	I_{SUPPLY}
I_{GND}	Total ground current	–	200	mA	I_{GND}
V_{IN}	DC input voltage	–0.3	V_{DD_IO} + 0.3	V	V_{IN}
V_{OUT}	DC output voltage	–0.3	V_{DD_IO} + 0.3	V	V_{OUT}
T_{STG}[1]	Storage temperature	–40	+85	°C	T_{STG}[1]

Notes:
1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

HiSPi Electrical Specifications

The HiSPi transmitter electrical specifications are listed at 700 MHz.

Table 14: Input Voltage Levels and Operating Temperatures

Parameter	Symbol	Min	Typ	Max	Unit
HiSPi power supply	V_{DD_SLVS}	0.3	0.4	0.6	V
Operating temperature	T_A	–30	–	70	°C

Table 15: Input Voltage and Current
Measurement Conditions: HiSPi Power Supply 0.4 V, Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Supply current (PWRHiSPi) (driving 100Ω load)	I_{DD_SLVS}	–	10	–	mA
HiSPi common mode voltage (driving 100Ω load)	V_{CMD}	V_{CMD}typ x 0.8	$V_{DD\_SLVS}/2$	V_{CMD}typ x 1.2	V
HiSPi differential output voltage (driving 100Ω load)	V_{DIFF}	V_{DIFF}typ x 0.8	$V_{DD\_SLVS}/2$	V_{DIFF}typ x 1.2	V
Output impedance	–	35	50	70	Ω

Figure 34: Differential Output Voltage for Clock or Data Pairs

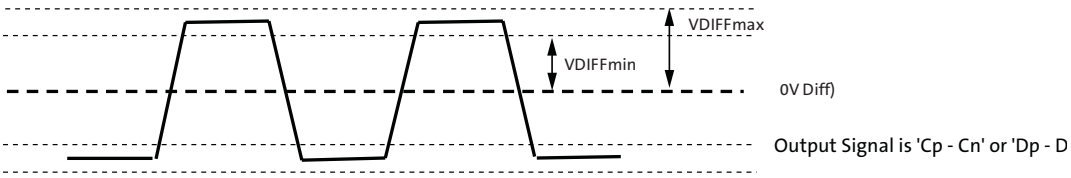


Table 16: Rise and Fall Times
Measurement Conditions: HiSPi Power Supply 0.4V, Max Freq 700MHz

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	1/UI	280	–	700	Mb/s
Max setup time from transmitter	TxPRE	–	600	–	ps
Max hold time from transmitter	TxPost	–	600	–	ps
Clock jitter t	CLKJITTER	–	100	–	ps
Rise time t	RISE	–	350	–	ps
Fall time t	FALL	–	350	–	ps
Clock duty t	PLL_DUTY	45	50	55	%

Figure 35: Eye Diagram for Clock and Data Signals

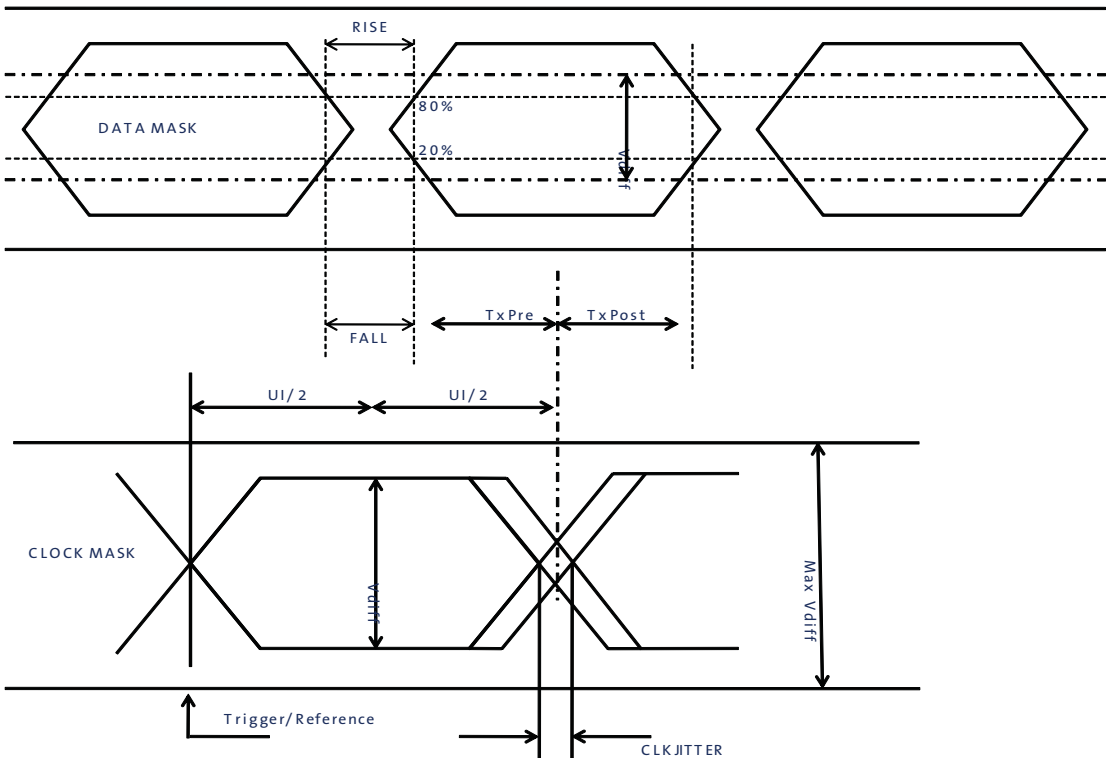
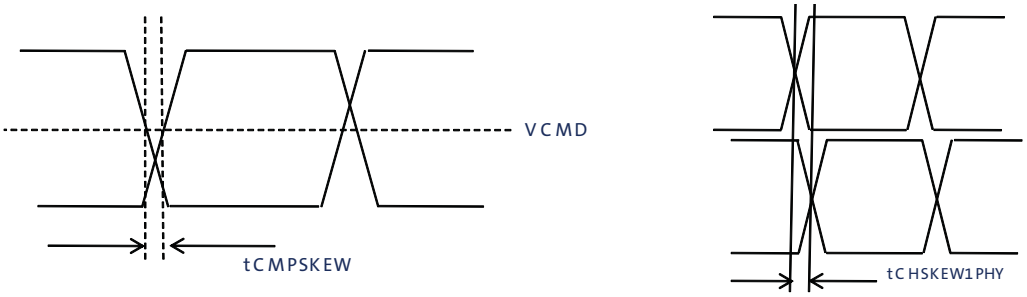


Table 17: Channel, PHY, and Intra-PHY Skew
Measurement Conditions: HiSPi Power Supply 0.4V, Max Freq 700 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Data channel to channel skew within one PHY	tCHSKEW1PHY	–	–	100	ps
Data or clock channel skew between two PHY	tCHSKEW2PHY	–	–	700	ps
Complementary skew between positive and negative output that comprises one clock or data channel	tCMPSKEW	–	–	50	ps

Figure 36: Skew Within the PHY and Output Channels



Power-On Reset and Standby Timing

Power-Up Sequence

The recommended power-up sequence for the MT9M031 is shown in Figure 37. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Turn on VDD_PLL power supply.
2. After 0–10µs, turn on VAA and VAA_PIX power supply.
3. After 0–10µs, turn on VDD_IO power supply.
4. After the last power supply is stable, enable EXTCLK.
5. Assert RESET_BAR for at least 1ms.
6. Wait 150000 EXTCLKs (for internal initialization into software standby.
7. Configure PLL, output, and image settings to desired values.
8. Wait 1ms for the PLL to lock.
9. Set streaming mode (R0x301a[2] = 1).

Figure 37: Power Up

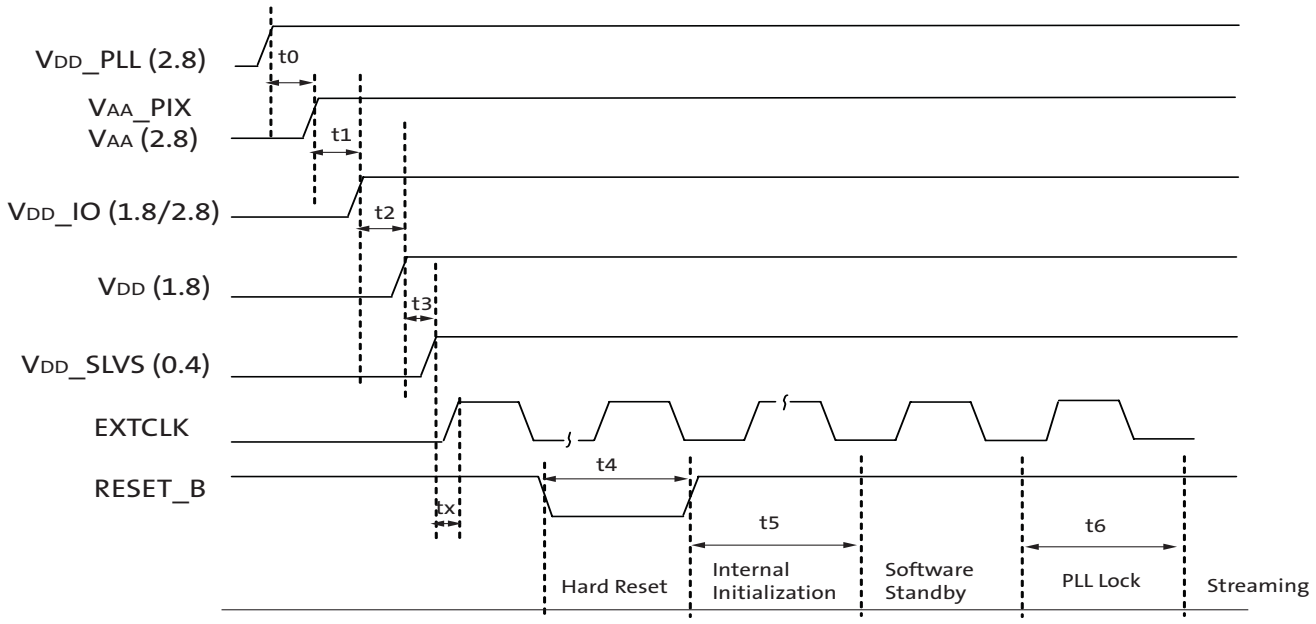


Table 18: Power-Up Sequence

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX	t0	0	10	–	µS
VAA/VAA_PIX to VDD_IO	t1	0	10	–	µS
VDD_IO to VDD	t2	10	–	–	µS
VDD to VDD_SLVS	t3	10	–	–	µS
Xtal settle time	tx	–	30[1]	–	mS
Hard Reset	t4	1[2]	–	–	mS
Internal Initialization	t5	150000	–	–	EXTCLKS
PLL Lock Time	t6	1	–	–	mS

Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 mS.
2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.

Power-Down Sequence

The recommended power-down sequence for the MT9M031 is shown in Figure 38. The available power supplies (VDD_IO, VDD, VDD_SLVS, VDD_PLL, VAA, VAA_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off VDD_SLVS.
4. Turn off VDD.
5. Turn off VDD_IO
6. Turn off VAA/VAA_PIX.
7. Turn off VDD_PLL.

Figure 38: Power Down

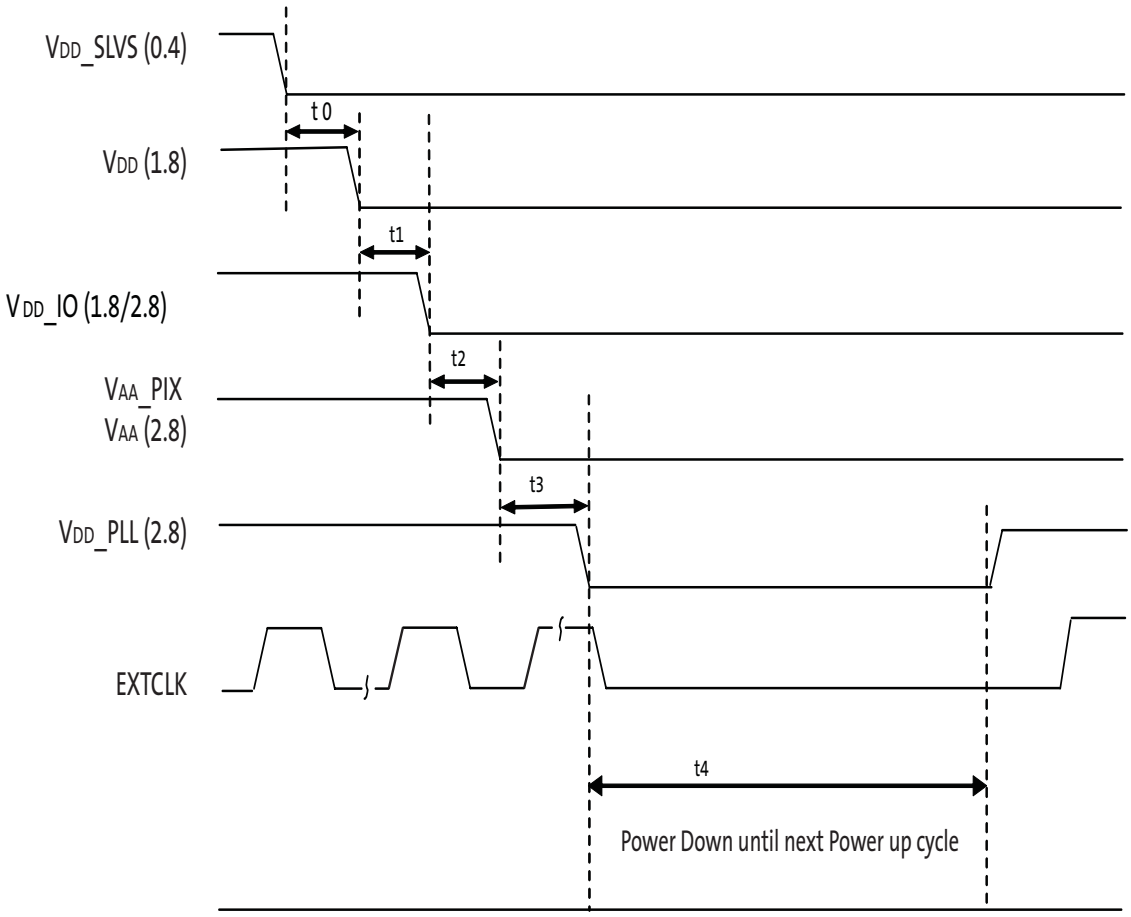


Table 19: Power-Down Sequence

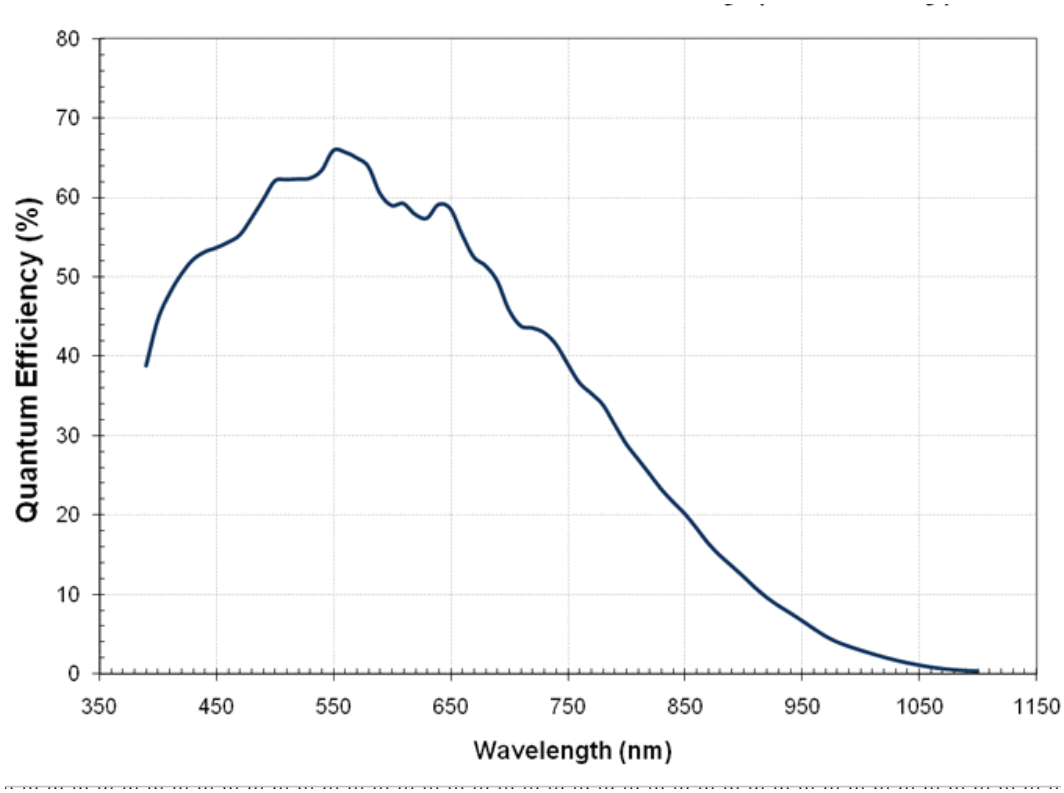
Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_SLVS to VDD	t0	0	–	–	µS
VDD to VDD_IO	t1	0	–	–	µS
VDD_IO to VAA/VAA_PIX	t2	0	–	–	µS
VAA/VAA_PIX to VDD_PLL	t3	0	–	–	µS
PwrDn until Next PwrUp Time	t4	100	–	–	mS

Note: t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

Figure 39: Estimated Quantum Efficiency – Color Sensor

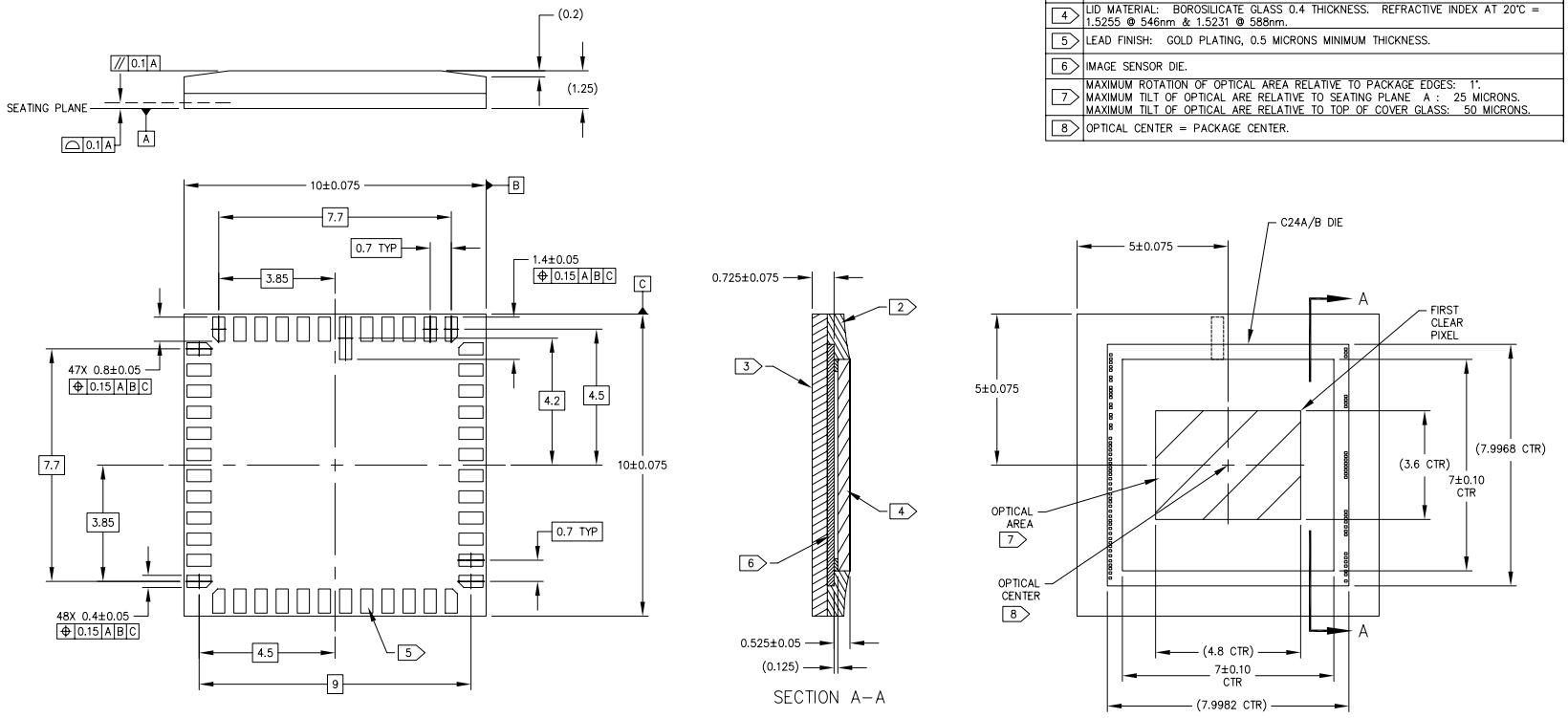
TBD

Figure 40: Estimated Quantum Efficiency – Monochrome Sensor



Package Dimensions

Figure 41: 48 iLCC Package Outline Drawing



Note: All dimensions in millimeters.

Revision History

Rev. A 10/16/09

- Initial release