



Package Style: QFN, 20-Pin, 3.5mmx3.5mmx0.55mm

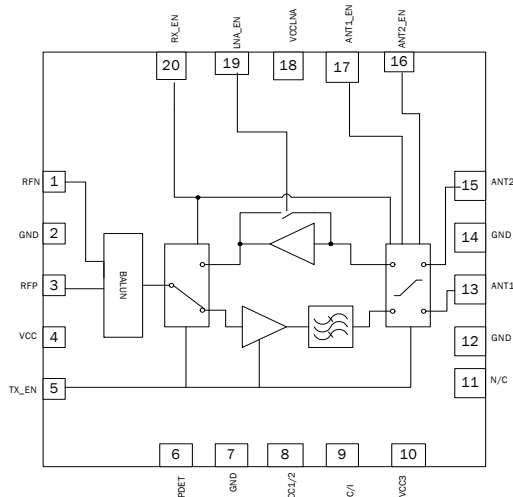


Features

- TX P1dB: 27 dBm
- Integrated RF Front End Module, Balun, PA, Filter, Ant Switch, LNA with Bypass, TX/RX Switch
- Single Differential Bidirectional TX/RX Port.
- Compatible with most transceivers

Applications

- ZigBee® 802.15.4 Based Systems for Remote Monitoring and Control
- WiFi 802.11b/g
- 2.4GHz ISM band applications
- Smart Meters for Energy Management



Functional Block Diagram

Product Description

The RF6505 integrates a complete solution in a single Front End Module (FEM) for WiFi and ZigBee applications in the 2.4GHz to 2.5GHz band. This FEM integrates a balun, TX/RX switch, power amplifier, harmonic filter, DP2T switch, and low noise amplifier with bypass mode. It provides a single balanced TDD access for Rx and Tx paths along with two ports for connecting a diversity solution or a test port. The device is provided in a 3.5mm x 3.5mm x 0.5mm, 20-pin QFN package.

Ordering Information

RF6505	Standard 25 piece bag
RF6505SR	Standard 100 piece reel
RF6505TR7	Standard 750 piece reel
RF6505TR13	Standard 2500 piece reel
RF6505PCK-410	Fully assembled evaluation board and 5 loose pieces

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☒ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BIFET HBT
☒ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	5	V
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
ESD Human Body Model RF Pins	500	V
ESD Human Body Model All Other Pins	500	V
ESD Charge Device Model All Pins	500	V
Moisture Sensitivity Level	MSL 2	
Maximum Input Power to PA and LNA (no damage)	+5	dBm

**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

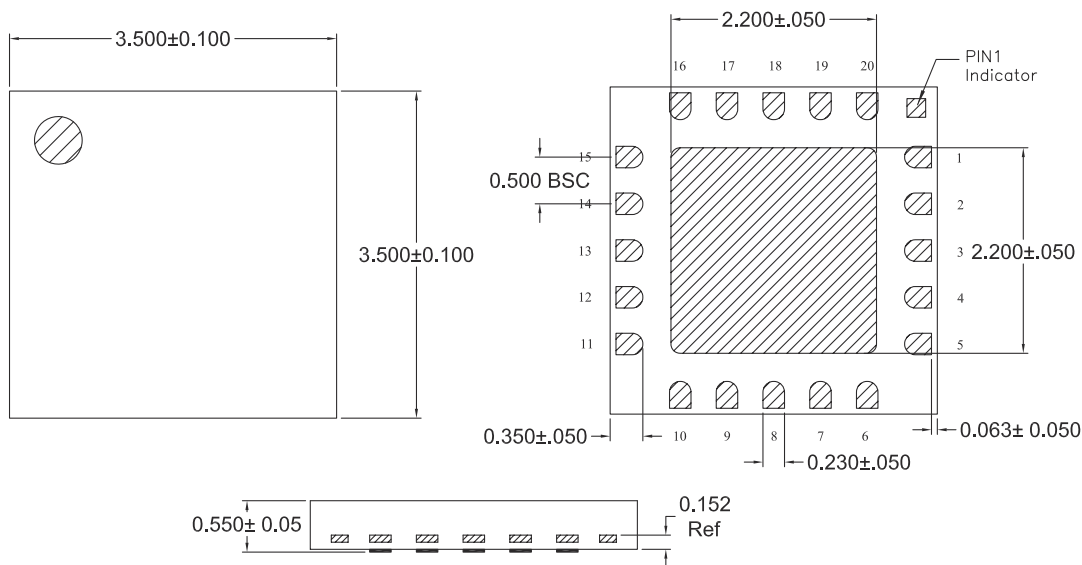
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Specifications must be met across supply voltage, control voltage, and temperature ranges unless otherwise noted. Typical conditions: T = 25 °C, V _{CC} = 3.6V
Operating Frequency Range	2400		2483	MHz	
Operating Voltage (V _{CC})	3.2	3.6	4.2	V	
TX_EN and RX_EN	2.9	3.0		V	
Leakage Current		1		uA	All control logics = Low, No RF Input
Transmit Parameters					
Frequency	2400		2483	MHz	
Input Return Loss	10				
Amplitude Imbalance	-1		1	dB	
Phase Imbalance	-10		10	deg	
Output Return Loss	10				
Gain	24	28		dB	At rated power
Gain Flatness	0.8		0.5	dB	
P1dB		27		dBm	V _{CC} = 3.6V, Temp = 25 °C. Using 802.15.4 OQPSK modulation signal
Spectral mask performance			-30	dBm	
Supply current		550		mA	P _O = 27 dBm 802.15.4 OQPSK
		380		mA	P _O = 24 dBm 802.15.4 OQPSK
Idle current		110		mA	No RF Input
Thermal Resistance		42		°C/W	4V V _{CC} , 4V V _{REG} , 27 dBm, P _{OUT} , T _{REF} = 90 °C
2nd harmonic level		-40		dBc	Measured using standard 802.15.4 OQPSK modulation signal
3rd harmonic level		-30		dBc	Measured using standard 802.15.4 OQPSK modulation signal
VSWR Stability and load mismatch susceptibility	5:1				
VSWR No damage	10:1				
Gain settling time			2	uS	
Current sourced through TX_EN pin		5	10	mA	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Receive Parameters					
Frequency	2400		2483	MHz	
Gain		10		dB	From antenna to RX pin (entire RX path).
Noise Figure		2.2	3	dB	From antenna to RX pin (entire RX path).
Current		7	15	mA	LNA + Switches
Input IP3	3	7		dBm	
Gain flatness	-0.5		0.5	dB	
Input return loss	10	12		dB	
Output return loss	10			dB	
Amplitude imbalance	-1		1	dB	
Phase imbalance	-10		10	deg	
ByPass Mode					
Frequency	2400		2483	MHz	
Insertion loss		5.5	7	dB	Entire RX path
Current		20		μA	ANT1 and ANT2
Input IP3		15		dBm	
Gain Flatness	-0.5		0.5	dB	
Input return loss	10	12		dB	
Output return loss	10			dB	
Amplitude imbalance	-1		1	dB	
Phase imbalance	-10		10	deg	
Antenna Switch					
RF-to-Control Isolation	50			dB	Measured at any control pin while in TX or RX mode.
ANT1 to ANT2 Isolation	18	20		dB	Measured from Antenna 1 to Antenna 2 port while in TX or RX mode.
Switch Control Logic = HIGH	2.8	3.1		V	All Logic I/O's
Switch Control Logic = LOW	0.0		0.4	V	All Logic I/O's
Switch Control Current. Logic HIGH		5.0	10.0	μA	All Logic I/O's
Switch Control Current. Logic LOW		0.1		μA	All Logic I/O's
Antenna Select Switch Speed			1	μS	ANT1 or ANT2 path, TX or RX mode

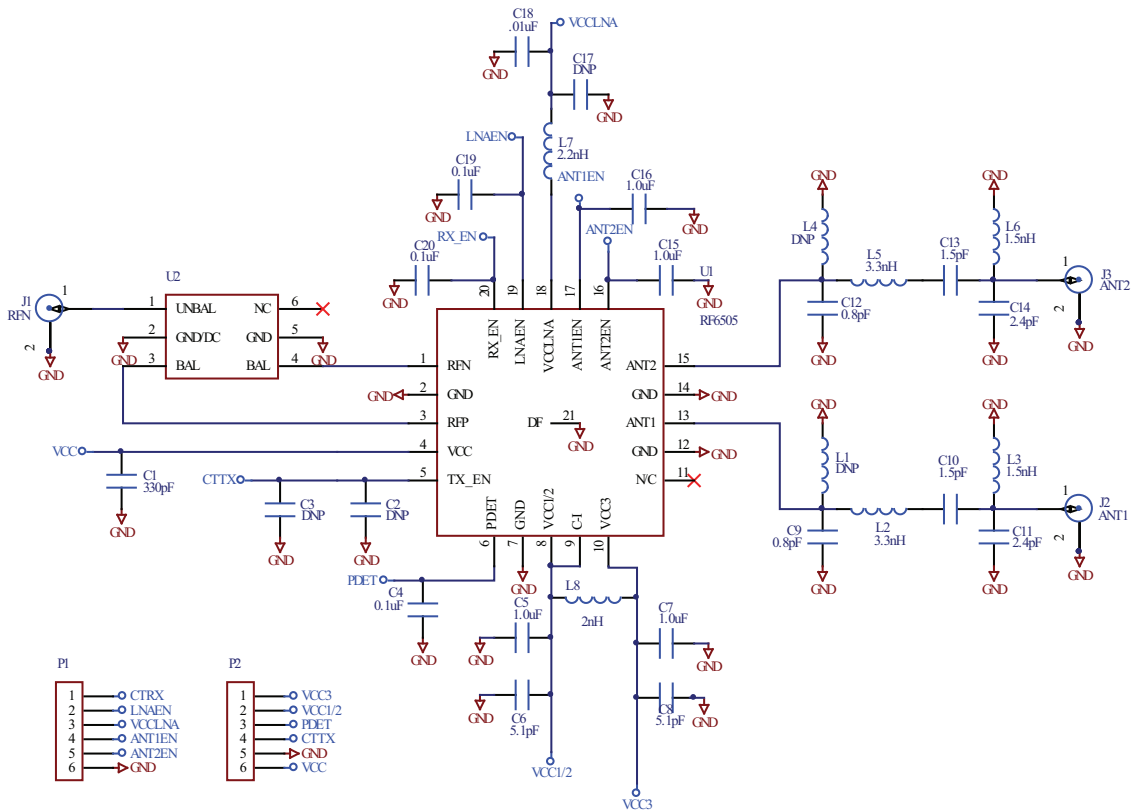
Pin	Function	Description
1	RFN	Differential RF input for PA (TX_Mode) and output for LNA (RX_Mode) internally matched to 100Ω.
2	GND	Ground.
3	RFP	Differential RF input for PA (TX_Mode) and output for LNA (RX_Mode) internally matched to 100Ω.
4	VCC	Voltage supply for VCC Bias. An external 0.1uF capacitor might be needed for low frequency decoupling.
5	TX_EN	Enable voltage pin for the PA and switch. See logic table for operation.
6	PDET	Provides and output voltage proportional to the output RF level.
7	GND	Ground.
8	VCC1/2	Voltage supply for the first and second stages of the PA. An external 1uF capacitor might be needed for low frequency decoupling.
9	C/I	This pin is connected internally (C/I) to Pin 8 therefore this pin should not be grounded. This pin should be left open.
10	VCC3	Voltage supply for the third stage of the PA. An external 1uF capacitor might be needed for low frequency decoupling.
11	NC	No connect.
12	GND	Ground.
13	ANT1	This is a common port (antenna). It is matched to 50Ω and DC block is provided internally.
14	GND	Ground.
15	ANT2	This is a common port (antenna). It is matched to 50Ω and DC block is provided internally.
16	ANT2_EN	Control pin for antenna select. See logic table for operation.
17	ANT1_EN	Control pin for antenna select. See logic table for operation.
18	VCCLNA	Voltage supply. An external 1uF capacitor might be needed for low frequency decoupling.
19	LNA_EN	LNA enable pin for selecting between High gain mode and Bypass mode.
20	RX_EN	Enable voltage pin for the Receive mode and switch. See logic table for operation.

Package Drawing



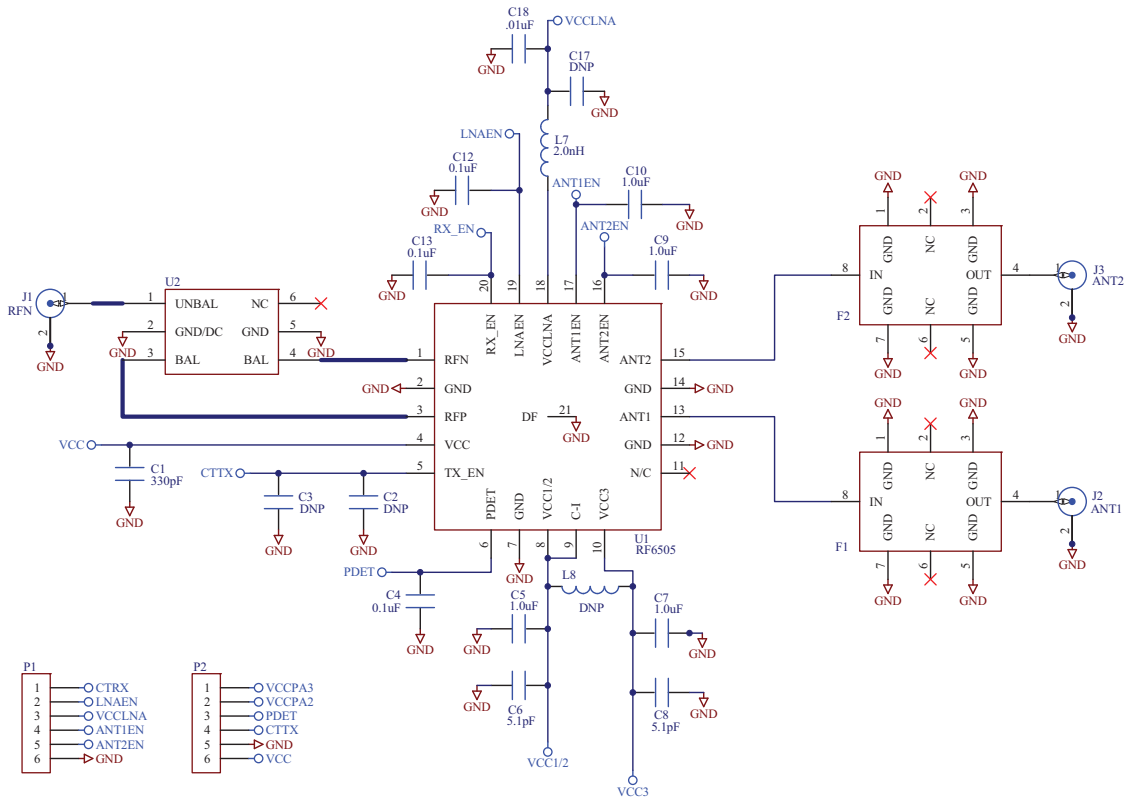
Mode	TX_EN	RX_EN	LNA_EN	ANT1_EN	ANT2_EN
Tx, Antenna 1	High	Low	Low	High	Low
Tx, Antenna 2	High	Low	Low	Low	High
Rx, Antenna 1	Low	High	High	High	Low
Rx, Antenna 2	Low	High	High	Low	High
Rx, Antenna 1, LNA Bypass	Low	High	Low	High	Low
Rx, Antenna 2, LNA Bypass	Low	High	Low	Low	High

Evaluation Board Schematic



*Note: Pin 9 is connected internally (C/I) to Pin 8 therefore this pin should not be grounded. This pin should be left open.

Evaluation Board Schematic with Murata Filter



RF6505 2.4GHz Front End Module

