

# PCF8574A Remote 8-Bit I/O Expander for I<sup>2</sup>C Bus

## 1 Features

- Low Standby-Current Consumption of 10  $\mu$ A Max
- I<sup>2</sup>C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## 2 Applications

- Telecom Shelters: Filter Units
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics
- Industrial Automation
- Products with GPIO-Limited Processors

## 3 Description

This 8-bit input/output (I/O) expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.5-V to 6-V V<sub>CC</sub> operation.

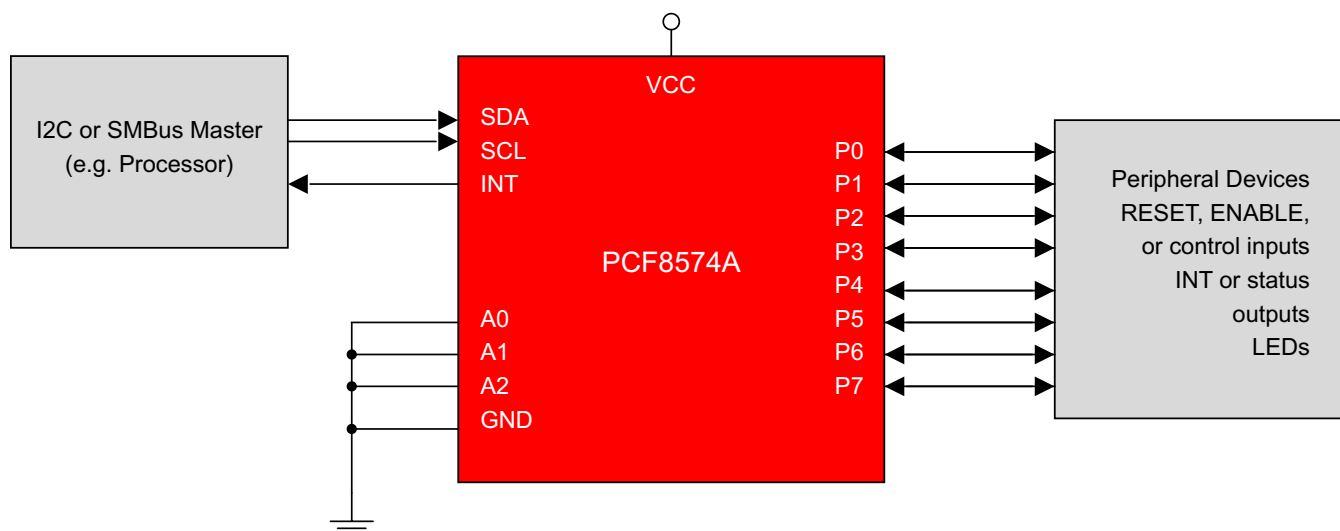
The PCF8574A device provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V<sub>CC</sub> is active.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
PCF8574A	VQFN (20)	4.50 mm × 3.50 mm
	PDIP (16)	19.30 mm × 6.35 mm
	SOIC (16)	10.30 mm × 7.50 mm
	TSSOP (20)	6.50 mm × 4.40 mm
	TVSOP (20)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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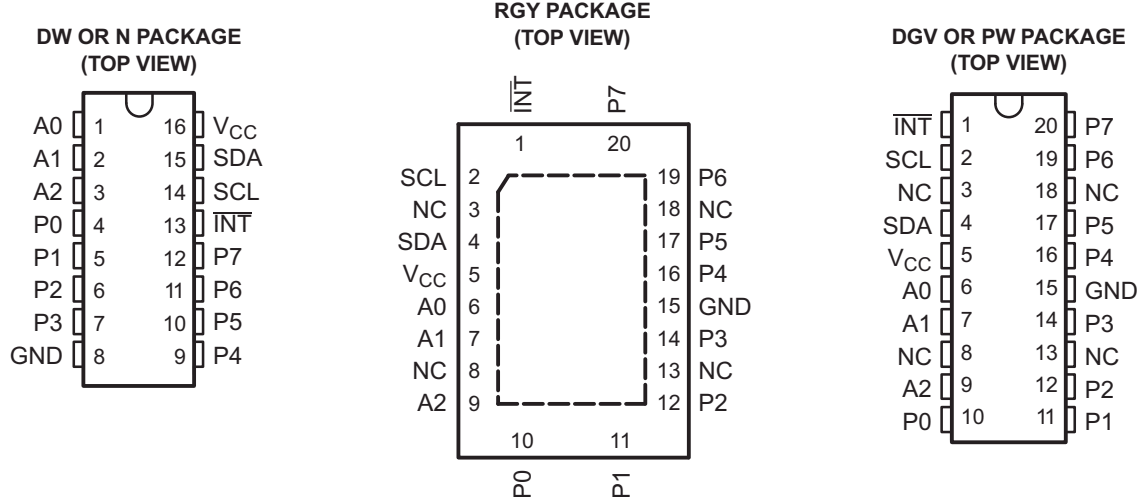
## 4 Revision History

### Changes from Revision D (October 2005) to Revision E

Page

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**
- Deleted *Ordering Information* table. .... **1**

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN			TYPE	DESCRIPTION
	RGY	DGV or PW	DW or N		
A[0..2]	6, 7, 9	6, 7, 9	1, 2, 3	I	Address inputs 0 through 2. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.
GND	15	15	8	—	Ground
INT	1	1	13	O	Interrupt output. Connect to V <sub>CC</sub> through a pullup resistor.
NC	3, 8, 13, 18	3, 8, 13, 18	-	—	Do not connect
P[0..7]	10, 11, 12, 14, 16, 17, 19, 20	10, 11, 12, 14, 16, 17, 19, 20	4, 5, 6, 7, 9, 10, 11, 12	I/O	P-port input/output. Push-pull design structure.
SCL	2	2	14	I	Serial clock line. Connect to V <sub>CC</sub> through a pullup resistor
SDA	4	4	15	I/O	Serial data line. Connect to V <sub>CC</sub> through a pullup resistor.
V <sub>CC</sub>	5	5	16	—	Voltage supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	$V_{CC} + 0.5$	V
$V_O$	Output voltage range <sup>(2)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	–20	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–20	mA
$I_{OK}$	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$	±400	µA
$I_{OL}$	Continuous output low current	$V_O = 0$ to $V_{CC}$	50	mA
$I_{OH}$	Continuous output high current	$V_O = 0$ to $V_{CC}$	–4	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.5	6	V
$V_{IH}$	High-level input voltage	$0.7 \times V_{CC}$	$V_{CC} + 0.5$	V
$V_{IL}$	Low-level input voltage	–0.5	$0.3 \times V_{CC}$	V
$I_{OH}$	High-level output current		–1	mA
$I_{OL}$	Low-level output current		25	mA
$T_A$	Operating free-air temperature	–40	85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PCF8574A					UNIT
		DGV	DW	N	PW	RGY	
		20 PINS	16 PINS	16 PINS	20 PINS	20 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	92	57	67	83	37	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = –18 mA	2.5 V to 6 V	–1.2			V
V <sub>POR</sub>	Power-on reset voltage <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	6 V		1.3	2.4	V
I <sub>OH</sub>	P port	V <sub>O</sub> = GND	2.5 V to 6 V	30		300	μA
I <sub>OHT</sub>	P-port transient pullup current	High during acknowledge, V <sub>OH</sub> = GND	2.5 V		–1		mA
I <sub>OL</sub>	SDA	V <sub>O</sub> = 0.4 V	2.5 V to 6 V	3			mA
	P port	V <sub>O</sub> = 1 V	5 V	10	25		
	$\overline{\text{INT}}$	V <sub>O</sub> = 0.4 V	2.5 V to 6 V	1.6			
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V			±5	μA
	$\overline{\text{INT}}$					±5	
	A0, A1, A2					±5	
I <sub>IHL</sub>	P port	V <sub>I</sub> ≥ V <sub>CC</sub> or V <sub>I</sub> ≤ GND	2.5 V to 6 V			±400	μA
I <sub>CC</sub>	Operating mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 100 kHz	6 V		40	100	μA
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0			2.5	10	
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V		1.5	7	pF
C <sub>io</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The power-on reset circuit resets the I<sup>2</sup>C-bus logic with V<sub>CC</sub> < V<sub>POR</sub> and sets all I/Os to logic high (with current source to V<sub>CC</sub>).

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 12)

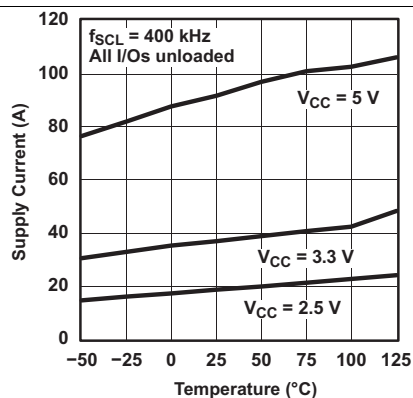
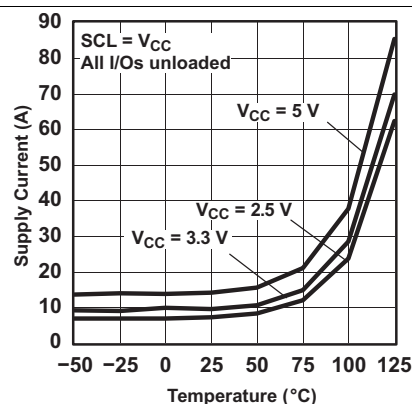
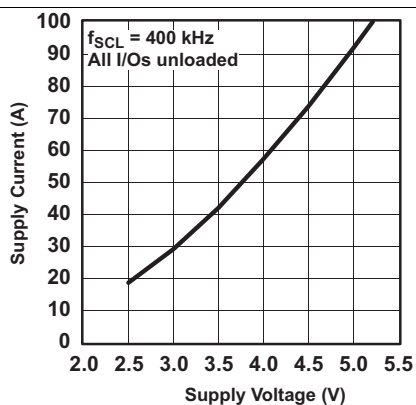
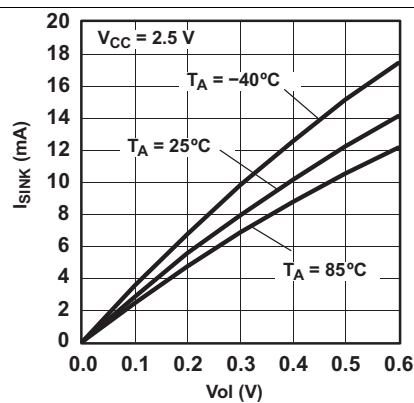
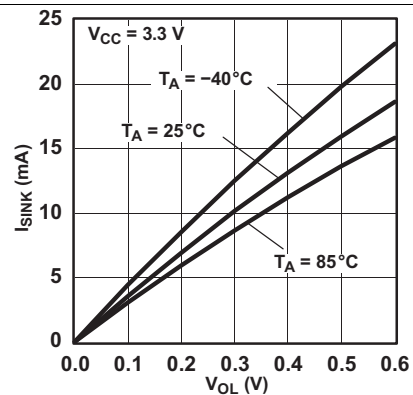
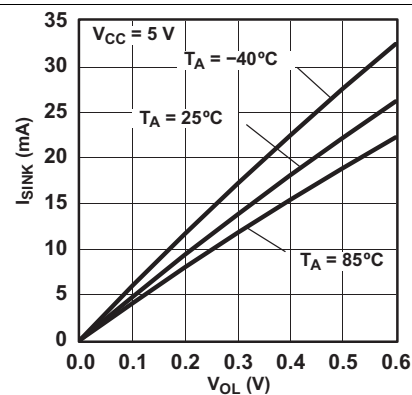
			MIN	MAX	UNIT
f <sub>scl</sub>	I <sup>2</sup> C clock frequency		100		kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time		4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time		4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		100		ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time		250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time		0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1		μs
t <sub>icf</sub>	I <sup>2</sup> C input fall time		0.3		μs
t <sub>ocf</sub>	I <sup>2</sup> C output fall time (10-pF to 400-pF bus)		300		ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start		4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup		4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold		4		μs
t <sub>sps</sub>	I <sup>2</sup> C stop-condition setup		4		μs
t <sub>vd</sub>	Valid-data time	SCL low to SDA output valid	3.4		μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400		pF

## 6.7 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pv</sub>	Output data valid	SCL		4	μs
t <sub>su</sub>	Input data setup time	P port		0	μs
t <sub>h</sub>	Input data hold time	SCL	4		μs
t <sub>iv</sub>	Interrupt valid time	P port		4	μs
t <sub>ir</sub>	Interrupt reset delay time	$\overline{\text{INT}}$		4	μs

## 6.8 Typical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

**Figure 1. Supply Current vs Temperature**

**Figure 2. Standby Supply Current vs Temperature**

**Figure 3. Supply Current vs Supply Voltage**

**Figure 4. I/O Sink Current vs Output Low Voltage**

**Figure 5. I/O Sink Current vs Output Low Voltage**

**Figure 6. I/O Sink Current vs Output Low Voltage**

## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

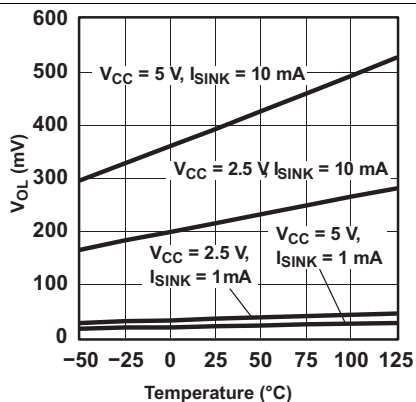


Figure 7. I/O Output Low Voltage vs Temperature

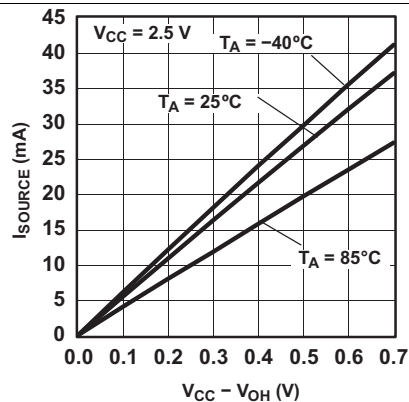


Figure 8. I/O Source Current vs Output High Voltage

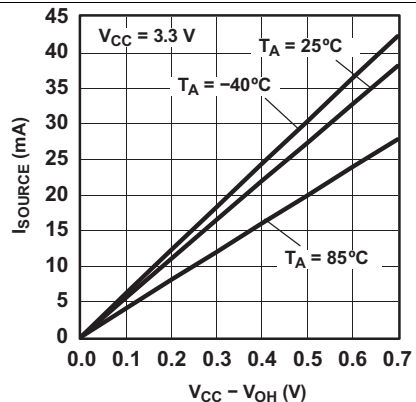


Figure 9. I/O Source Current vs Output High Voltage

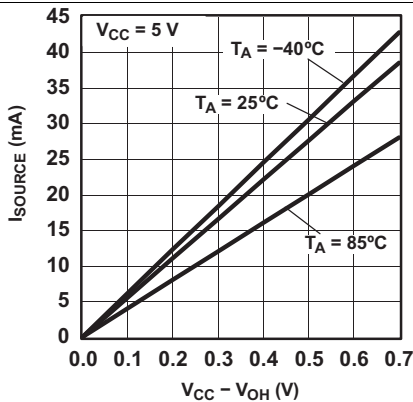


Figure 10. I/O Source Current vs Output High Voltage

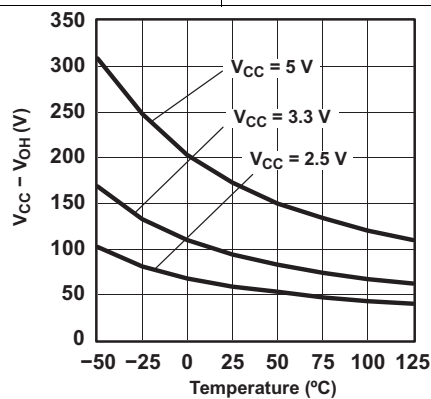
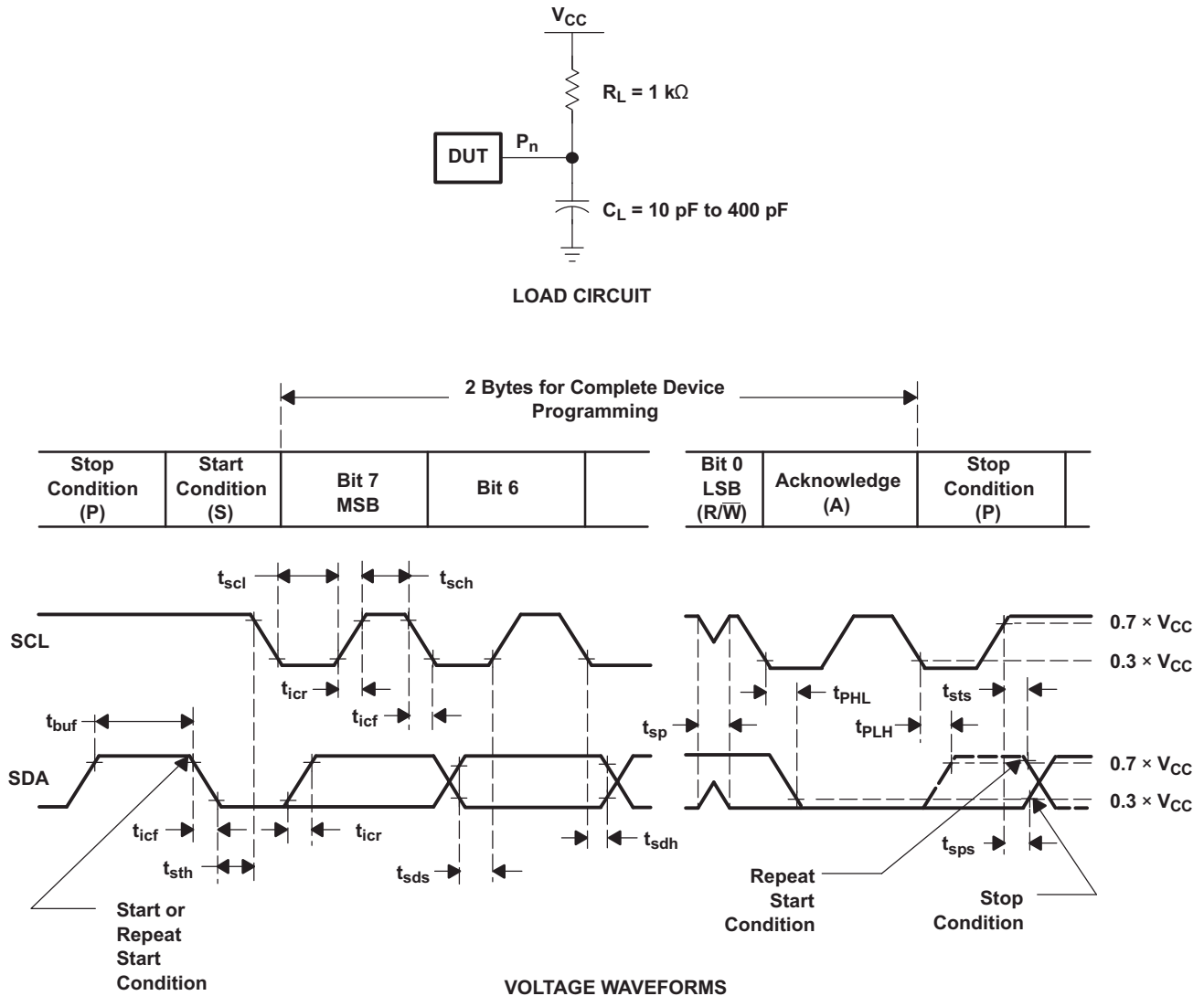


Figure 11. I/O High Voltage vs Temperature

## 7 Parameter Measurement Information



**Figure 12. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms**



## Parameter Measurement Information (continued)

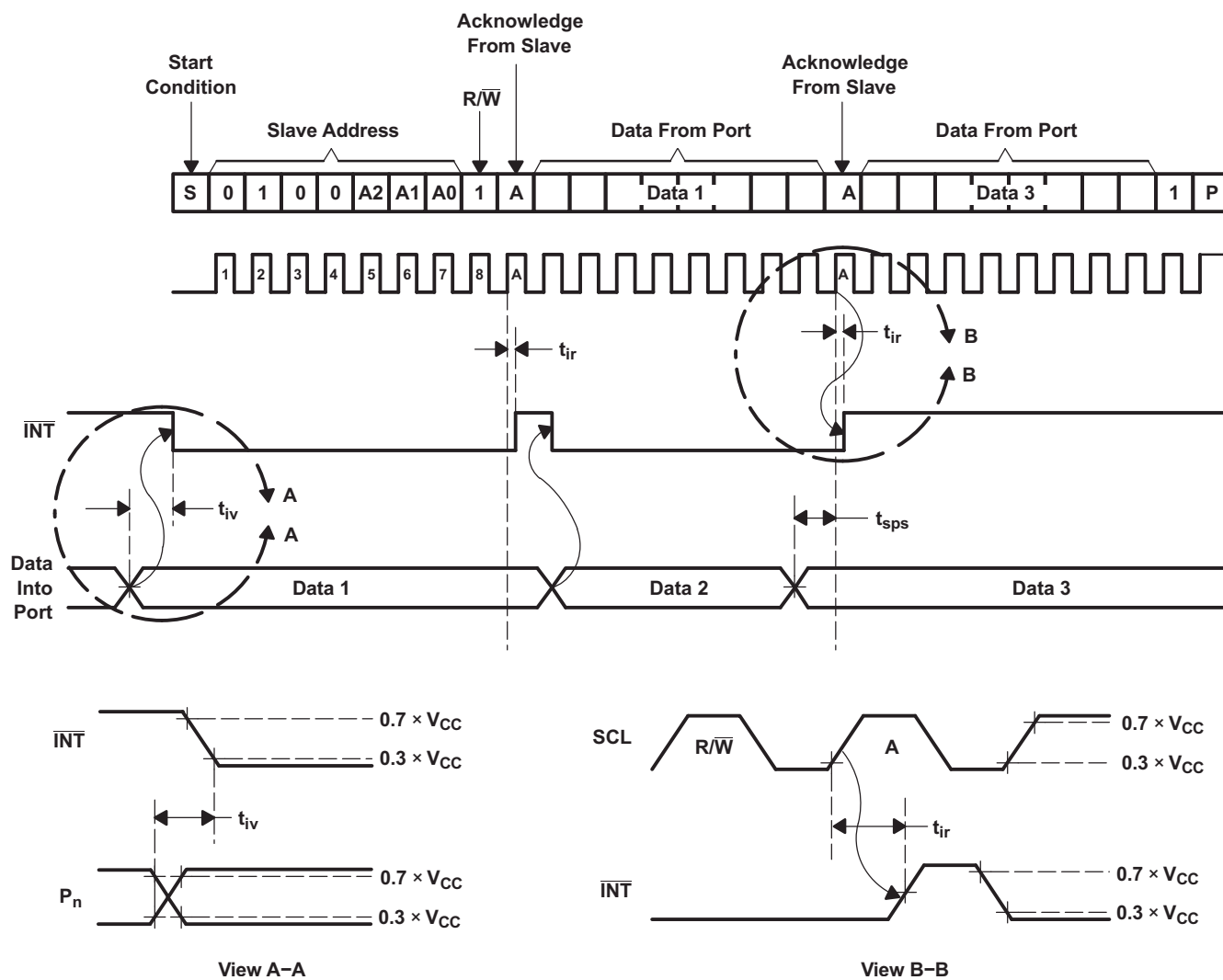


Figure 13. Interrupt Voltage Waveforms

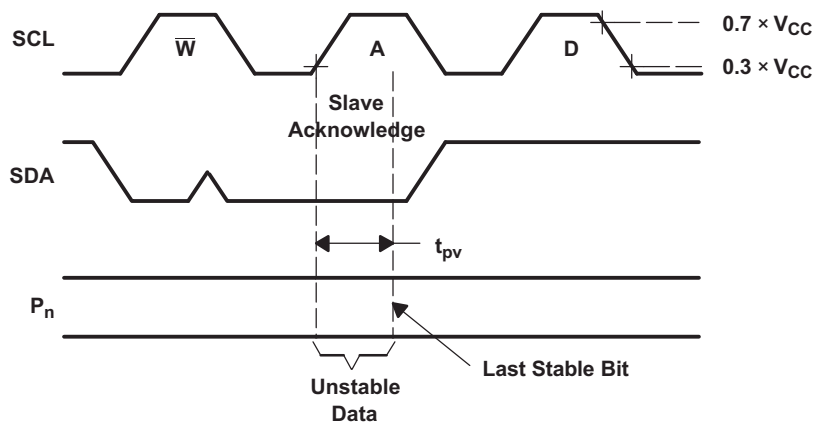
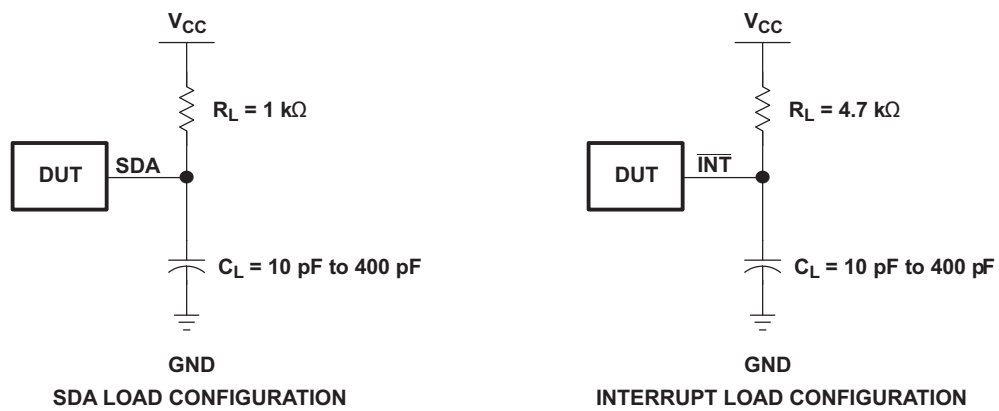


Figure 14. I<sup>2</sup>C Write Voltage Waveforms

**Parameter Measurement Information (continued)**

**Figure 15. Load Circuits**

## 8 Detailed Description

### 8.1 Overview

The PCF8574A device provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface [serial clock (SCL), serial data (SDA)].

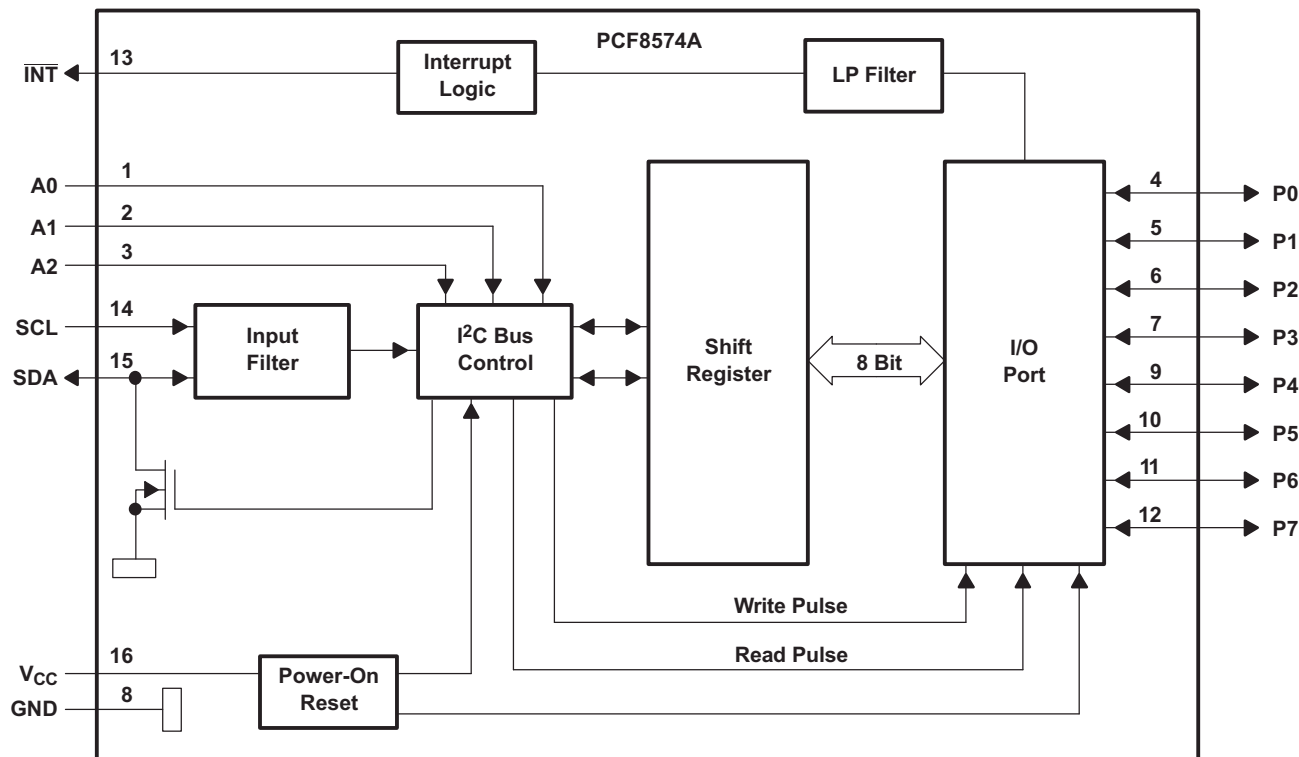
The device features an 8-bit quasi-bidirectional I/O port (P0–P7), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to V<sub>CC</sub> is active. An additional strong pullup to V<sub>CC</sub> allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

The PCF8574A device provides an open-drain output ( $\overline{\text{INT}}$ ) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t<sub>iv</sub>,  $\overline{\text{INT}}$  is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal, or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as  $\overline{\text{INT}}$ . Reading from, or writing to, another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Therefore, the PCF8574A device can remain a simple slave device.

### 8.2 Functional Block Diagram

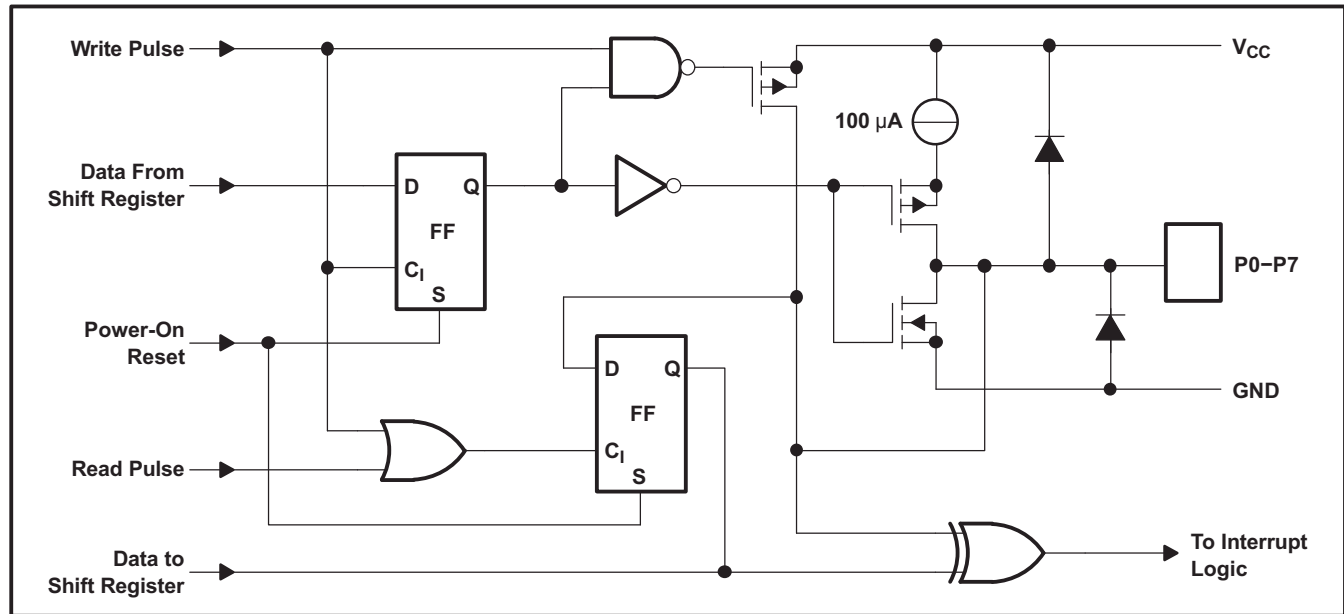
#### 8.2.1 Simplified Block Diagram of Device



Pin numbers shown are for the DW and N packages.

## Functional Block Diagram (continued)

### 8.2.2 Simplified Schematic Diagram of Each P-Port Input/Output



## 8.3 Feature Description

### 8.3.1 I<sup>2</sup>C Interface

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the R/W bit is high, the data from this device are the values read from the P port. If the R/W bit is low, the data are from the master, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time,  $t_{pv}$ , after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master.

### 8.3.2 Interface Definition

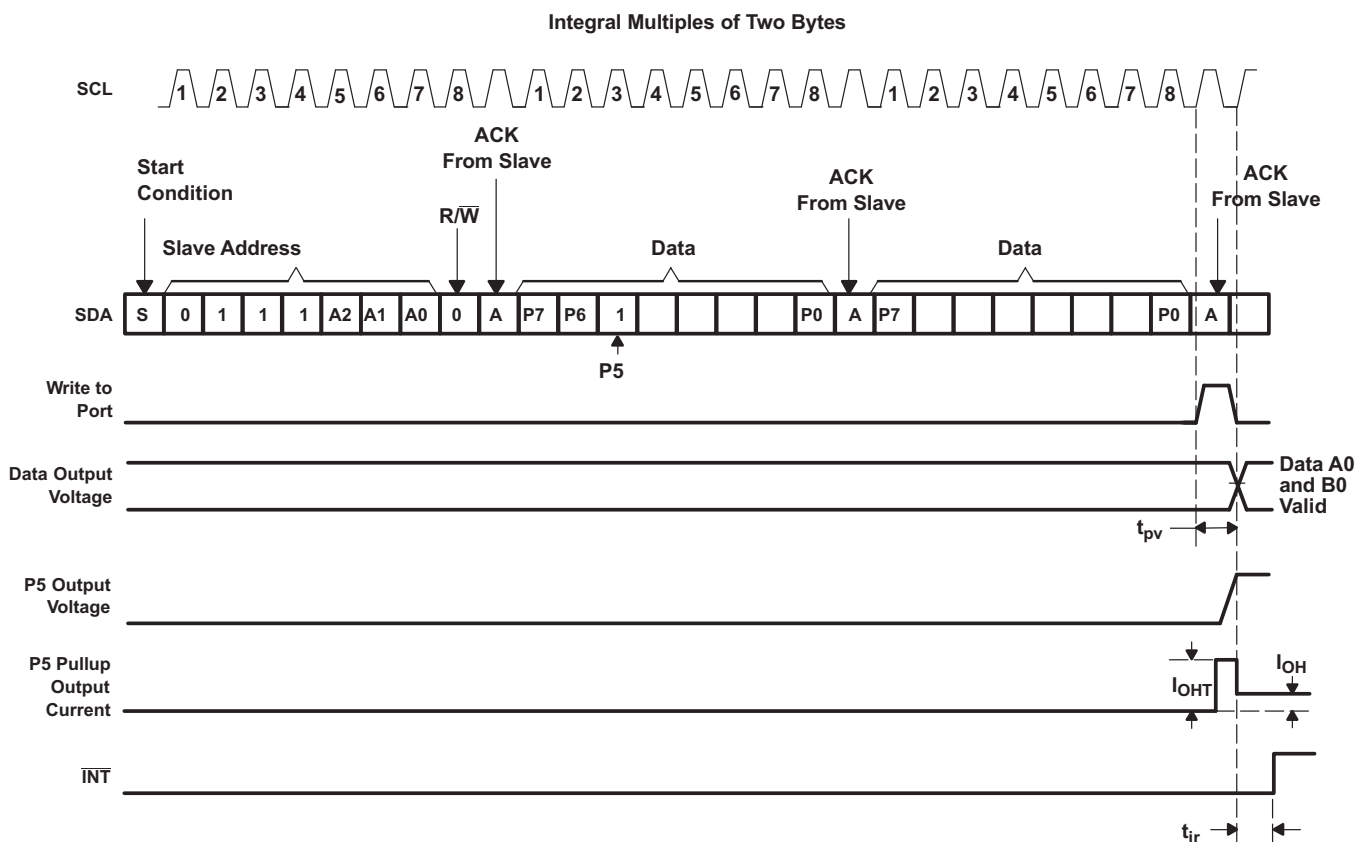
BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	H	H	H	A2	A1	A0	R/W
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

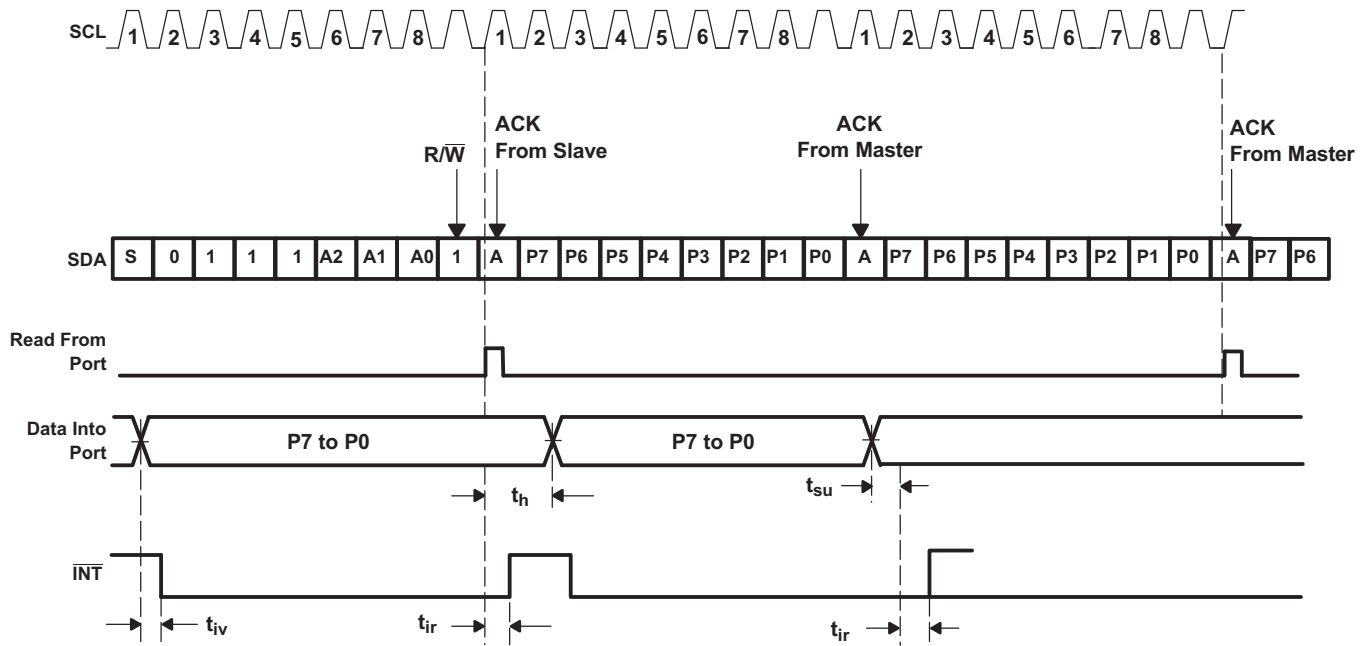
### 8.3.3 Address Reference

INPUTS			I <sup>2</sup> C BUS SLAVE 8-BIT READ ADDRESS	I <sup>2</sup> C BUS SLAVE 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	113 (dec), 71 (hex)	112 (dec), 70 (hex)
L	L	H	115 (dec), 73 (hex)	114 (dec), 72 (hex)
L	H	L	117 (dec), 75 (hex)	116 (dec), 74 (hex)
L	H	H	119 (dec), 77 (hex)	118 (dec), 76 (hex)
H	L	L	121 (dec), 79 (hex)	120 (dec), 78 (hex)
H	L	H	123 (dec), 7B (hex)	122 (dec), 7A (hex)
H	H	L	125 (dec), 7D (hex)	124 (dec), 7C (hex)
H	H	H	127 (dec), 7F (hex)	126 (dec), 7E (hex)

### 8.4 Device Functional Modes

Figure 16 and Figure 17 show the address and timing diagrams for the write and read modes, respectively.



**Device Functional Modes (continued)**


- A. A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

**Figure 17. Read Mode (Input)**

## 9 Application and Implementation

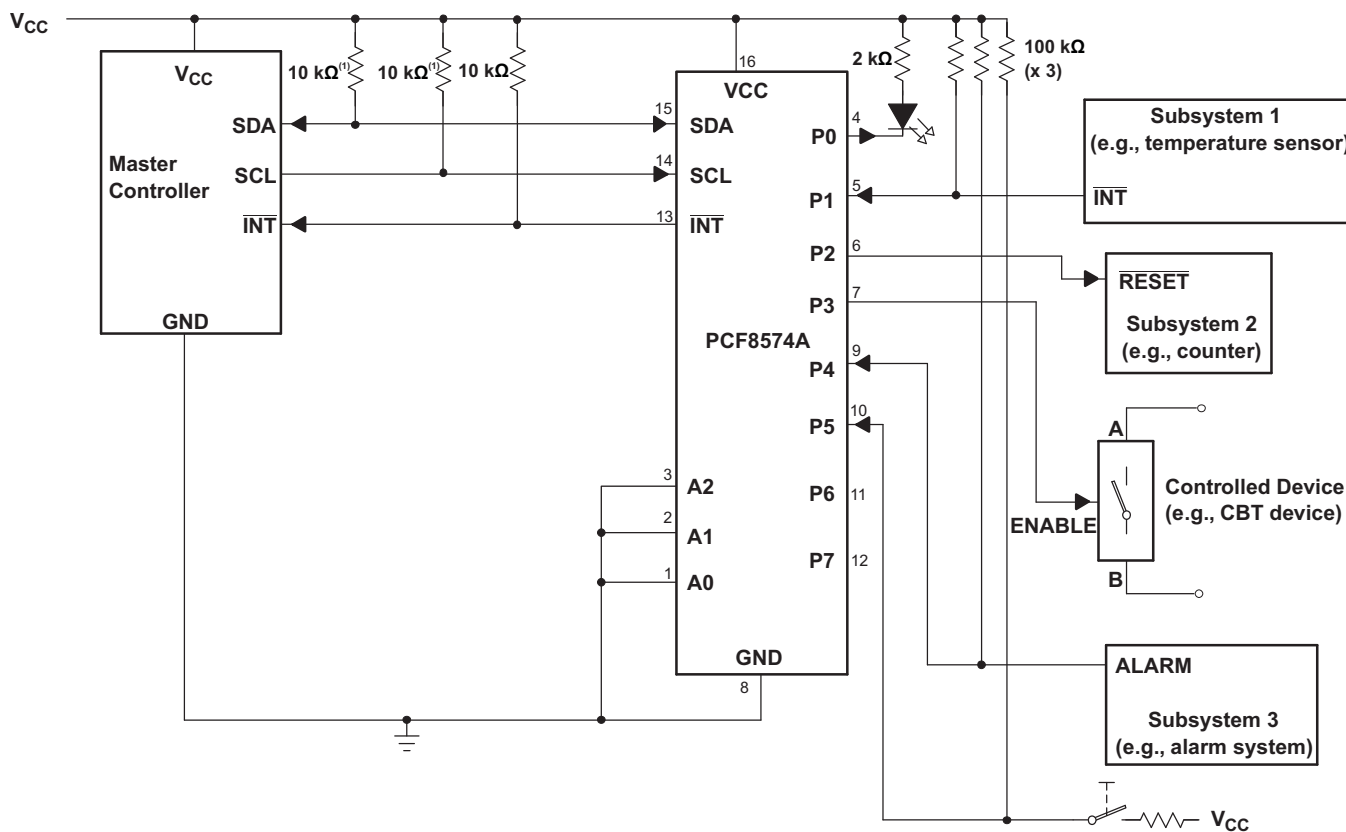
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Figure 18 shows an application in which the PCF8574A device can be used.

### 9.2 Typical Application



- (1) The SCL and SDA pins must be pulled up to  $V_{CC}$  because if SCL and SDA are pulled up to an auxiliary power supply that could be powered on while  $V_{CC}$  is powered off, then the supply current,  $I_{CC}$ , will increase as a result.
- A. Device address is configured as 0100000 for this example.
- B. P0, P2, and P3 are configured as outputs.
- C. P1, P4, and P5 are configured as inputs.
- D. P6 and P7 are not used and must be configured as outputs.

**Figure 18. Application Schematic**

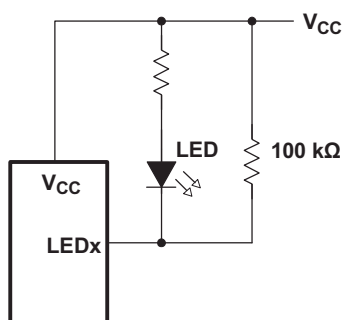
## Typical Application (continued)

### 9.2.1 Design Requirements

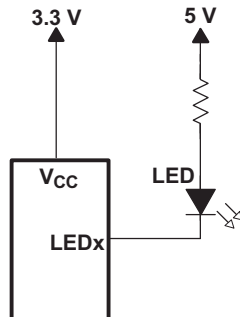
#### 9.2.1.1 Minimizing $I_{CC}$ When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to  $V_{CC}$  through a resistor as shown in Figure 27. For a P-port configured as an input,  $I_{CC}$  increases as  $V_I$  becomes lower than  $V_{CC}$ . The LED is a diode, with threshold voltage  $V_T$ , and when a P-port is configured as an input the LED will be off but  $V_I$  is a  $V_T$  drop below  $V_{CC}$ .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to  $V_{CC}$  when the P-ports are configured as input to minimize current consumption. Figure 19 shows a high-value resistor in parallel with the LED. Figure 20 shows  $V_{CC}$  less than the LED supply voltage by at least  $V_T$ . Both of these methods maintain the I/O  $V_I$  at or above  $V_{CC}$  and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.



**Figure 19. High-Value Resistor in Parallel With LED**



**Figure 20. Device Supplied by a Lower Voltage**



## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

The pull-up resistors,  $R_p$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

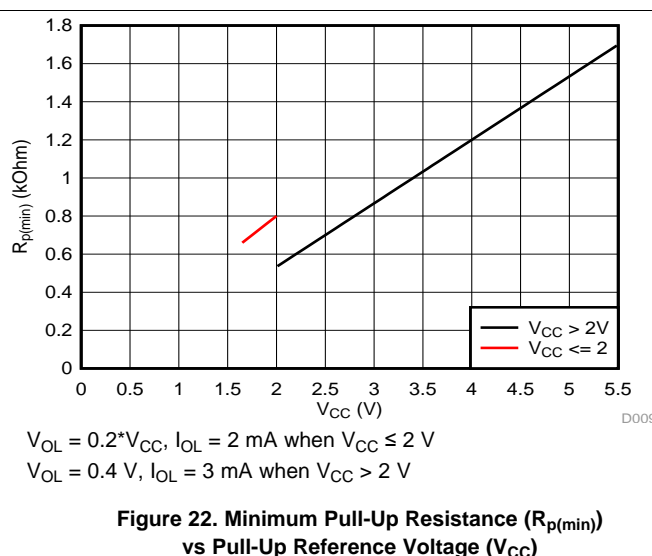
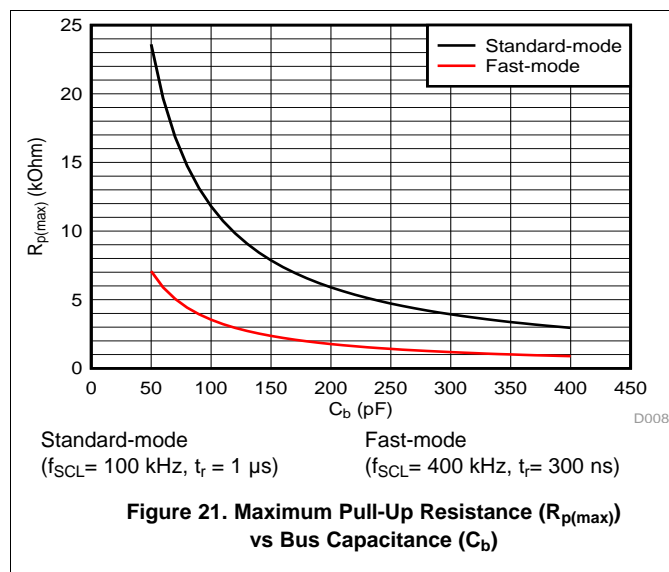
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8574A device,  $C_i$  for SCL or  $C_{i0}$  for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

### 9.2.3 Application Curves

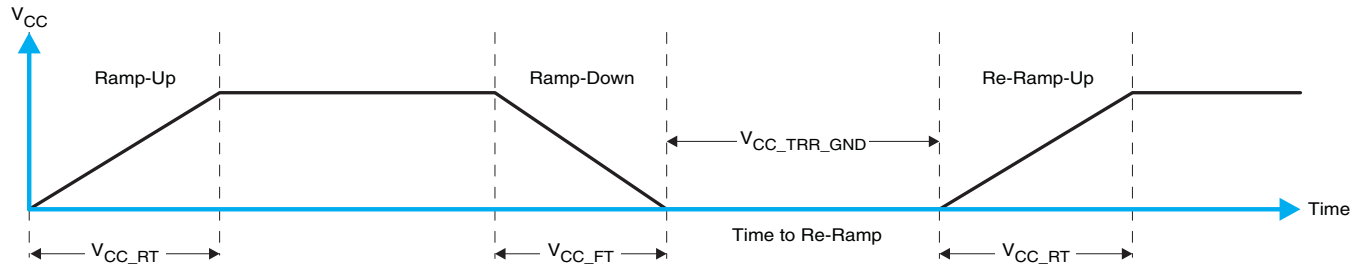


## 10 Power Supply Recommendations

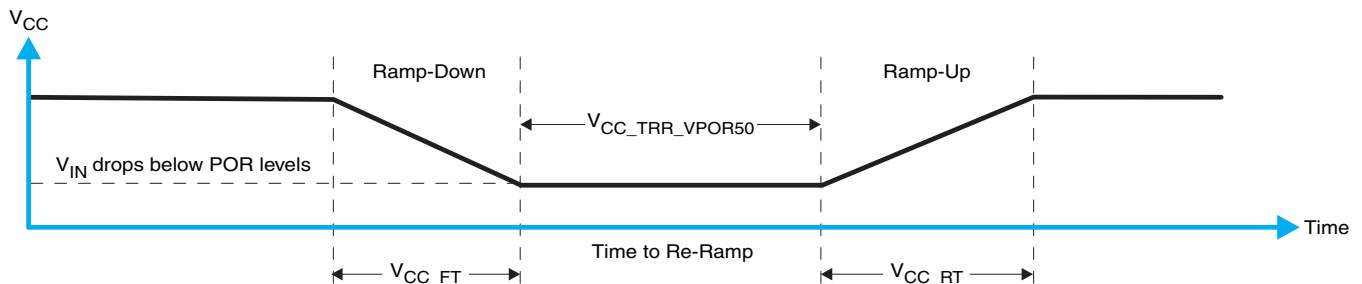
### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCF8574A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 23](#) and [Figure 24](#).



**Figure 23.  $V_{CC}$  is Lowered Below 0.2 V or 0 V and Then Ramped Up to  $V_{CC}$**



**Figure 24.  $V_{CC}$  is Lowered Below the POR Threshold, Then Ramped Back Up to  $V_{CC}$**

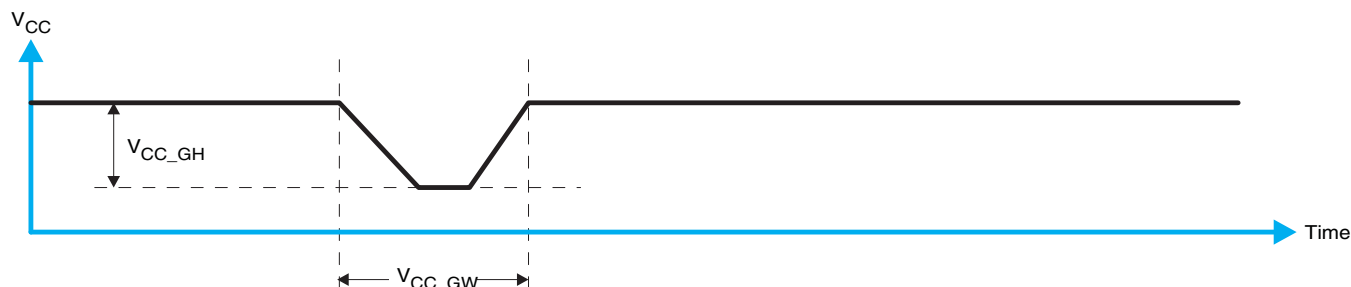
[Table 1](#) specifies the performance of the power-on reset feature for PCF8574A for both types of power-on reset.

**Table 1. Recommended Supply Sequencing and Ramp Rates<sup>(1)</sup>**

PARAMETER			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See <a href="#">Figure 23</a>	1		100	ms
$V_{CC\_RT}$	Rise rate	See <a href="#">Figure 23</a>	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when $V_{CC}$ drops to GND)	See <a href="#">Figure 23</a>	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV)	See <a href="#">Figure 24</a>	0.001			ms
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s	See <a href="#">Figure 25</a>			1.2	V
$V_{CC\_GW}$	Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCX}$	See <a href="#">Figure 25</a>				$\mu$ s
$V_{PORF}$	Voltage trip point of POR on falling $V_{CC}$		0.767		1.144	V
$V_{PORR}$	Voltage trip point of POR on rising $V_{CC}$		1.033		1.428	V

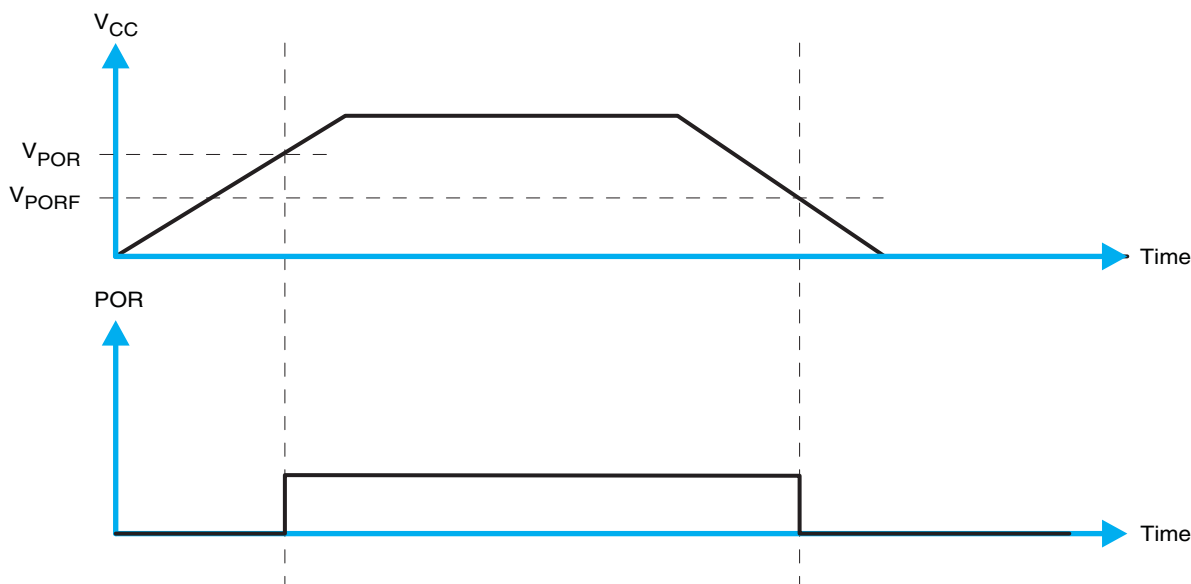
(1)  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 25 and Table 1 provide more information on how to measure these specifications.



**Figure 25. Glitch Width and Glitch Height**

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 26 and Table 1 provide more details on this specification.



**Figure 26.  $V_{POR}$**

## 11 Layout

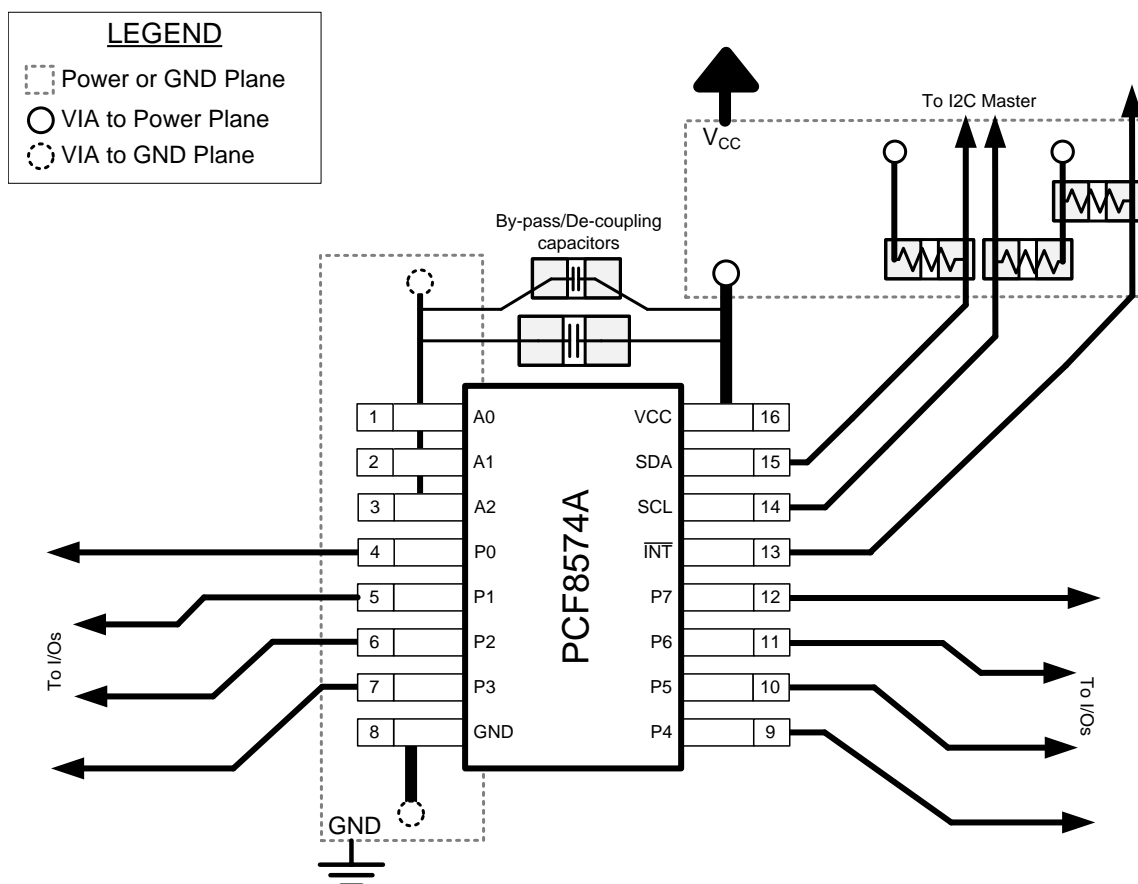
### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of PCF8574A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the  $V_{CC}$  pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8574A device as possible. These best practices are shown in Figure 27.

For the layout example provided in Figure 27, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power ( $V_{CC}$ ) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to  $V_{CC}$  or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 27.

### 11.2 Layout Example



**Figure 27. Layout Example for PCF8574A**

## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8574ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	<a href="#">Samples</a>
PCF8574ADWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	<a href="#">Samples</a>
PCF8574ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574A	<a href="#">Samples</a>
PCF8574ADWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	PCF8574A	<a href="#">Samples</a>
PCF8574ADWRE4	ACTIVE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
PCF8574ADWRG4	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85		
PCF8574AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574AN	<a href="#">Samples</a>
PCF8574ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574AN	<a href="#">Samples</a>
PCF8574APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574APWE4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
PCF8574APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574A	<a href="#">Samples</a>
PCF8574ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8574ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8574ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8574ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCF8574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCF8574ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8574ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
PCF8574ADWR	SOIC	DW	16	2000	366.0	364.0	50.0
PCF8574APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
PCF8574ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

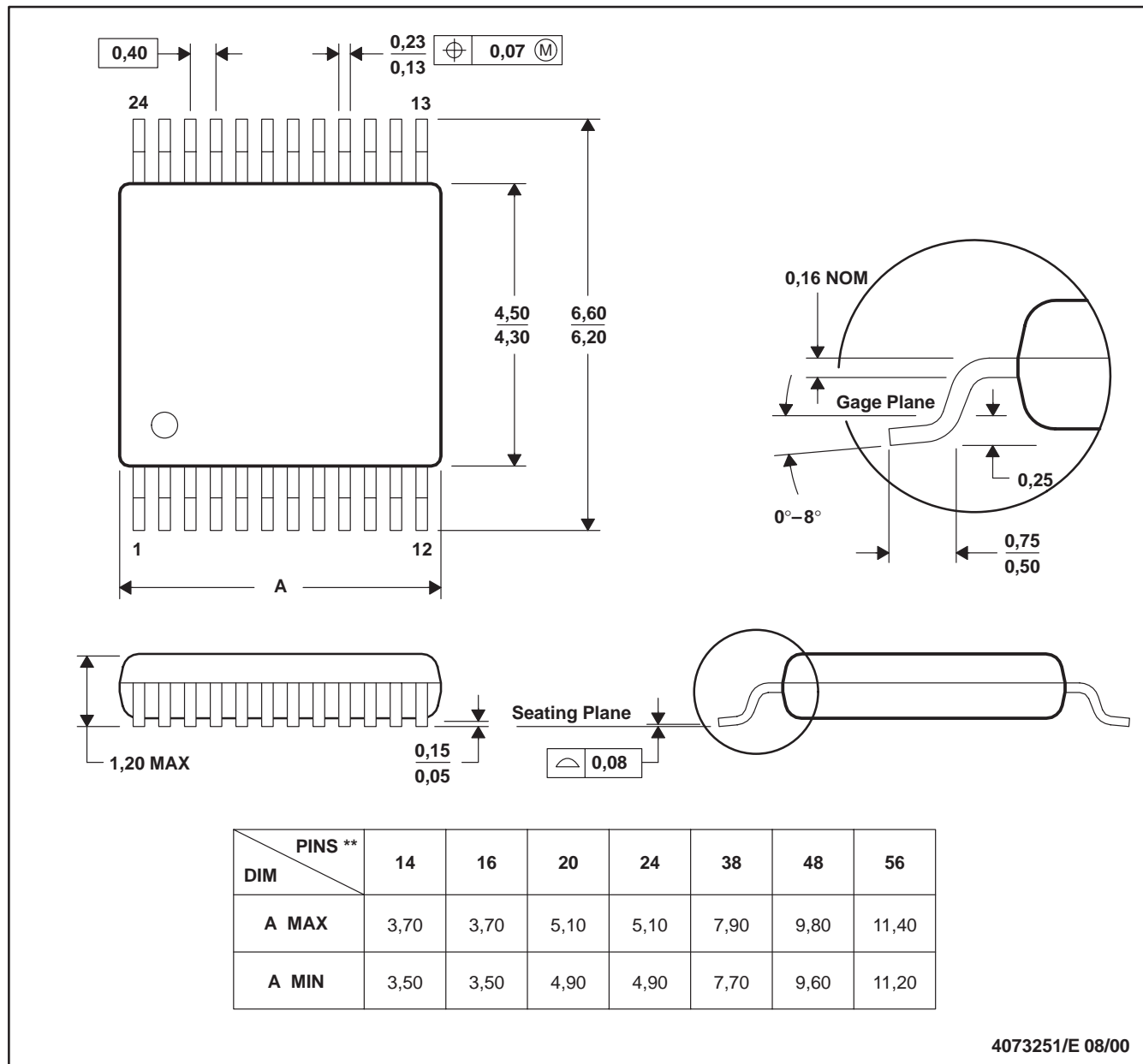
NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



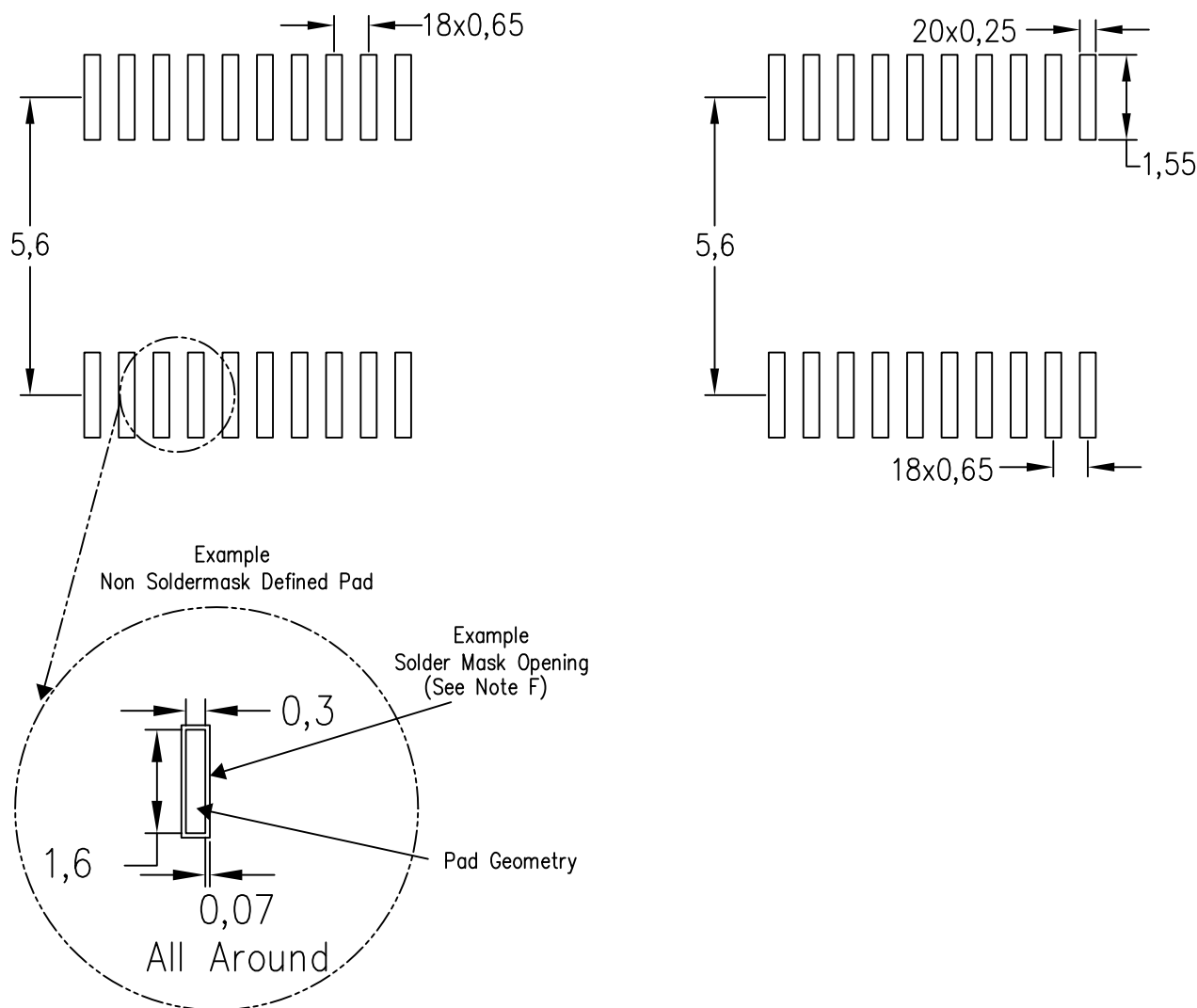
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).

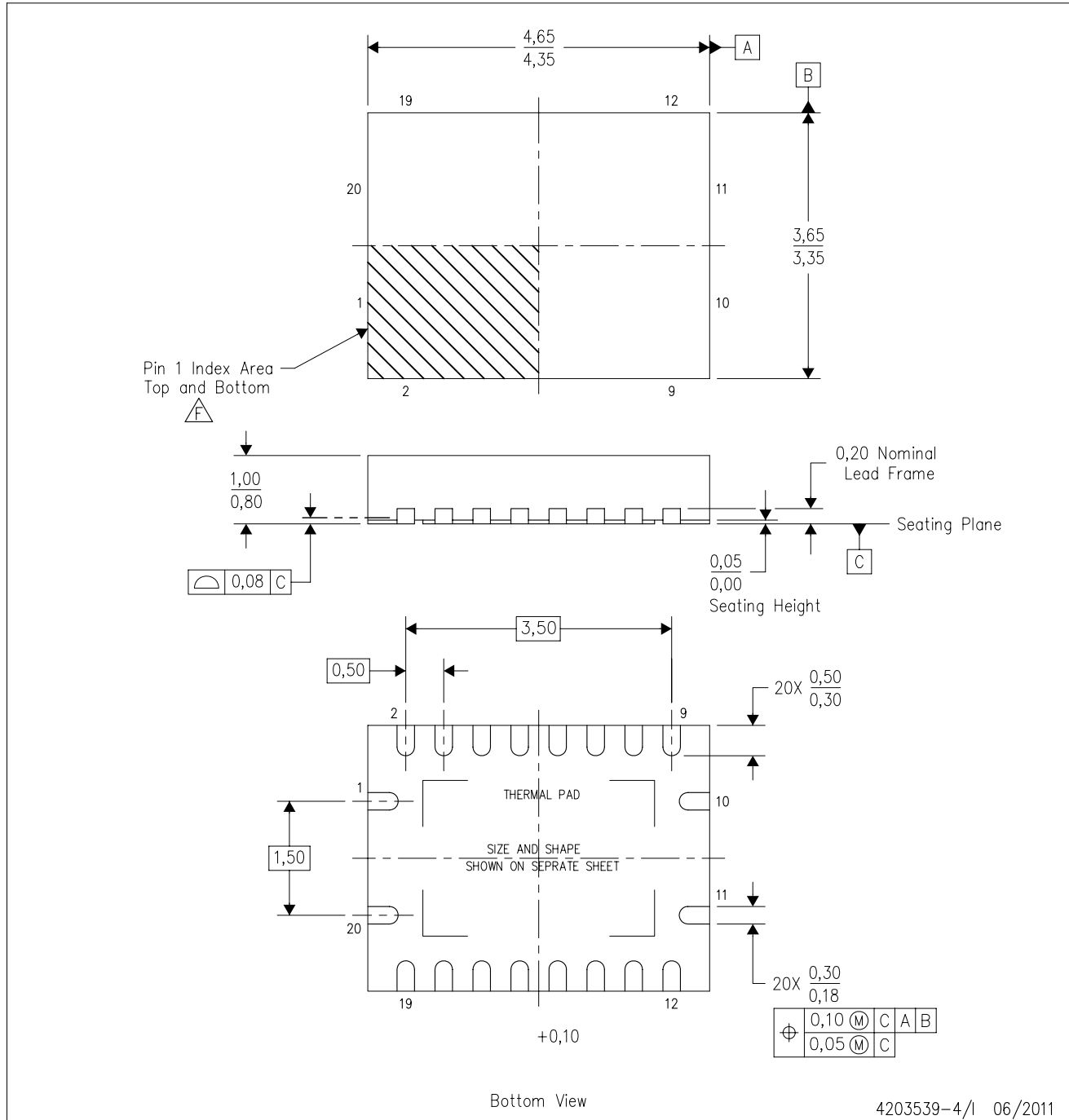


4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-4/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

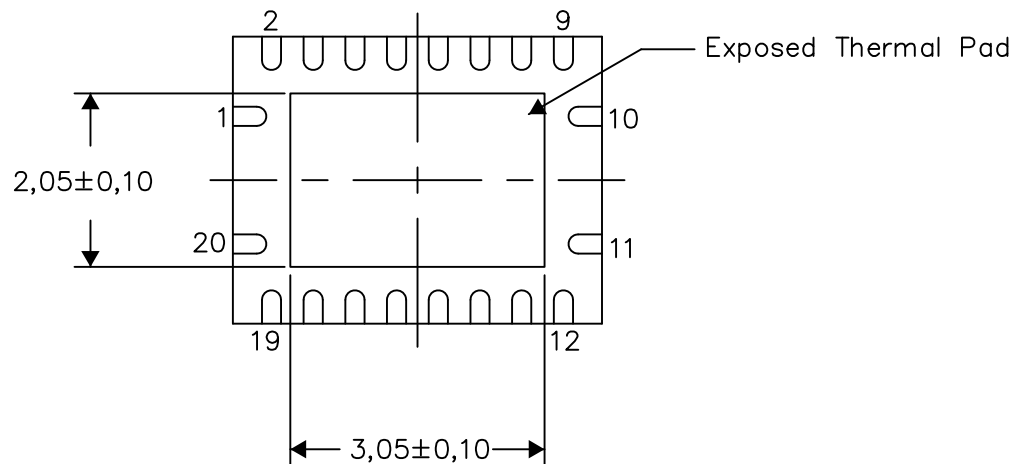
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

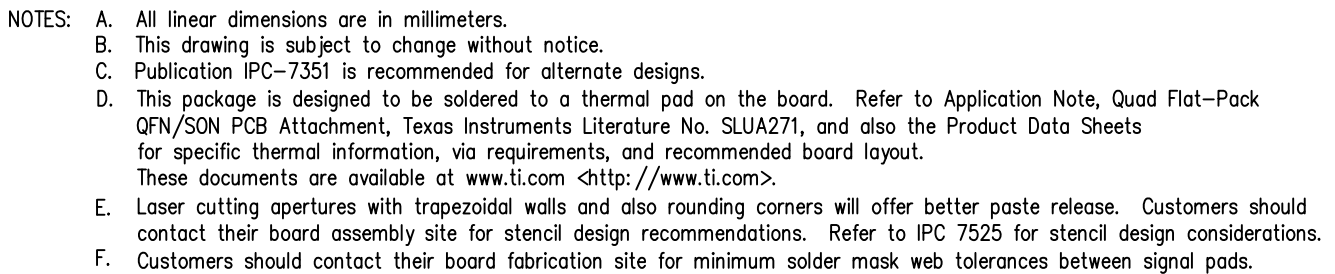


Bottom View

Exposed Thermal Pad Dimensions

4206353-4/P 03/14

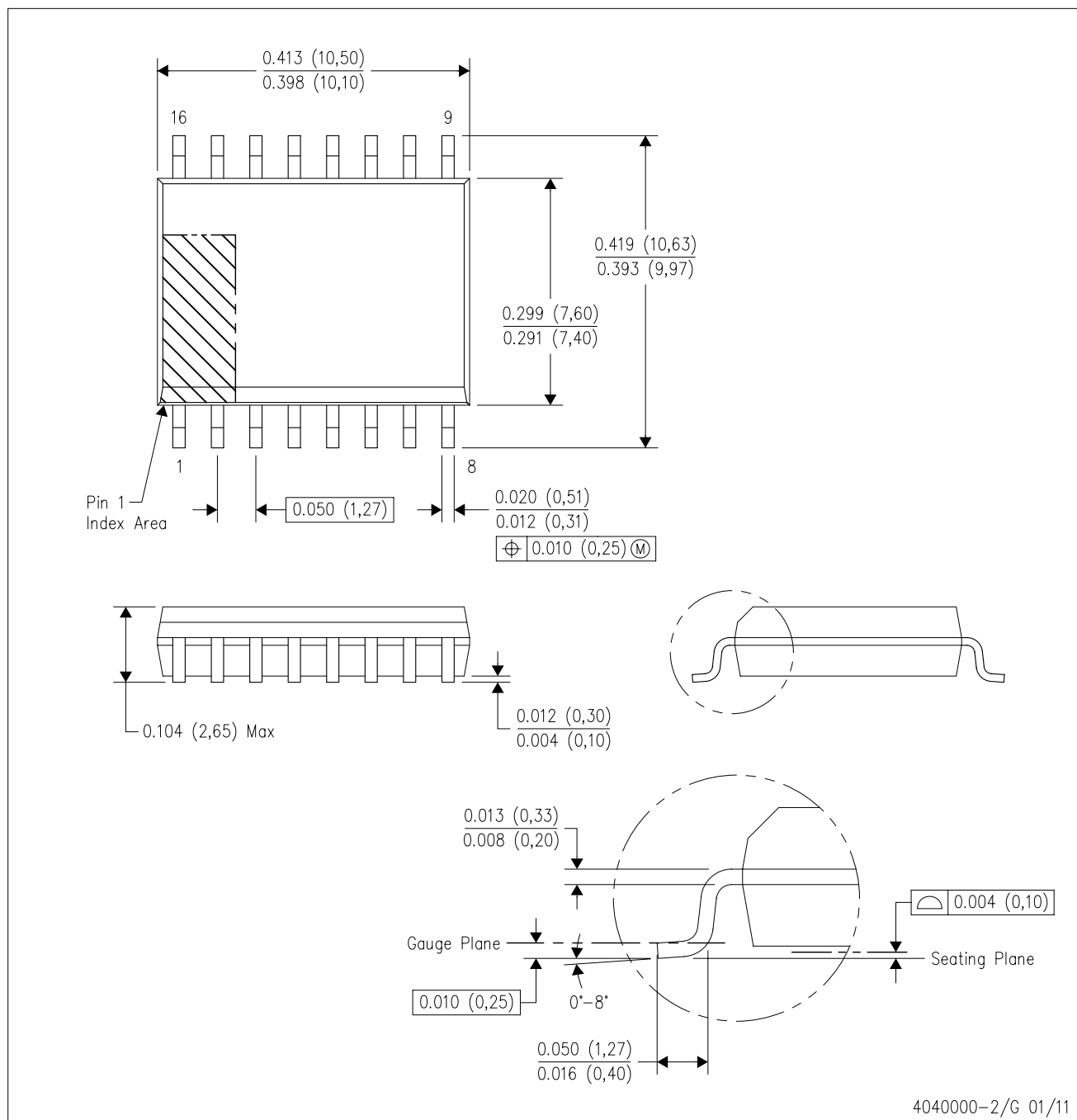
NOTE: All linear dimensions are in millimeters





DW (R-PDSO-G16)

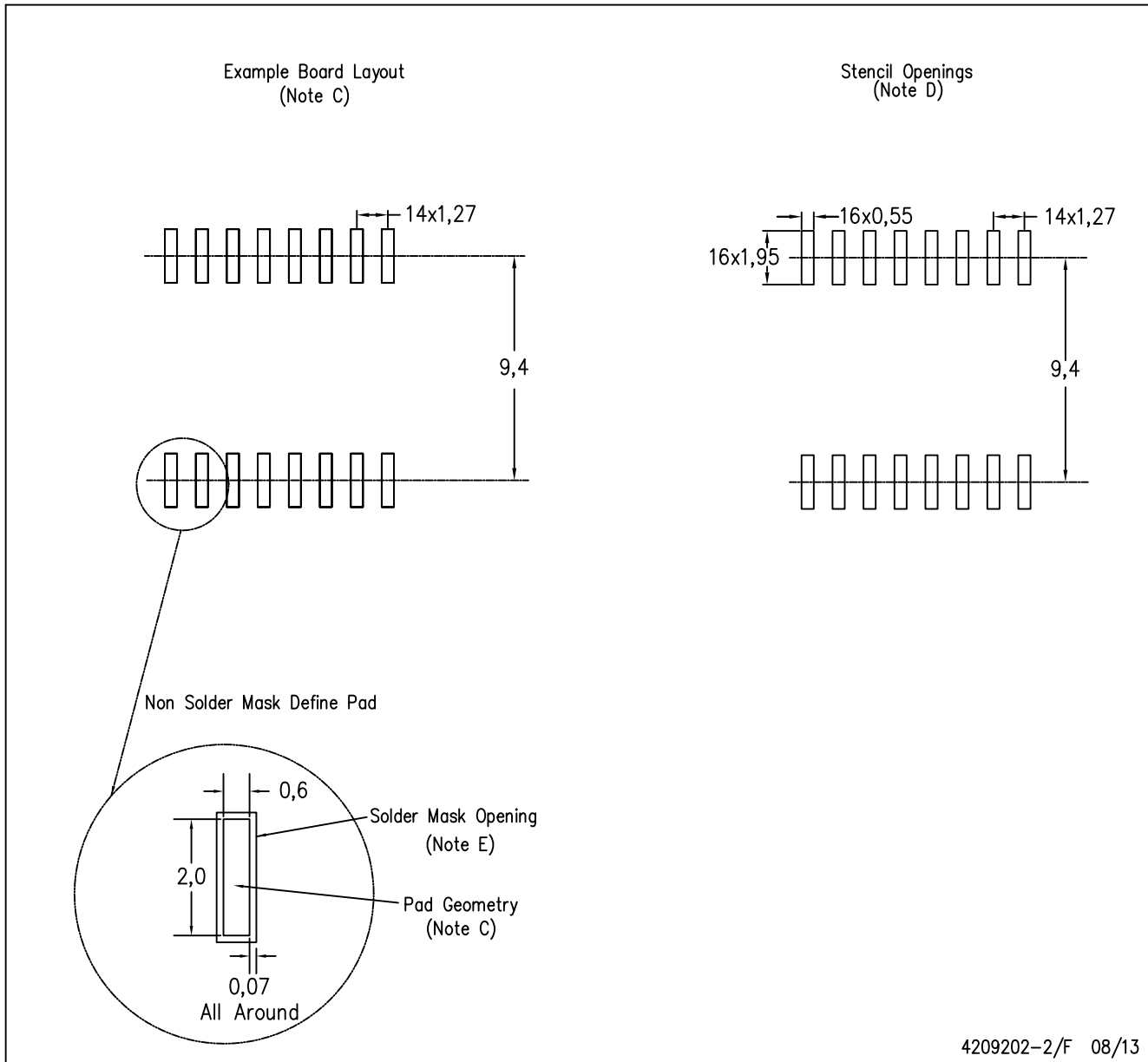
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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