H9CKNNNBKTMTDR

LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory.

These devices contain the following number of bits:
8 Gb has 8,589,934,592 bits
LPDDR3 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input
pins in the system. The 10-bit CA bus contains command, address, and bank information. Each command uses one clock
cycle, during which command information is transferred on both the positive and negative edge of the clock.
These devices also use a double data rate architecture on the DQ pins to achieve high speed operation. The double data
rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data bits per DQ
every clock cycle at the I/O pins. A single read or write access for the LPDDR3 SDRAM effectively consists of a single
8n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clockcycle
data transfers at the I/O pins.
Read and write accesses to the LPDDR3 SDRAMs are burst oriented; accesses start at a selected location and continue
for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate
command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the
Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with
the Read or Write command are used to select the bank and the starting column location for the burst access.
Prior to normal operation, the LPDDR3 SDRAM must be initialized. The following section provides detailed information
covering device initialization, register definition, command description and device operation.

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Features

[FBGA]
Operation Temperature
- -30'C ~ 105'C
Packcage
- 216-ball FBGA
- 15.0x15.0mm2, 0.70t, 0.50mm pitch
- Lead & Halogen Free
[LPDDR3]
VDD1 = 1.8V (1.7V to 1.95V)
VDD2, VDDCA and VDDQ = 1.2V (1.14V to 1.30)
HSUL_12 interface (High Speed Unterminated Logic 1.2V)
Double data rate architecture for command, address and data Bus;
- all control and address except CS_n, CKE latched at both rising and falling edge of the clock
- CS_n, CKE latched at rising edge of the clock
- two data accesses per clock cycle
Differential clock inputs (CK_t, CK_c)
Bi-directional differential data strobe (DQS_t, DQS_c)
- Source synchronous data transaction aligned to bi-directional differential data strobe (DQS_t, DQS_c)
- Data outputs aligned to the edge of the data strobe (DQS_t, DQS_c) when READ operation
- Data inputs aligned to the center of the data strobe (DQS_t, DQS_c) when WRITE operation
DM masks write data at the both rising and falling edge of the data strobe
Programmable RL (Read Latency) and WL (Write Latency)
Programmable burst length: 8
Auto refresh and self refresh supported
All bank auto refresh and per bank auto refresh supported
Auto TCSR (Temperature Compensated Self Refresh)

PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
DS (Drive Strength)
DPD (Deep Power Down)
ZQ (Calibration)
ODT (On Die Termination)

Ordering Information

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
H9CKNNNBKTMTDR-NUH	LPDDR3	1.8V/1.2/1.2/1.2	16Gb (x32, 2Ch 1CS)	DDR3 1866	216Ball FBGA (Lead & Halogen Free)
H9CKNNNBKTMTDR-NTH	LPDDR3	1.8V/1.2/1.2/1.2	16Gb (x32, 2Ch 1CS)	DDR3 1600	216Ball FBGA (Lead & Halogen Free)