

# MC1488, SN55188, SN75188 QUADRUPLE LINE DRIVERS

SLLS094C – SEPTEMBER 1983 – REVISED MAY 2004

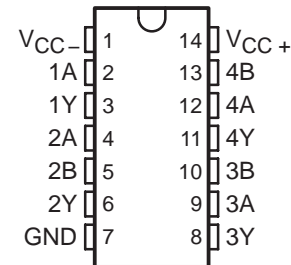
- Meet or Exceed the Requirements of ANSI TIA/EIA-232-E and ITU Recommendation V.28
- Current-Limited Output: 10 mA Typical
- Power-Off Output Impedance: 300  $\Omega$  Minimum
- Slew Rate Control by Load Capacitor
- Flexible Supply-Voltage Range
- Input Compatible With Most TTL Circuits

## description/ordering information

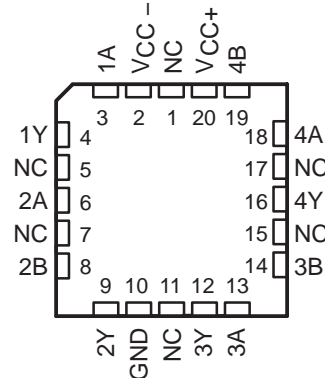
The MC1488, SN55188, and SN75188 are monolithic quadruple line drivers designed to interface data terminal equipment with data communications equipment in conformance with ANSI TIA/EIA-232-E, using a diode in series with each supply-voltage terminal as shown under typical applications.

The SN55188 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The MC1488 and SN75188 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN55188 . . . J OR W PACKAGE  
SN75188 . . . D, N, OR NS PACKAGE  
MC1488 . . . N PACKAGE  
(TOP VIEW)



SN55188 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	MC1488N	MC1488N
		Tube of 25	SN75188N	SN75188N
	SOIC (D)	Tube of 50	SN75188D	SN75188
		Reel of 2500	SN75188DR	
–55°C to 125°C	SOP (NS)	Reel of 2000	SN75188NSR	SN75188
	CDIP (J)	Tube of 25	SN55188J	SN55188J
			SNJ55188J	SNJ55188J
	CFP (W)	Tube of 150	SNJ55188W	SNJ55188W
	LCCC (FK)	Tube of 55	SNJ55188FK	SNJ55188FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

MC1488, SN55188, SN75188  
QUADRUPLE LINE DRIVERS

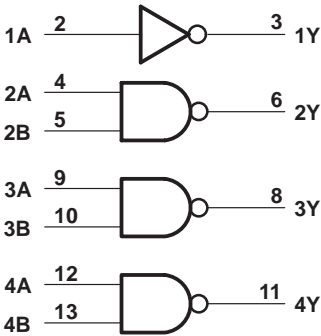
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FUNCTION TABLE  
(drivers 2–4)

A	B	Y
H	H	L
L	X	H
X	L	H

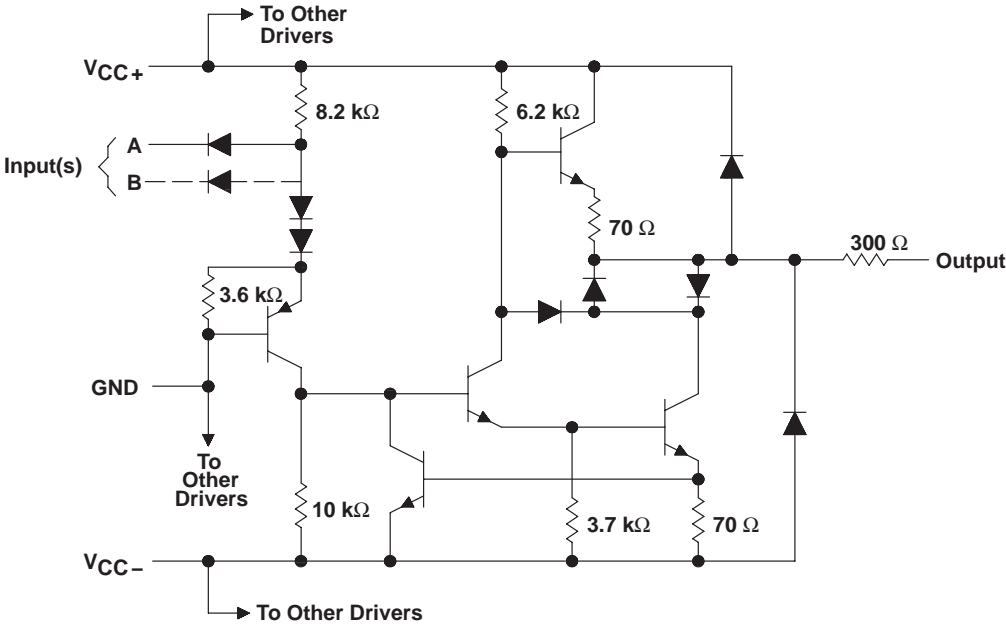
H = high level, L = low level,  
X = irrelevant

logic diagram (positive logic)



Positive logic  
 $Y = \overline{A}$  (driver 1)  
 $Y = \overline{AB}$  or  $\overline{A} + \overline{B}$  (drivers 2 thru 4)

schematic (each driver)



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**

Supply voltage, $V_{CC+}$ at (or below) 25°C free-air temperature (see Notes 1 and 2)	15 V
Supply voltage, $V_{CC-}$ at (or below) 25°C free-air temperature (see Notes 1 and 2)	–15 V
Input voltage, $V_I$	–15 V to 7 V
Output voltage, $V_O$	–15 V to 15 V
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table
Package thermal impedance, $\theta_{JA}$ (see Notes 3 and 4): D package	86°C/W
N package	80°C/W
NS package	76°C/W
Operating virtual junction temperature, $T_J$	150°C
Case temperature for 60 seconds, FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to the network ground terminal.
  2. For operation above 25°C free-air temperature, refer to the maximum supply voltage curve, Figure 6. In the J package, SN55188 chips are alloy mounted.
  3. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.
  4. The package thermal impedance is calculated in accordance with JESD 51-7.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

**recommended operating conditions**

		SN55188			MC1488, SN75188			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC+}$	Supply voltage	7.5	9	15	7.5	9	15	V
$V_{CC-}$	Supply voltage	–7.5	–9	–15	–7.5	–9	–15	V
$V_{IH}$	High-level input voltage	1.9			1.9			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$T_A$	Operating free-air temperature	–55		125	0		70	°C

# MC1488, SN55188, SN75188 QUADRUPLE LINE DRIVERS

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electrical characteristics over operating free-air temperature range,  $V_{CC\pm} = \pm 9\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55188			MC1488, SN75188			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>OH</sub>	High-level output voltage	V <sub>IL</sub> = 0.8 V, R <sub>L</sub> = 3 kΩ	V <sub>CC+</sub> = 9 V, V <sub>CC-</sub> = -9 V	6	7		6	7		V
			V <sub>CC+</sub> = 13.2 V, V <sub>CC-</sub> = -13.2 V	9	10.5		9	10.5		
V <sub>OL</sub>	Low-level output voltage	V <sub>IH</sub> = 1.9 V, R <sub>L</sub> = 3 kΩ	V <sub>CC+</sub> = 9 V, V <sub>CC-</sub> = -9 V		-7‡	-6		-7	-6	V
			V <sub>CC+</sub> = 13.2 V, V <sub>CC-</sub> = -13.2 V		-10.5‡	-9		-10.5	-9	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 5 V				10			10	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0			-1	-1.6		-1	-1.6	mA
I <sub>OS(H)</sub>	Short-circuit output current at high level§	V <sub>I</sub> = 0.8 V,	V <sub>O</sub> = 0	-4.6	-9	-13.5	-6	-9	-12	mA
I <sub>OS(L)</sub>	Short-circuit output current at low level§	V <sub>I</sub> = 1.9 V,	V <sub>O</sub> = 0	4.6	9	13.5	6	9	12	mA
r <sub>o</sub>	Output resistance, power off	V <sub>CC+</sub> = 0, V <sub>O</sub> = -2 V to 2 V	V <sub>CC-</sub> = 0,	300			300			Ω
I <sub>CC+</sub>	Supply current from V <sub>CC+</sub>	V <sub>CC+</sub> = 9 V, No load	All inputs at 1.9 V		15	20		15	20	mA
			All inputs at 0.8 V		4.5	6		4.5	6	
		V <sub>CC+</sub> = 12 V, No load	All inputs at 1.9 V		19	25		19	25	
			All inputs at 0.8 V		5.5	7		5.5	7	
		V <sub>CC+</sub> = 15 V, No load, T <sub>A</sub> = 25°C	All inputs at 1.9 V			34			34	
			All inputs at 0.8 V			12			12	
I <sub>CC-</sub>	Supply current from I <sub>CC-</sub>	V <sub>CC-</sub> = -9 V, No load	All inputs at 1.9 V	-13	-17		-13	-17	mA	
			All inputs at 0.8 V		-0.5			-0.015		
		V <sub>CC-</sub> = -12 V, No load	All inputs at 1.9 V	-18	-23		-18	-23		
			All inputs at 0.8 V		-0.5			-0.015		
		V <sub>CC-</sub> = -15 V, No load, T <sub>A</sub> = 25°C	All inputs at 1.9 V		-34			-34		
			All inputs at 0.8 V		-2.5			-2.5		
P <sub>D</sub>	Total power dissipation	V <sub>CC+</sub> = 9 V, No load	V <sub>CC-</sub> = -9 V,			333			333	mW
		V <sub>CC+</sub> = 12 V, No load	V <sub>CC-</sub> = -12 V,			576			576	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if  $-6\text{ V}$  is a maximum, the typical value is a more negative voltage.

§ Not more than one output should be shorted at a time.

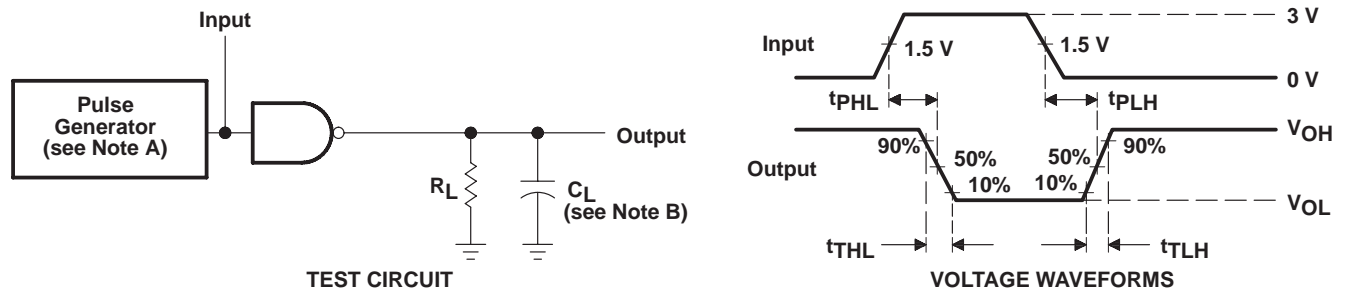
switching characteristics,  $V_{CC\pm} = \pm 9\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega$ , See Figure 1 $C_L = 15\text{ pF}$		220	350	ns
$t_{PHL}$ Propagation delay time, high- to low-level output			100	175	ns
$t_{TLH}$ Transition time, low- to high-level output <sup>†</sup>			55	100	ns
$t_{THL}$ Transition time, high- to low-level output <sup>†</sup>			45	75	ns
$t_{TLH}$ Transition time, low- to high-level output <sup>‡</sup>	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , See Figure 1 $C_L = 2500\text{ pF}$		2.5		$\mu\text{s}$
$t_{THL}$ Transition time, high- to low-level output <sup>‡</sup>			3.0		$\mu\text{s}$

<sup>†</sup> Measured between 10% and 90% points of output waveform

<sup>‡</sup> Measured between 3 V and  $-3\text{ V}$  points on the output waveform (TIA/EIA-232-E conditions)

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics:  $t_w = 0.5\text{ }\mu\text{s}$ ,  $\text{PRR} \leq 1\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

# TYPICAL CHARACTERISTICS†

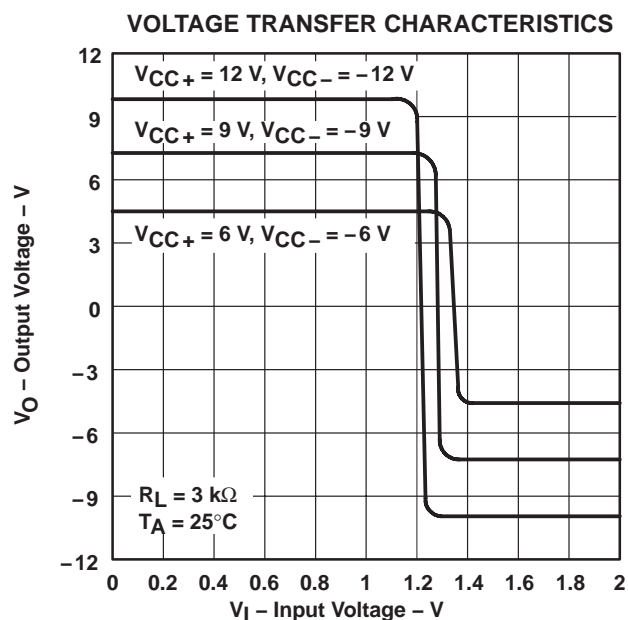


Figure 2

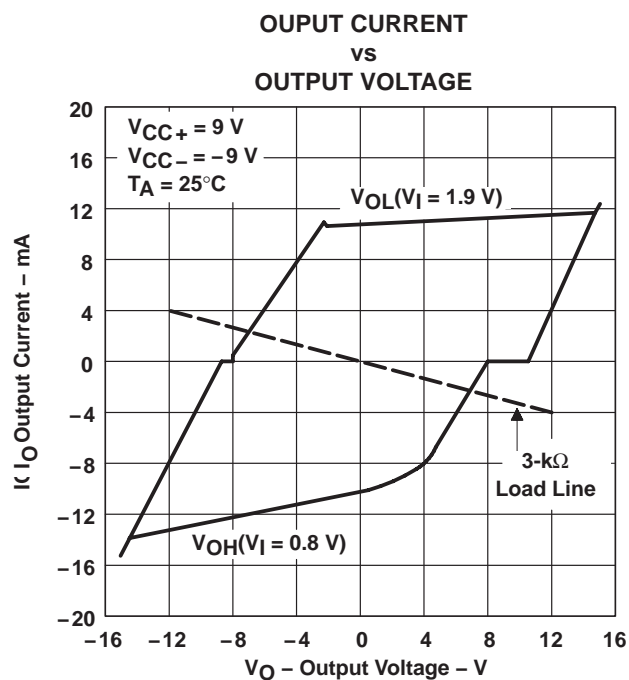


Figure 3

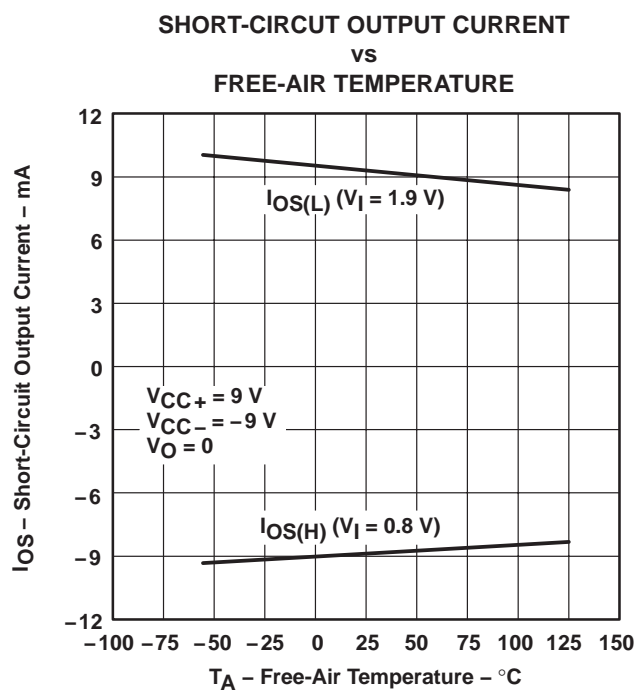


Figure 4

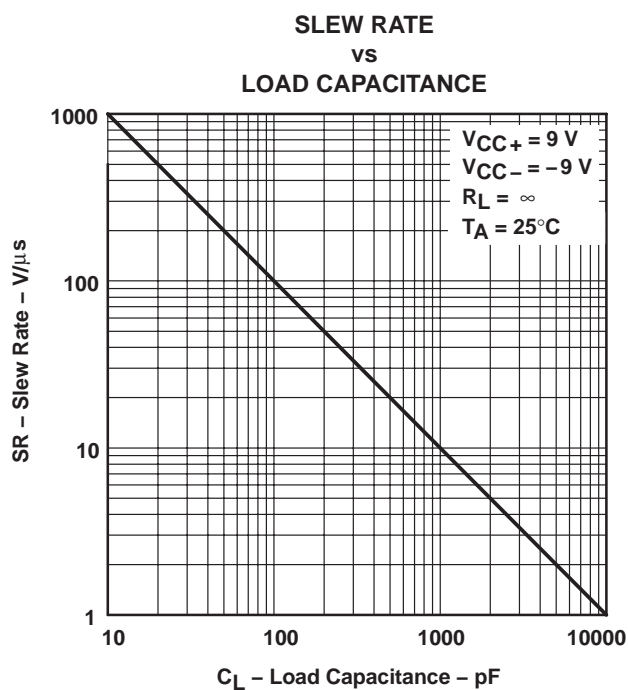
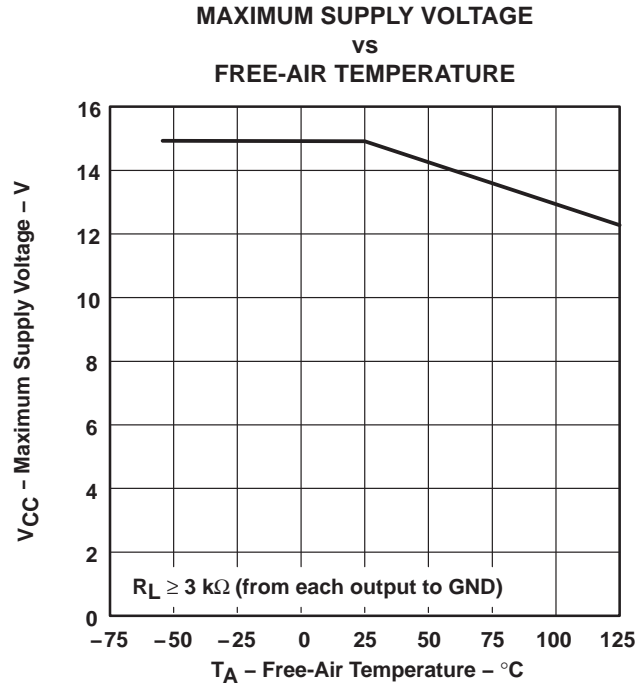


Figure 5

† Data for temperatures below  $0^\circ\text{C}$  and above  $70^\circ\text{C}$  are applicable to SN55188 circuit only.

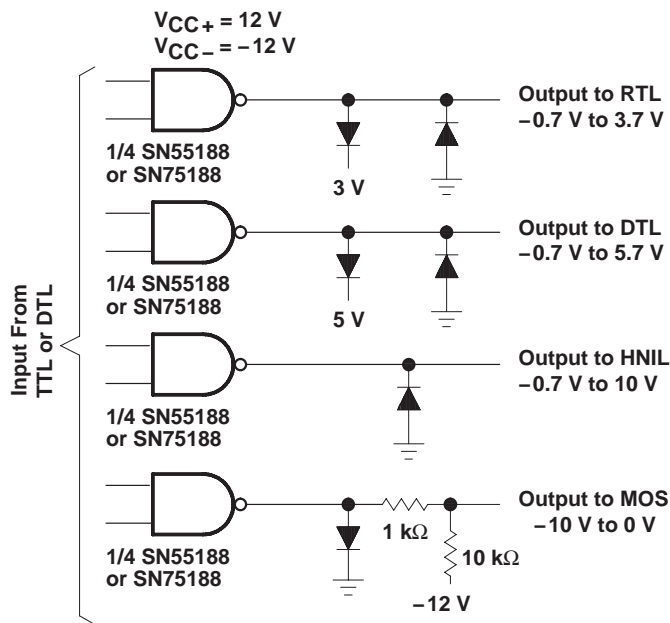
## THERMAL INFORMATION†



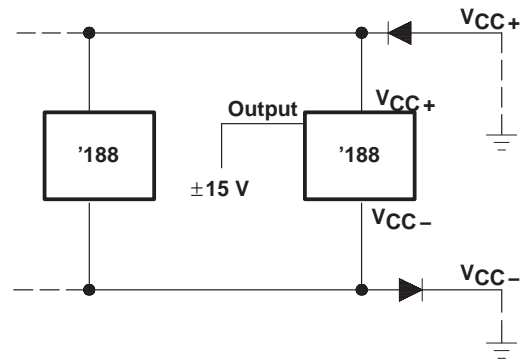
**Figure 6**

† Data for temperatures below 0°C and above 70°C are applicable to the SN55188 circuit only.

## APPLICATION INFORMATION



**Figure 7. Logic Translator Applications**



Diodes placed in series with the  $V_{CC+}$  and  $V_{CC-}$  leads protect the SN55188/SN75188 in the fault condition in which the device outputs are shorted to  $\pm 15 \text{ V}$ , and the power supplies are at low voltage and provide low-impedance paths to ground.

**Figure 8. Power-Supply Protection to Meet Power-Off Fault Conditions of ANSI TIA/EIA-232-E**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86889012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 86889012A SNJ55 188FK	<a href="#">Samples</a>
5962-8688901CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688901CA SNJ55188J	<a href="#">Samples</a>
5962-8688901DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688901DA SNJ55188W	<a href="#">Samples</a>
MC1488N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC1488N	<a href="#">Samples</a>
MC1488NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	MC1488N	<a href="#">Samples</a>
SN55188J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55188J	<a href="#">Samples</a>
SN75188D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	<a href="#">Samples</a>
SN75188DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	<a href="#">Samples</a>
SN75188DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	<a href="#">Samples</a>
SN75188DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	<a href="#">Samples</a>
SN75188DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	<a href="#">Samples</a>
SN75188N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75188N	<a href="#">Samples</a>
SN75188NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75188N	<a href="#">Samples</a>
SN75188NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	<a href="#">Samples</a>
SN75188NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75188	<a href="#">Samples</a>
SNJ55188FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 86889012A SNJ55	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										188FK	
SNJ55188J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688901CA SNJ55188J	<a href="#">Samples</a>
SNJ55188W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8688901DA SNJ55188W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN55188, SN75188 :**

- Catalog: [SN75188](#)
- Military: [SN55188](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75188DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75188NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75188DR	SOIC	D	14	2500	367.0	367.0	38.0
SN75188NSR	SO	NS	14	2000	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

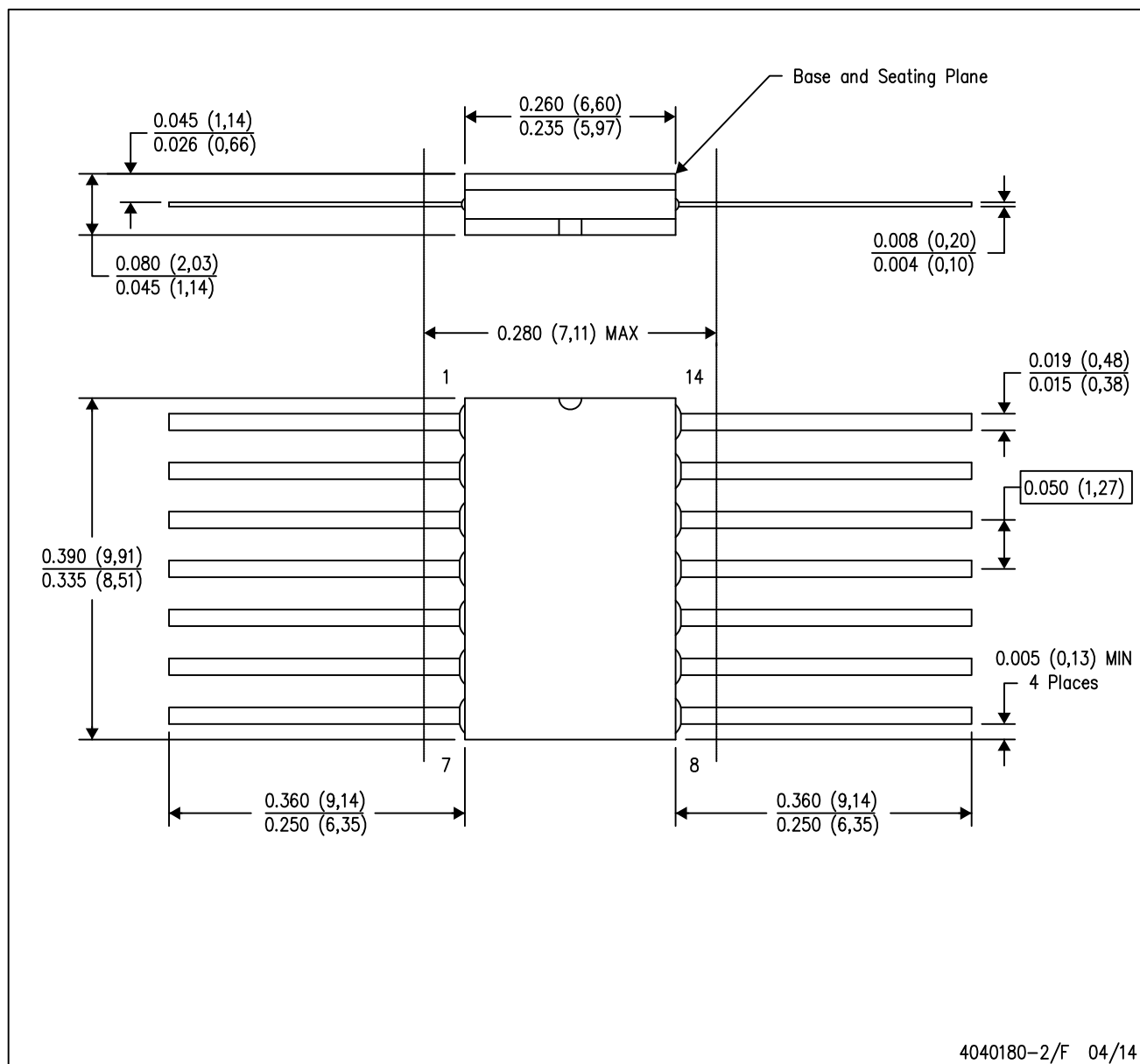


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- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

# LEADLESS CERAMIC CHIP CARRIER



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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