

May 2014

FDMS7608S

Dual N-Channel PowerTrench[®] MOSFET Q1: 30 V, 22 A, 10.0 m Ω Q2: 30 V, 30 A, 6.3 m Ω

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 10.0 m Ω at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 13.6 m Ω at V_{GS} = 4.5 V, I_D = 10 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 6.3 m Ω at V_{GS} = 10 V, I_D = 15 A
- Max $r_{DS(on)} = 7.2 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 13 \text{ A}$
- RoHS Compliant

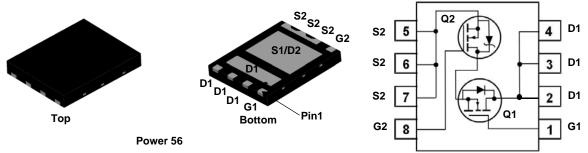
General Description

This device includes two specialized N-Channel MOSFETs in a dual MLP package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFETTM (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units	
V _{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
	Drain Current -Continuous (Package limited)	T _C = 25 °C	22	30	
I_D	-Continuous $T_A = 25^{\circ}$		12 ^{1a}	15 ^{1b}	Α
	-Pulsed		50	60	
E _{AS}	Single Pulse Avalanche Energy (Note		29	33	mJ
P _D	Power Dissipation for Single Operation	T _A = 25°C	2.2 ^{1a}	2.5 ^{1b}	W
	Power Dissipation for Single Operation $T_A = 25^{\circ}C$		1.0 ^{1c}	1.0 ^{1d}	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to	+150	°C	

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57 ^{1a}	50 ^{1b}	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 ^{1c}	120 ^{1d}	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.0	3.2	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7608S	FDMS7608S	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Off Chara	ncteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$ $I_D = 1 mA, V_{GS} = 0 V$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$, referenced to 25°C $I_D = 10 \text{ mA}$, referenced to 25°C	Q1 Q2		13 19		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	Q1 Q2			1 500	μΑ
I_{GSS}	Gate to Source Leakage Current	V _{GS} = 20 V, V _{DS} = 0 V	Q1 Q2			100 100	nA nA
On Chara	cteristics						
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu A$ $V_{GS} = V_{DS}$, $I_D = 1 mA$	Q1 Q2	1.2 1.2	1.9 1.7	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$, referenced to 25°C $I_D = 10 \text{ mA}$, referenced to 25°C	Q1 Q2		-6 -4		mV/°C
	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, \ I_D = 12 \text{ A}$ $V_{GS} = 4.5 \text{ V}, \ I_D = 10 \text{ A}$ $V_{GS} = 10 \text{ V}, \ I_D = 12 \text{ A}, \ T_J = 125^{\circ}\text{C}$	Q1		7.4 10.0 10.3	10.0 13.6 13.9	- mΩ
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, \ I_D = 15 \text{ A}$ $V_{GS} = 4.5 \text{ V}, \ I_D = 13 \text{ A}$ $V_{GS} = 10 \text{ V}, \ I_D = 15 \text{ A}, \ T_J = 125^{\circ}\text{C}$	Q2		4.8 6.0 6.6	6.3 7.2 8.6	- 11152
9 _{FS}	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_{D} = 12 \text{ A}$ $V_{DD} = 5 \text{ V}, I_{D} = 15 \text{ A}$	Q1 Q2		54 76		S
Dynamic	Characteristics						
C _{iss}	Input Capacitance	Q1: V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHZ	Q1 Q2		1135 1380	1510 1835	pF
C _{oss}	Output Capacitance	Q2:	Q1 Q2		390 478	520 635	pF
C _{rss}	Reverse Transfer Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHZ}$	Q1 Q2		42 60	65 90	pF
R_g	Gate Resistance		Q1 Q2	0.2 0.2	1.6 0.5	3.2 2.0	Ω

Switching Characteristics

	·						
t _{d(on)}	Turn-On Delay Time	Q1		Q1 Q2	7 7	14 14	ns
t _r	Rise Time	$V_{DD} = 15 \text{ V, } I_{D} = 12$	$V_{DD} = 15 \text{ V}, I_{D} = 12 \text{ A}, R_{GEN} = 6 \Omega$		3	10 10	ns
t _{d(off)}	Turn-Off Delay Time	Q2 $V_{DD} = 15 \text{ V, } I_{D} = 15 \text{ A, } R_{GEN} = 6 \Omega$		Q2 Q1 Q2	19 20	35 36	ns
t _f	Fall Time			Q1 Q2	3 2	10 10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0V to 10 V	Q1	Q1 Q2	18 21	24 30	nC
Q _{g(TOT)}	Total Gate Charge	$V_{GS} = 0V \text{ to } 5 \text{ V}$	$V_{GS} = 0V \text{ to 5 } V$ $I_D = 15 \text{ V},$ $I_D = 12 \text{ A}$		9 12	14 16	nC
Q _{gs}	Gate to Source Charge	Q2 V _{DD} = 15 V, I _D = 15 A		Q1 Q2	3.6 3.5		nC
Q _{gd}	Gate to Drain "Miller" Charge			Q1 Q2	2.5 3.0		nC

Units

Max

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Parameter

Drain-S	Source Diode Characteristics						
		$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	Q1	0.75	1.1	
\/	Source-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 12 \text{ A}$	(Note 2)	Q1	0.84	1.2	V
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	Q2	0.63	8.0	V
		$V_{GS} = 0 V, I_{S} = 15 A$	(Note 2)	Q2	0.80	1.2	
+	Reverse Recovery Time	Q1		Q1	25	40	20
^L rr	Reverse Recovery Time	$I_F = 12 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$		Q2	21	34	ns
Q _{rr}	Dayaraa Daaayary Charga	Q2		Q1	9	18	nC
	Reverse Recovery Charge	$I_F = 15 \text{ A}, \text{ di/dt} = 300 \text{ A/}\mu\text{s}$		Q2	19	33	nc

Test Conditions

Notes:

Symbol

 R_{0LR} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0LR} is guaranteed by design while R_{0CR} is determined by the user's board design.



a. 57 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in² pad of 2 oz copper

Type

Min

Тур



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.
- 3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- 4. Q1: E_{AS} of 29 mJ is based on starting $T_J = 25$ °C; N-ch: L = 0.3 mH, $I_{AS} = 14$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V. 100% tested at L = 3 mH, $I_{AS} = 3.75$ A. Q2: E_{AS} of 33 mJ is based on starting $T_J = 25$ °C; N-ch: L = 0.3 mH, $I_{AS} = 15$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V. 100% tested at L = 3 mH, $I_{AS} = 3.9$ A.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

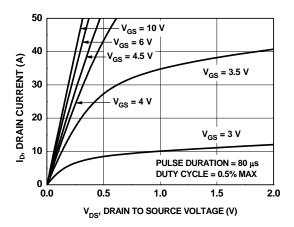
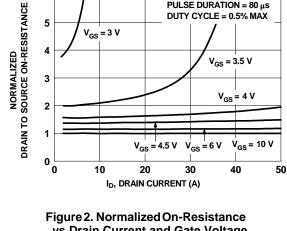


Figure 1. On Region Characteristics



PULSE DURATION = 80 μs

vs Drain Current and Gate Voltage

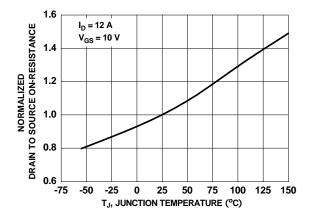


Figure 3. Normalized On Resistance vs Junction Temperature

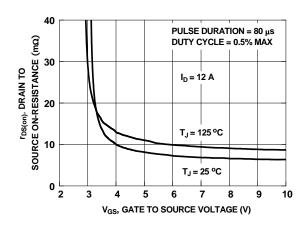


Figure 4. On-Resistance vs Gate to Source Voltage

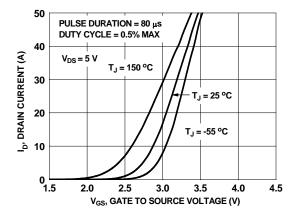


Figure 5. Transfer Characteristics

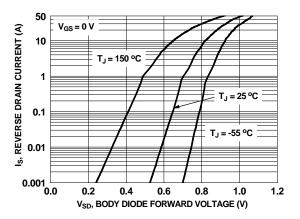


Figure 6. Source to Drain Diode **Forward Voltage vs Source Current**

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

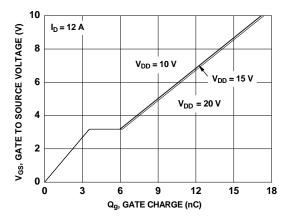


Figure 7. Gate Charge Characteristics

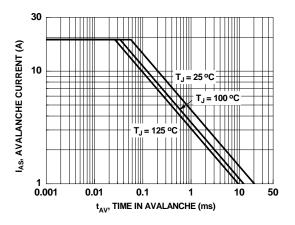


Figure 9. Unclamped Inductive Switching Capability

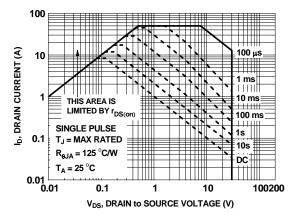


Figure 11. Forward Bias Safe Operating Area

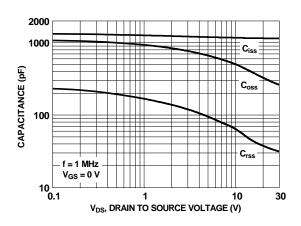


Figure 8. Capacitance vs Drain to Source Voltage

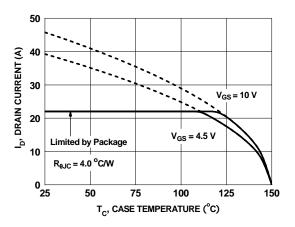


Figure 10. Maximum Continuous Drain Current vs Case Temperature

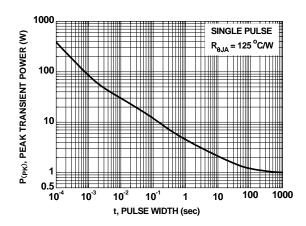


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25$ °C unless otherwise noted

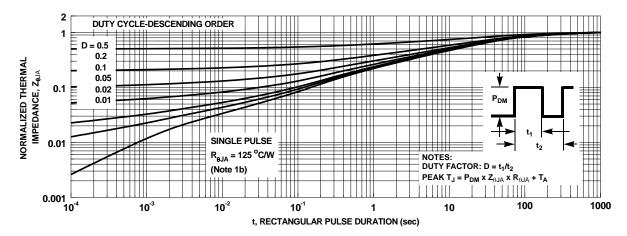


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

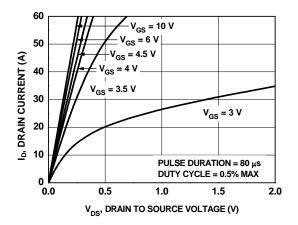


Figure 14. On-Region Characteristics

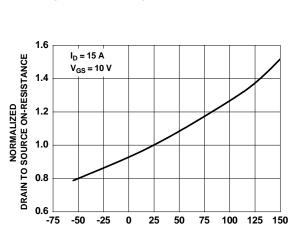


Figure 16. Normalized On-Resistance vs Junction Temperature

T_J, JUNCTION TEMPERATURE (°C)

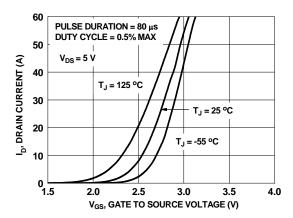


Figure 18. Transfer Characteristics

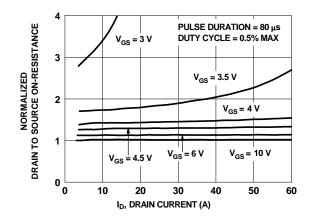


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

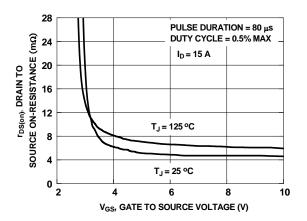


Figure 17. On-Resistance vs Gate to Source Voltage

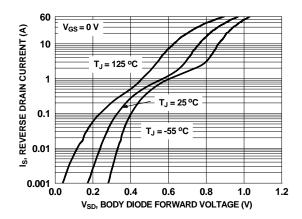


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted

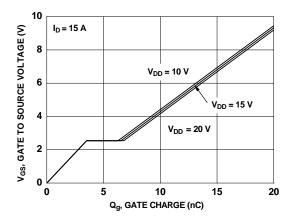


Figure 20. Gate Charge Characteristics

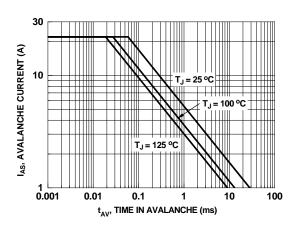


Figure 22. Unclamped Inductive Switching Capability

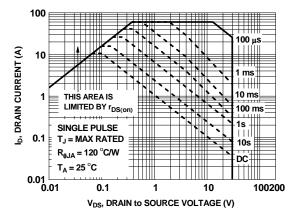


Figure 24. Forward Bias Safe Operating Area

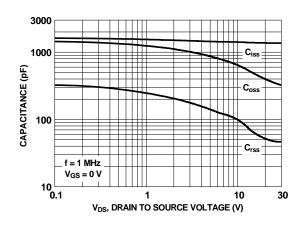


Figure 21. Capacitance vs Drain to Source Voltage

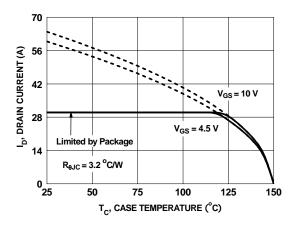


Figure 23. Maximum Continuous Drain Current vs Case Temperature

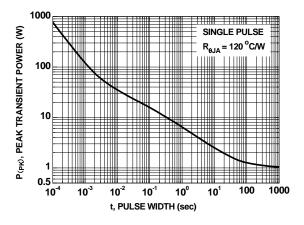


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

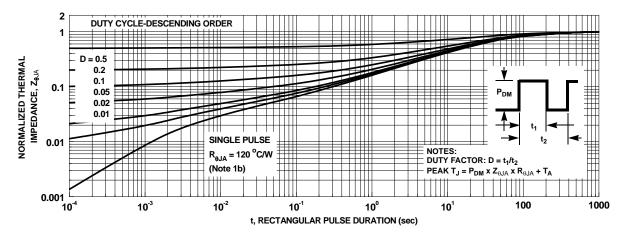


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFETTM Schottky body diode Characteristics

Fairchild's SyncFETTM process embeds a Schottky diode in parallel with PowerTrench[®] MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS7608S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

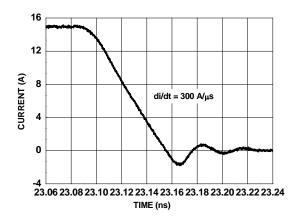


Figure 27. FDMS7608S SyncFETTM Body Diode Reverse Recovery Characteristic

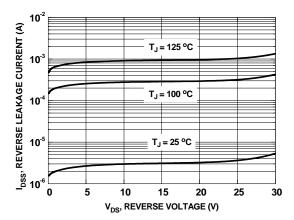
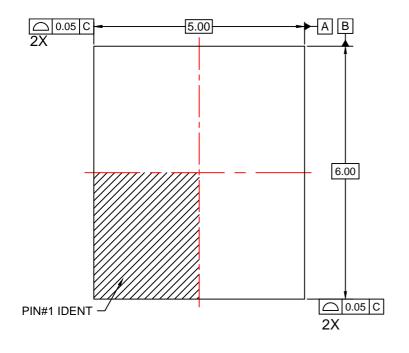
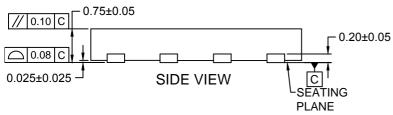
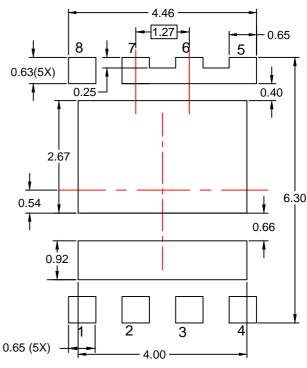


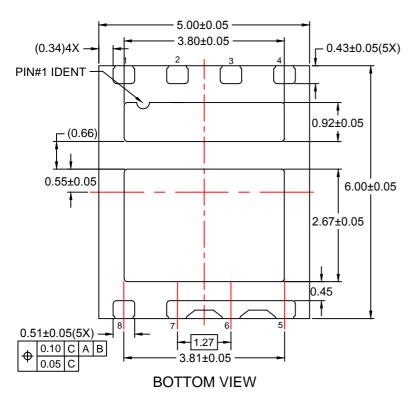
Figure 28. SyncFETTM Body Diode Reverse Leakage vs. Drain-Source Voltage





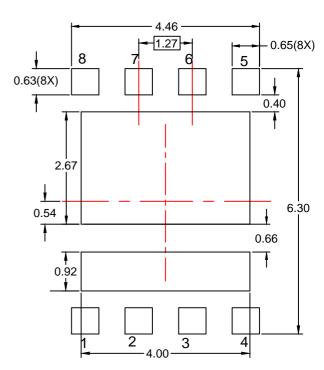


RECOMMENDED LAND PATTERN (OPTION 1 - FUSED LEADS 5,6,7)



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Prev2.



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Definition of Terms

Definition of Terms						
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Rev. 171

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