

OptiMOS[®] 2 Power-Transistor

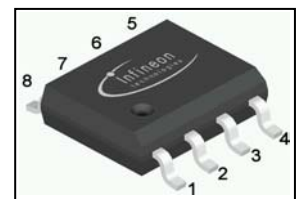
Features

- Fast switching MOSFET for SMPS
- Optimized technology for notebook DC/DC
- Qualified according to JEDEC¹ for target applications
- N-channel
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Avalanche rated
- dv/dt rated

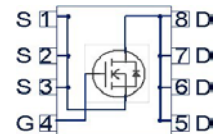
Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	6.4	m Ω
I_D	16	A

P-DSO-8



Type	Package	Ordering Code	Marking
BSO064N03S	P-DSO-8	Q67042-S4207	64N3S



Maximum ratings, at $T_J=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			10 secs	steady state	
Continuous drain current	I_D	$T_A=25\text{ }^{\circ}\text{C}^{(2)}$	16	12	A
		$T_A=70\text{ }^{\circ}\text{C}^{(2)}$	12	9.9	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ }^{\circ}\text{C}^{(3)}$	64		
Avalanche energy, single pulse	E_{AS}	$I_D=16\text{ A}$, $R_{GS}=25\text{ }\Omega$	170		mJ
Reverse diode dv/dt	dv/dt	$I_D=16\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ }^{\circ}\text{C}$	6		kV/ μs
Gate source voltage	V_{GS}		± 20		V
Power dissipation	P_{tot}	$T_A=25\text{ }^{\circ}\text{C}^{(2)}$	2.5	1.56	W
Operating and storage temperature	T_J , T_{stg}		-55 ... 150		$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - soldering point	R_{thJS}		-	-	35	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm ² cooling area ²⁾ , $t_p \leq 10$ s	-	-	50	
		6 cm ² cooling area ²⁾ , steady state	-	-	80	

Electrical characteristics, at $T_j = 25$ °C, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 1$ mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 50$ µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_j = 25$ °C	-	0.1	1	µA
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_j = 125$ °C	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS} = 20$ V, $V_{DS} = 0$ V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 14$ A	-	7.0	8.8	mΩ
		$V_{GS} = 10$ V, $I_D = 16$ A	-	5.3	6.4	
Gate resistance	R_G		-	0.9	-	Ω
Transconductance	g_{fs}	$ V_{DS} > 2 I_D R_{DS(on)max}$, $I_D = 16$ A	26	51	-	S

¹⁾ J-STD20 and JESD22

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	2720	3620	pF
Output capacitance	C_{oss}		-	970	1290	
Reverse transfer capacitance	C_{rss}		-	120	180	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=8\text{ A}, R_G=2.7\text{ }\Omega$	-	6.7	10	ns
Rise time	t_r		-	5.8	8.7	
Turn-off delay time	$t_{d(off)}$		-	29	43	
Fall time	t_f		-	4.2	6.3	

Gate Charge Characteristics⁴⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=8\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	7.4	10	nC
Gate charge at threshold	$Q_{g(th)}$		-	4.3	5.8	
Gate to drain charge	Q_{gd}		-	5.0	7.5	
Switching charge	Q_{sw}		-	8.1	12	
Gate charge total	Q_g		-	21	28	
Gate plateau voltage	$V_{plateau}$		-	2.7	-	V
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	18	25	nC
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	23	31	

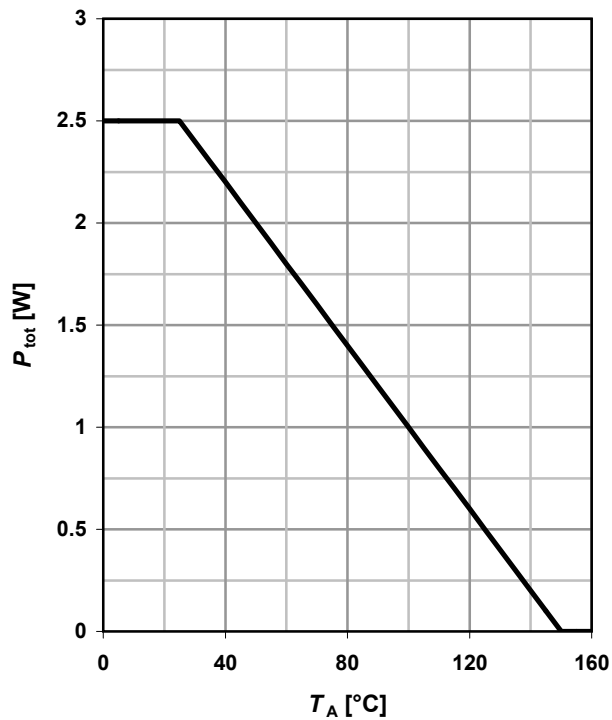
Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	2.5	A
Diode pulse current	$I_{S,pulse}$		-	-	64	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=2.5\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.73	1	
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	

⁴⁾ See figure 16 for gate charge parameter definition

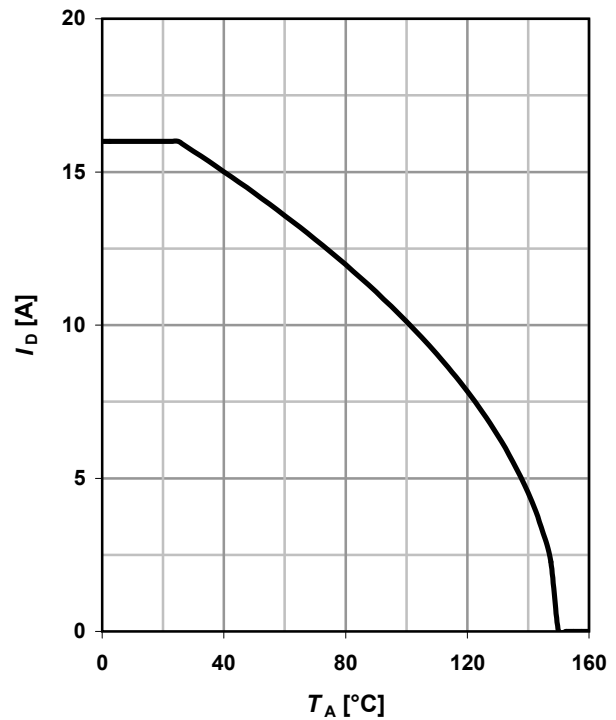
1 Power dissipation

$$P_{\text{tot}} = f(T_A); t_p \leq 10 \text{ s}$$



2 Drain current

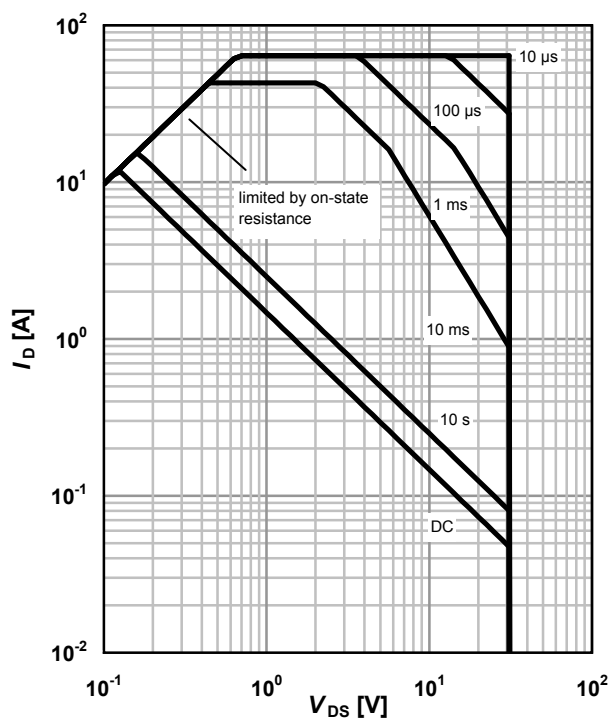
$$I_D = f(T_A); V_{GS} \geq 10 \text{ V}; t_p \leq 10 \text{ s}$$



3 Safe operation area

$$I_D = f(V_{DS}); T_A = 25^\circ\text{C}^{(1)}; D = 0$$

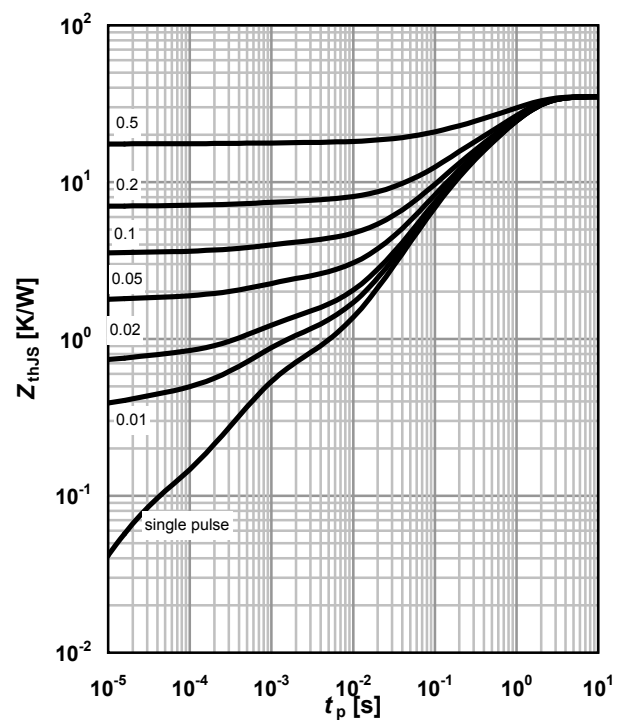
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJS}} = f(t_p)$$

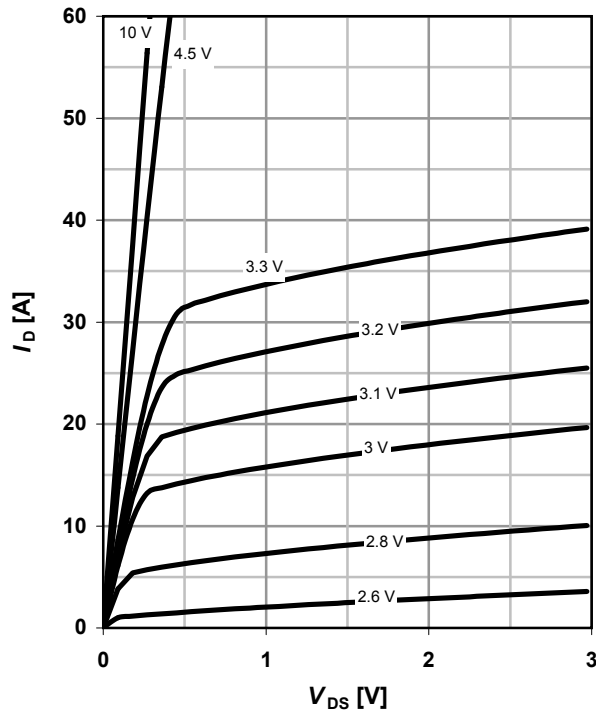
parameter: $D = t_p/T$



5 Typ. output characteristics

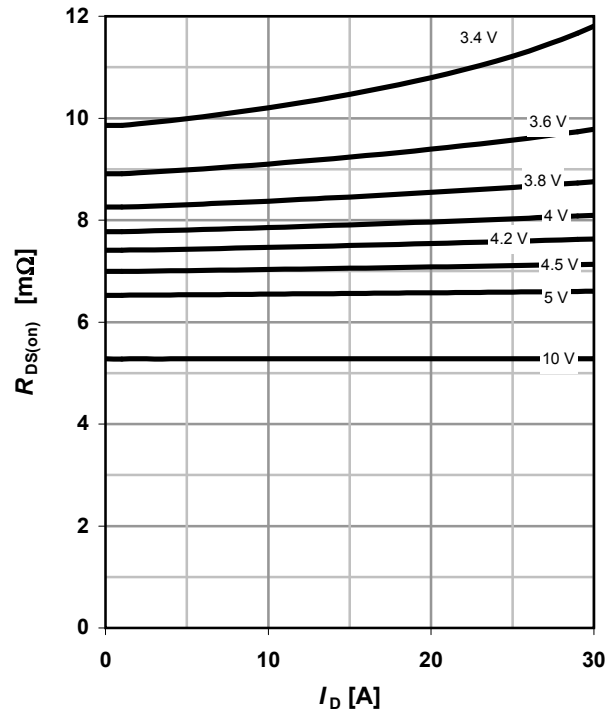
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

parameter: V_{GS}


6 Typ. drain-source on resistance

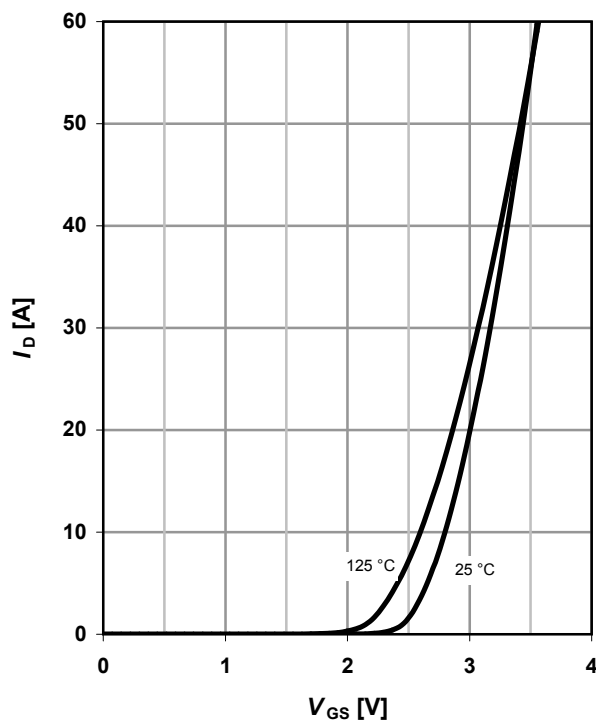
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

parameter: V_{GS}

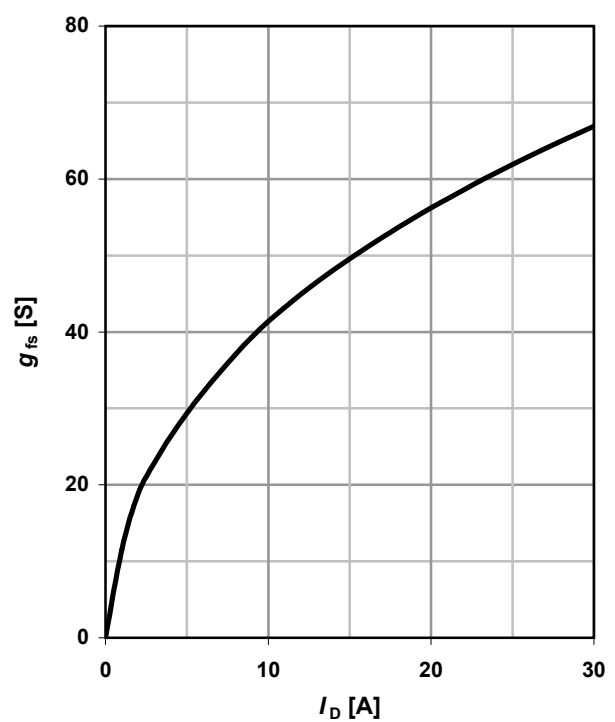

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)\max}$$

parameter: T_j

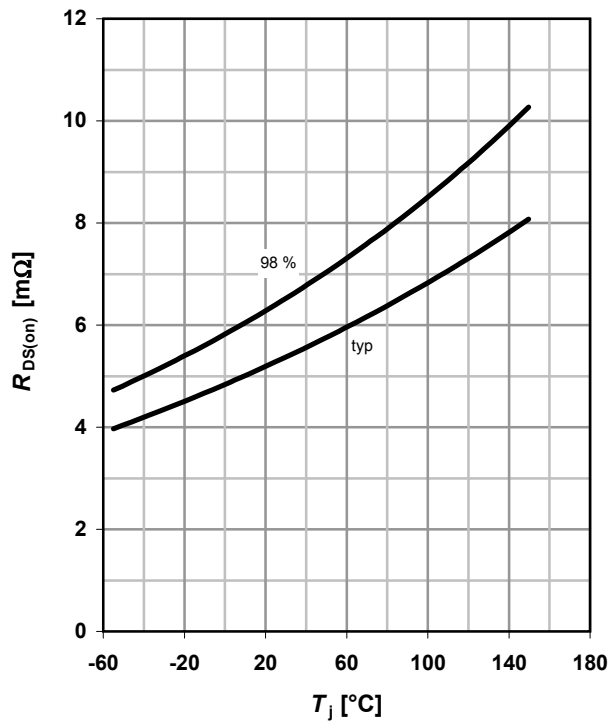

8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



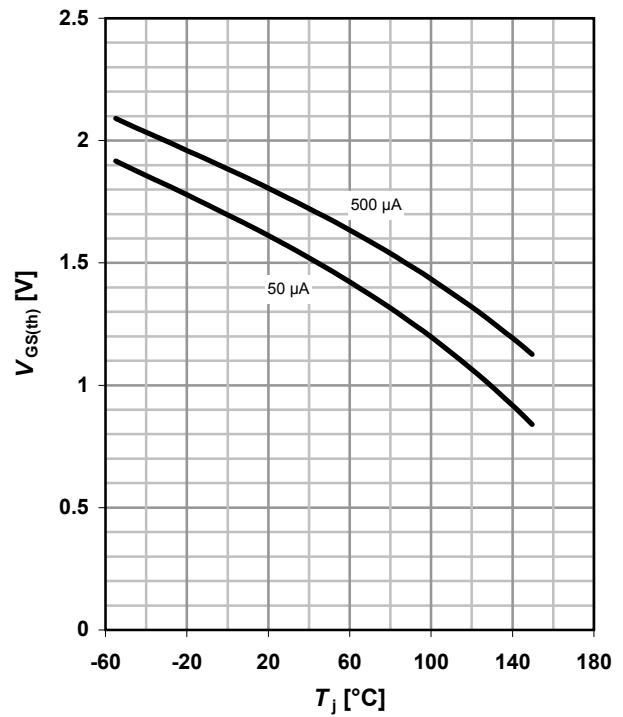
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 16 \text{ A}; V_{GS} = 10 \text{ V}$$

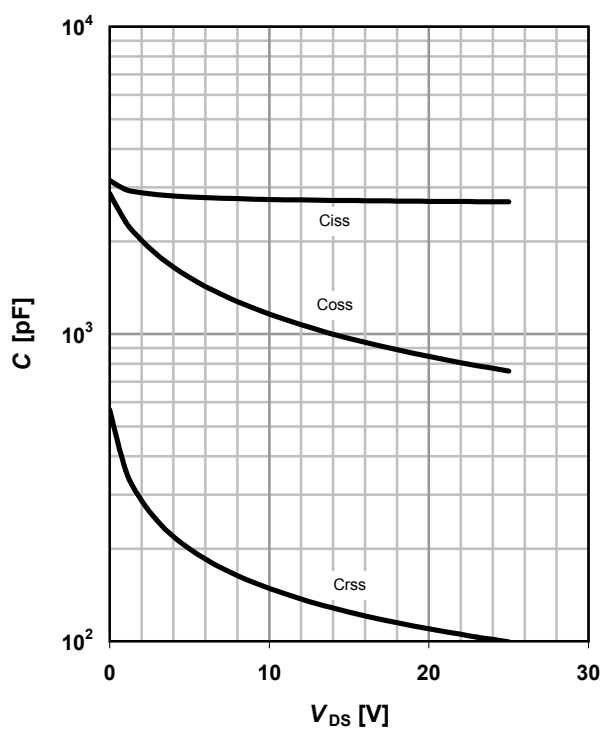

10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D

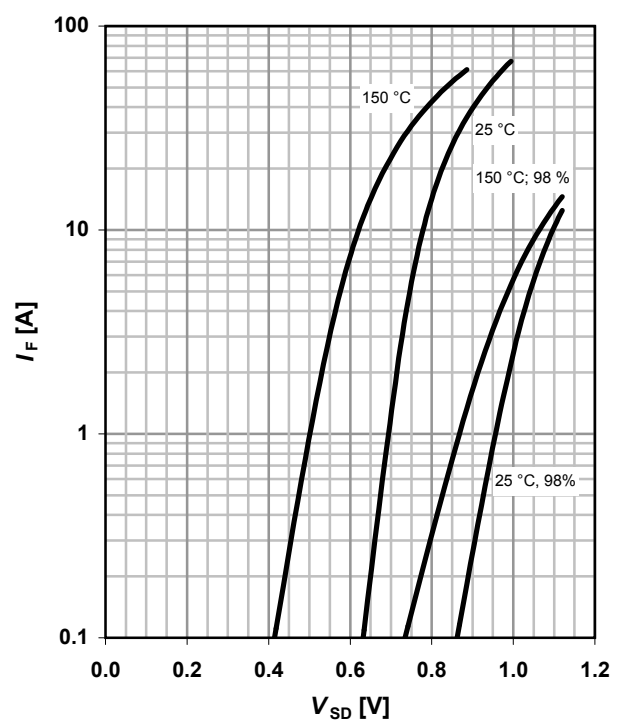

11 Typ. capacitances

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

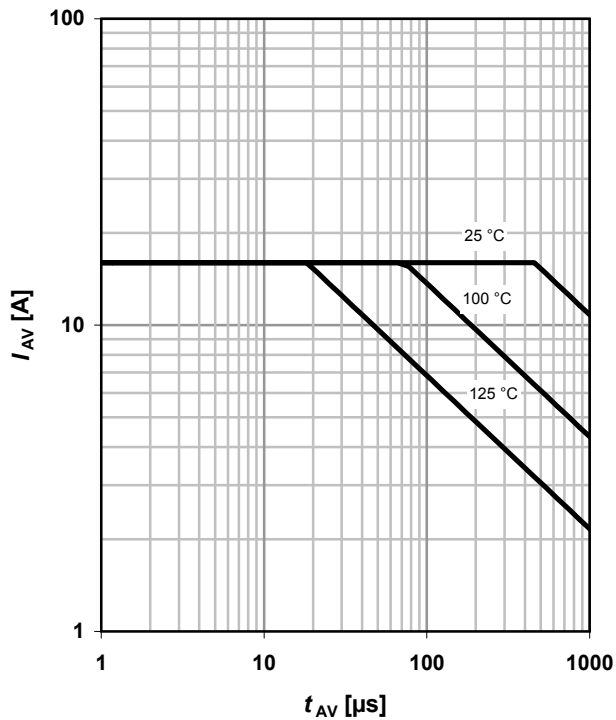
parameter: T_j



13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

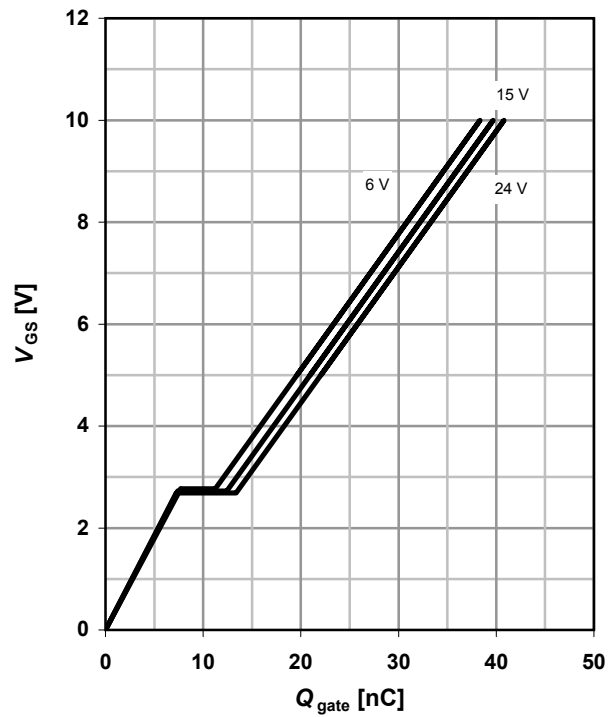
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

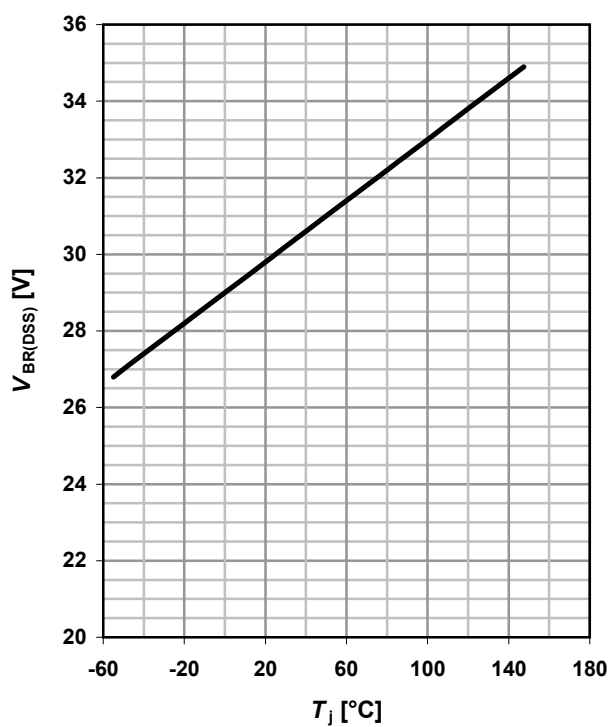
$$V_{GS}=f(Q_{\text{gate}}); I_D=8\ \text{A pulsed}$$

parameter: V_{DD}

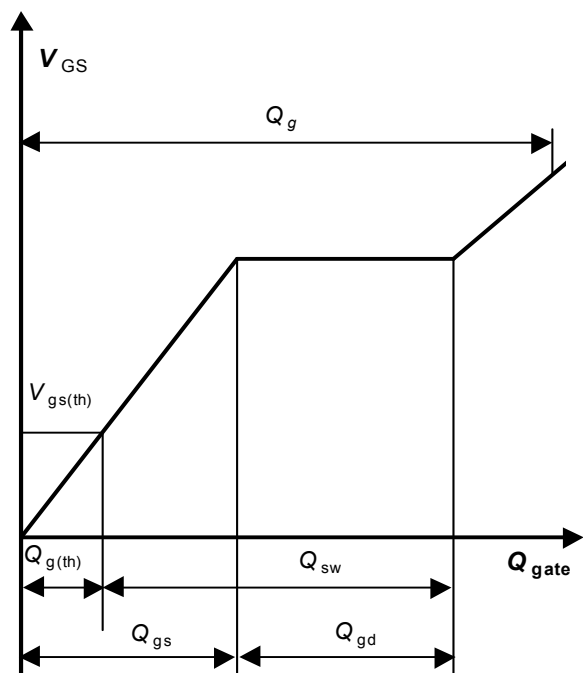


15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=1\ \text{mA}$$

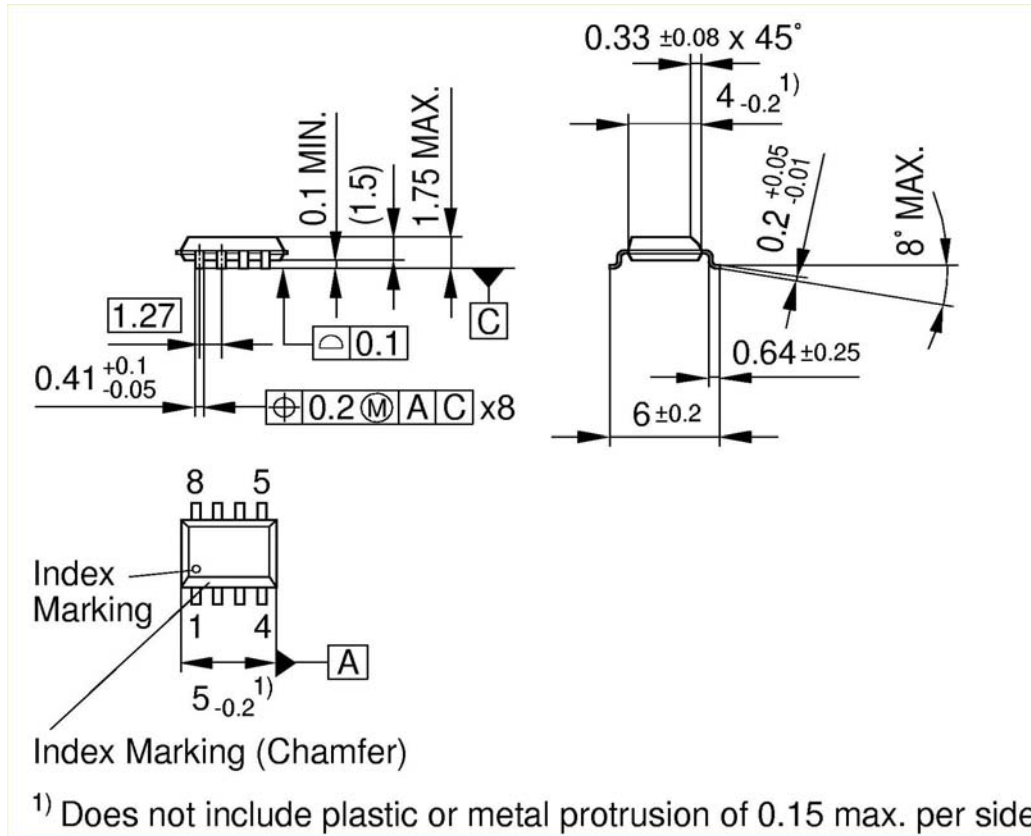


16 Gate charge waveforms

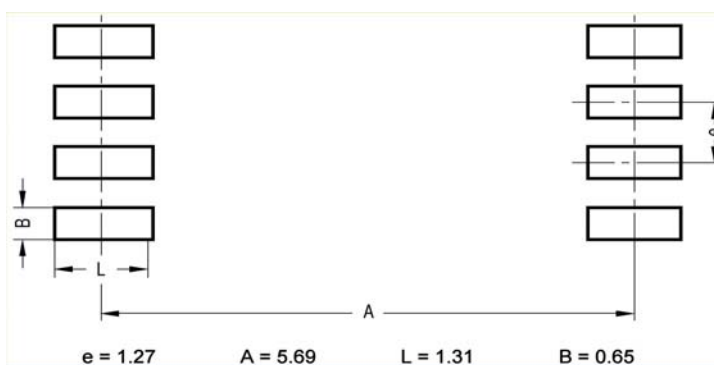


Package Outline

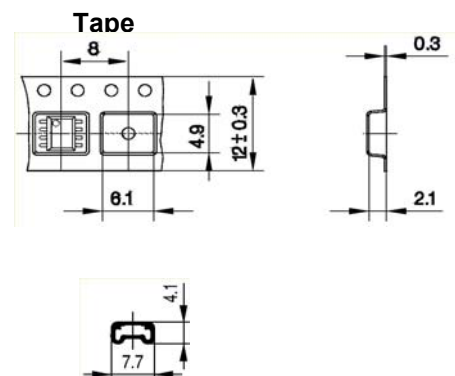
P-DSO-8: Outline



Footprint



Packaging



Dimensions in mm

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