LCD Driver for 96 Display Units BL55066

General Description

The BL55066 is a peripheral device, which interfaces to almost any Liquid Crystal Display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four back planes and up to 24 segments and can easily be cascaded for larger LCD applications. The BL55066 is compatible with most microprocessors/micro controllers and communicates via a two-line bi-directional IIC -bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware sub addressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable back plane drive figuration: static or2, 3or 4backplane multiplexing
- Selectable display bias configuration: static,1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24×4-bit RAM for display data storage
- Auto-incremented display data loading across device sub address boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2.5 to 6V power supply range
- Low power consumption
- Power saving mode for extremely low power consumption in battery-operated and telephone applications
- IIC -bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/micro controllers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Ascendable with the 40segment LCD driver BL55076
- Optimized pinning for single plane wiring in both single and multiple BL55066 applications
- Space-saving 40 lead plastic very small outline package (LQFP44)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process.

Application

Telephone、Power meter、Toy、Clock…

Pin Assignment

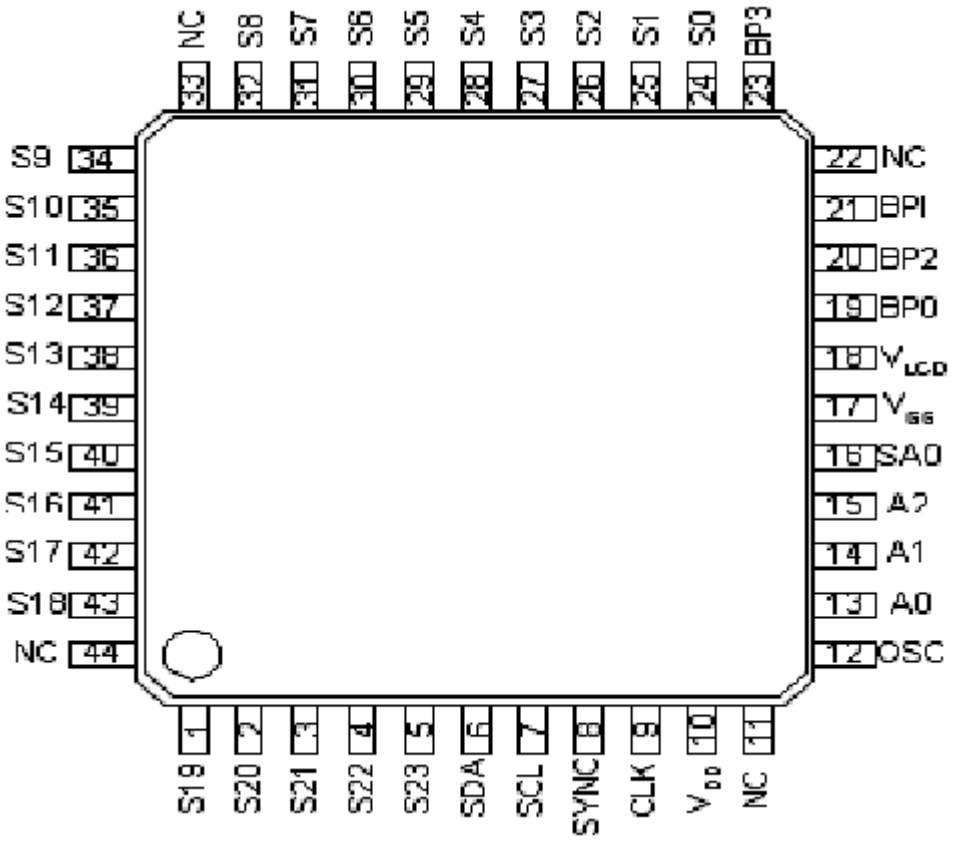


Fig.1

Pin Description

Pin No.	Pin name	Function
6	SDA	Serial data input
7	SCL	Clock input
8	SYNC	Cascade synchronization clock
9	CLK	External oscillator input
10	Vdd	Plus Power terminal
12	OSC	Oscilator control
13、14、15	A0、A1、A2	Subaddress Select
16	SA0	Slave address bit 0
17	Vss	Minus power terminal
18	Vlcd	LCD power source
19、20、21、23	BP0、BP2、BP1、BP3	Common terminal driving output
24-32、34-43、1-5	S0——S23	Segment terminal driving output
11、22、33、44	NC	Unused

Table 1

FUNCTIONAL DESCRIPTION

Functional Circuit

The BL55066 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCD is. It can directly drive any static or multiplexed LCD containing up to 4 back planes and up to 24 segments. The display configurations possible with the BL55066 depend on the number of active back plane outputs required; a selection of display configurations is given in Table 2.

All of the display configurations given in Table 2 can be implemented in the typical system shown in Fig.2. The host microprocessor/micro controller maintains the two-line bus communication channel with the BL55066. The internal oscillator is selected by tying OSC (pin 12) to VSS. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (VDD, VSS and VLCD) and to the LCD panel chosen for the application.

ACTIVE BACKPLANE OUTPUTS	NUMBER OF SEGMENTS	7-SEGMENT NUMERIC	14-SEGMENT ALPHANUMERIC	DOT MATRIX
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 × 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 × 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 × 24)
1	24	3 digits + 3 indicator symbols	1 character + 10 indicator symbols	24 dots

Table 2

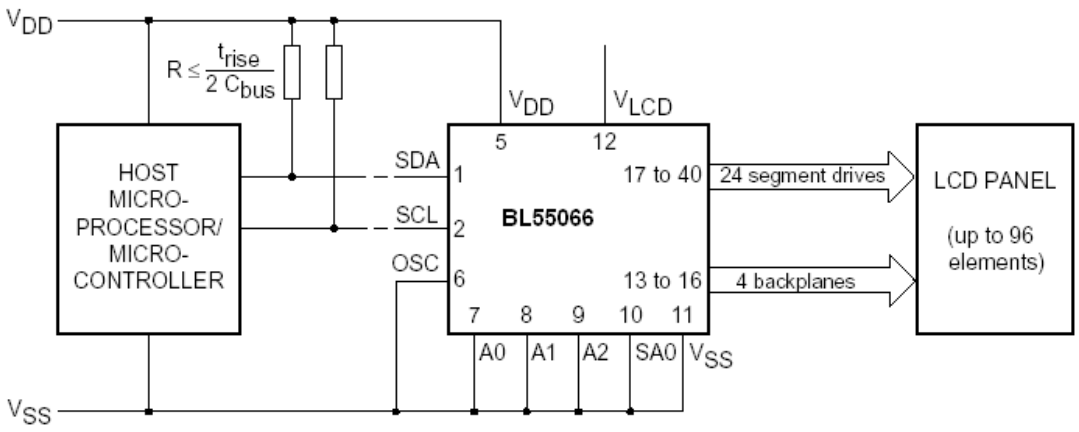


Fig 2

Display Ram

The display RAM is a static 24×4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off ' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the ,individual bits of a RAM word and the back plane outputs. The first RAM column corresponds to the 24 segments operated with respect to back plane BP0 (see Fig.3).In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data are transmitted to the BL55066 the display bytes received are stored in the

display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7 segment numeric display showing all drive modes is given in Fig.4; the RAM filling organization depicted applies equally to other LCD types. With reference to Fig.4, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

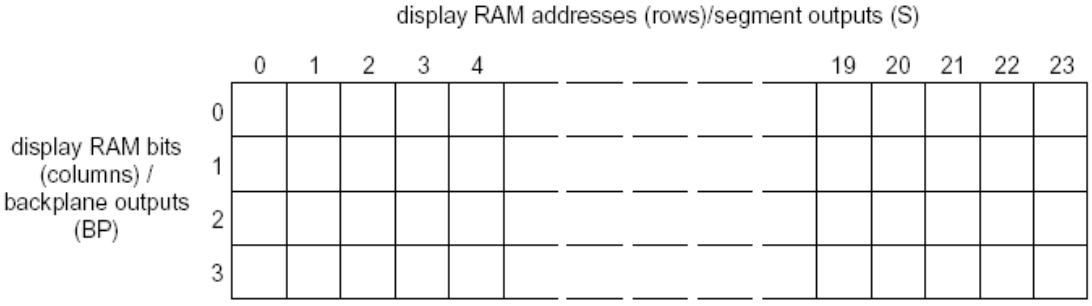


Fig 3

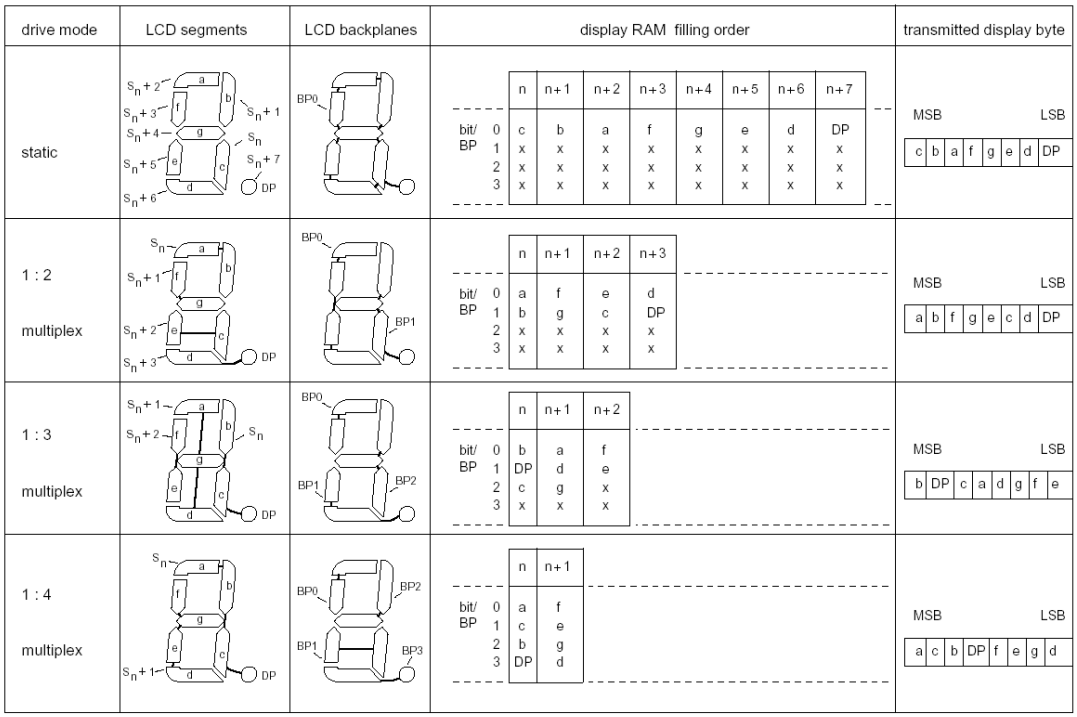


Fig 4

IIC-BUS DESCRIPTION

The IIC-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

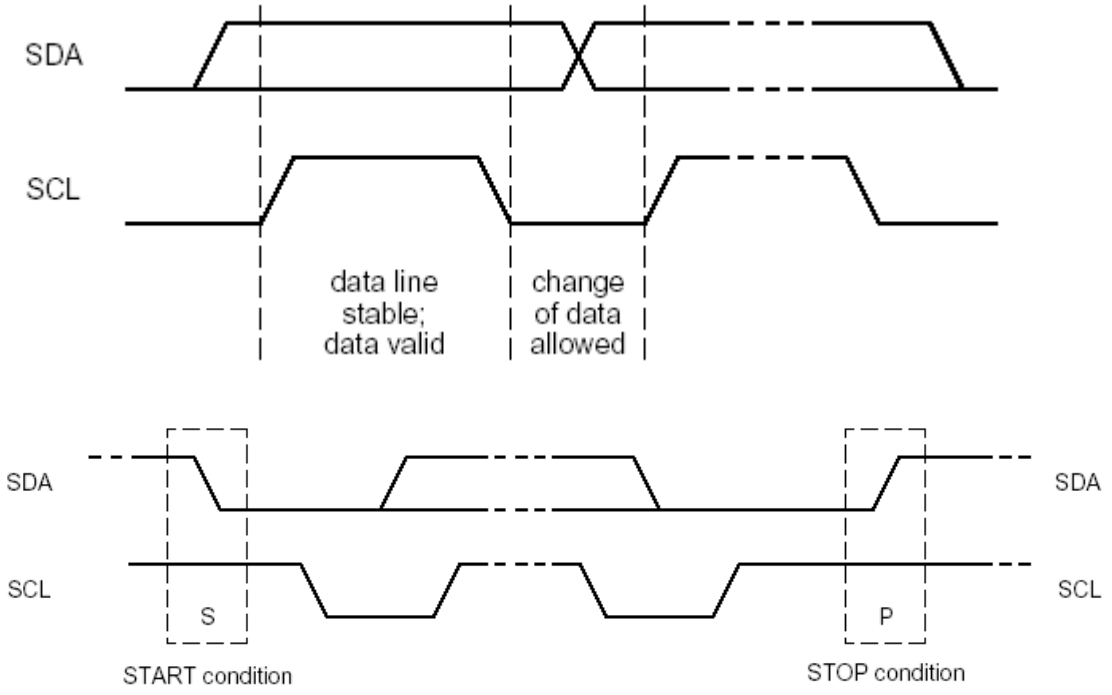
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is a 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



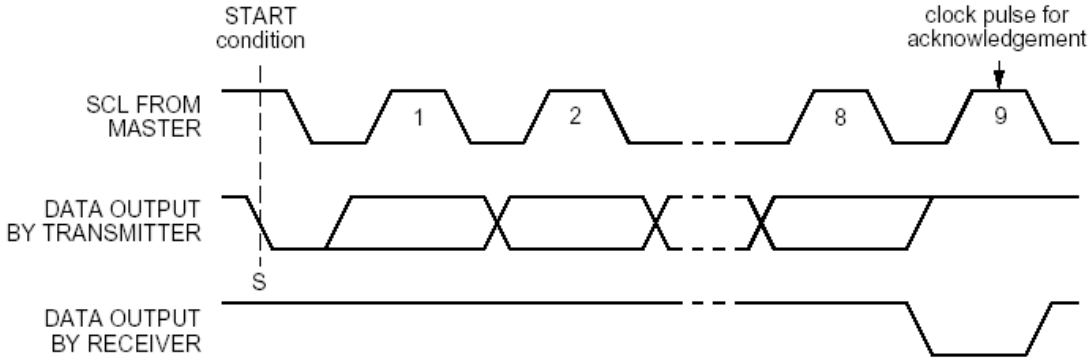


Fig 5

BL55066 IIC-bus controller

The BL55066 acts as an IIC-bus slave receiver. It does not initiate IIC-bus transfers or transmit data to an IIC-bus master receiver. The only data output from the BL55066 are the acknowledge signals of the selected devices. Device selection depends on the IIC-bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to VSS which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to VSS or VDD according to a binary coding scheme such that no two devices with a common I2C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the BL55066 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the BL55066 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the IIC-bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

IIC-bus protocol

Two IIC-bus slave addresses (0111110 and 0111111) are reserved for BL55066. The least-significant bit of the slave address that a BL55066 will respond to is defined by the level tied at its input SA0 (pin 16). Therefore, two types of BL55066 can be distinguished on the same IIC-bus which allows:

1. Up to 16 BL55066s on the same IIC-bus for very large LCD applications
2. The use of two types of LCD multiplex on the same IIC-bus.

The IIC-bus protocol is shown in Fig.15. The sequence is initiated with a START condition (S) from the IIC-bus master which is followed by one of the two BL55066 slave addresses available. All BL55066s with the corresponding SA0 level acknowledge in parallel the slave address but all BL55066s with the alternative SA0 level ignore the whole IIC-bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed BL55066s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed BL55066s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress

counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended BL55066 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed BL55066. After the last display byte, the IIC-bus master issues a STOP condition (P).

Command decoder

The command decoder identifies command bytes that arrive on the IIC-bus. All available commands carry a continuation bit C in their most-significant bit position (see Fig.6). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data. The five commands available to the BL55066 are defined in Table 5.

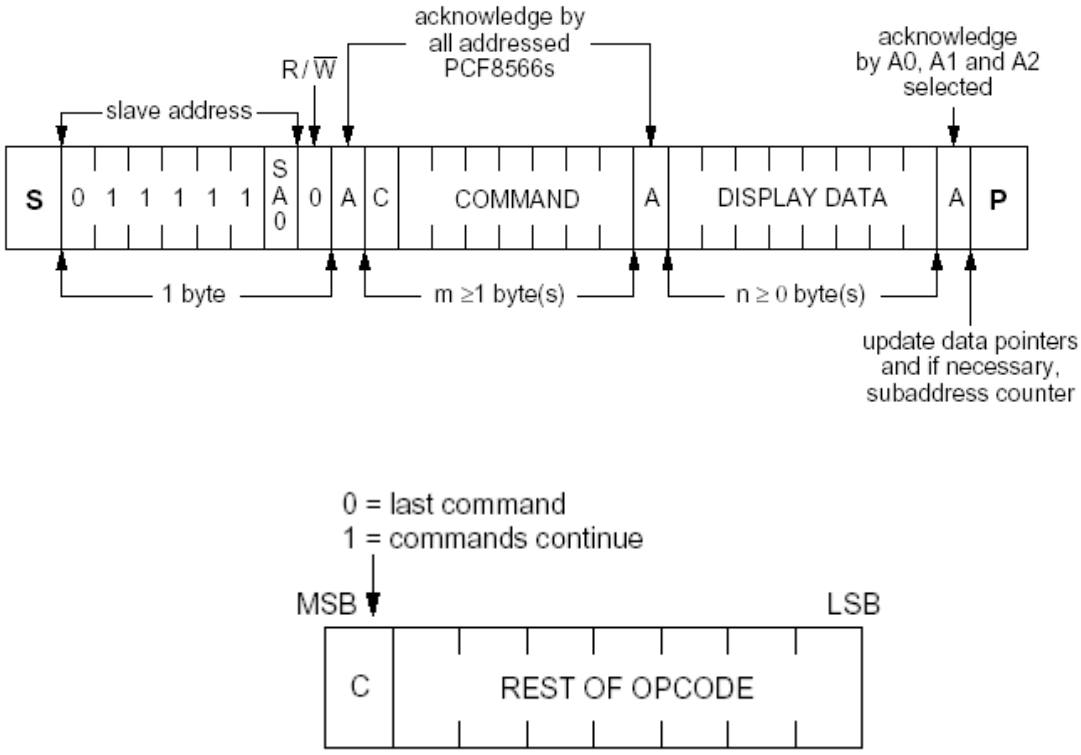


Fig 6

COMMAND/OPCODE								OPTIONS	DESCRIPTION
Mode set									
C	1	0	LP	E	B	M1	M0	see Table 6	defines LCD drive mode
								see Table 7	defines LCD bias configuration
								see Table 8	defines display status; the possibility to disable the display allows implementation of blinking under external control
								see Table 9	defines power dissipation mode
Load data pointer									
C	0	0	P4	P3	P2	P1	P0	see Table 10	five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
Device select									
C	1	1	0	0	A2	A1	A0	see Table 11	three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses
Bank select									
C	1	1	1	1	0	I	O	see Table 12	defines input bank selection (storage of arriving display data)
								see Table 13	defines output bank selection (retrieval of LCD display data)
									the BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
Blink									
C	1	1	1	0	A	BF1	BF0	see Table 14	defines the blinking frequency
								see Table 15	selects the blinking mode; normal operation with frequency set by bits BF1 and BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Table 5

LCD DRIVE MODE	BIT M1	BIT M0
Static (1 BP)	0	1
1 : 2 MUX (2 BP)	1	0
1 : 3 MUX (3 BP)	1	1
1 : 4 MUX (4 BP)	0	0

Table 6

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the BL55066 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 BL55066s can be distinguished on the same IIC-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable IIC-bus slave address (SA0). It is also possible to cascade up to 16 BL55066s. When cascaded, several BL55066s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the outputs of only one device need to be through-plated to the backplane electrodes of the display. The other BL55066s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig.7).

The SYNC line is provided to maintain the correct synchronization between all cascaded BL55066s. This synchronization is guaranteed after the power-on reset. The only time that SYNC is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when BL55066s with differing SA0 levels are cascaded). SYNC is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A BL55066 asserts the SYNC line at the onset of its last active backplane signal and monitors the SYNC line at all other times.

Should synchronization in the cascade be lost, it will be restored by the first BL55066 to assert SYNC. The timing relationships between the backplane waveforms and the SYNC signal for the various drive modes of the BL55066 are shown in Fig.18. The waveforms are identical with the parent device BL55066. Cascade ability between BL55066s and BL55066s is possible, giving cost effective LCD applications.

Table 7 LCD bias configuration

LCD BIAS	BIT B
1/3 bias	0
1/2 bias	1

Table 8 Display status

DISPLAY STATUS	BIT E
Disabled (blank)	0
Enabled	1

Table 9 Power dissipation mode

MODE	BIT LP
Normal mode	0
Power-saving mode	1

Table 10 Load data pointer

BITS	P4	P3	P2	P1	P0
5-bit binary value of 0 to 23					

Table 11 Device select

BITS	A0	A1	A2
3-bit binary value of 0 to 7			

Table 12 Input bank selection

STATIC	1 : 2 MUX	BIT 1
RAM bit 0	RAM bits 0, 1	0
RAM bit 2	RAM bits 2, 3	1

Table 13 Output bank selection

STATIC	1 : 2 MUX	BIT 0
RAM bit 0	RAM bits 0, 1	0
RAM bit 2	RAM bits 2, 3	1

Table 14 Blinking frequency

BLINK FREQUENCY	BIT BF1	BIT BF0
Off	0	0
2 Hz	0	1
1 Hz	1	0
0.5 Hz	1	1

Table 15 Blink mode selection

BLINK MODE	BIT A
Normal blinking	0
Alternation blinking	1

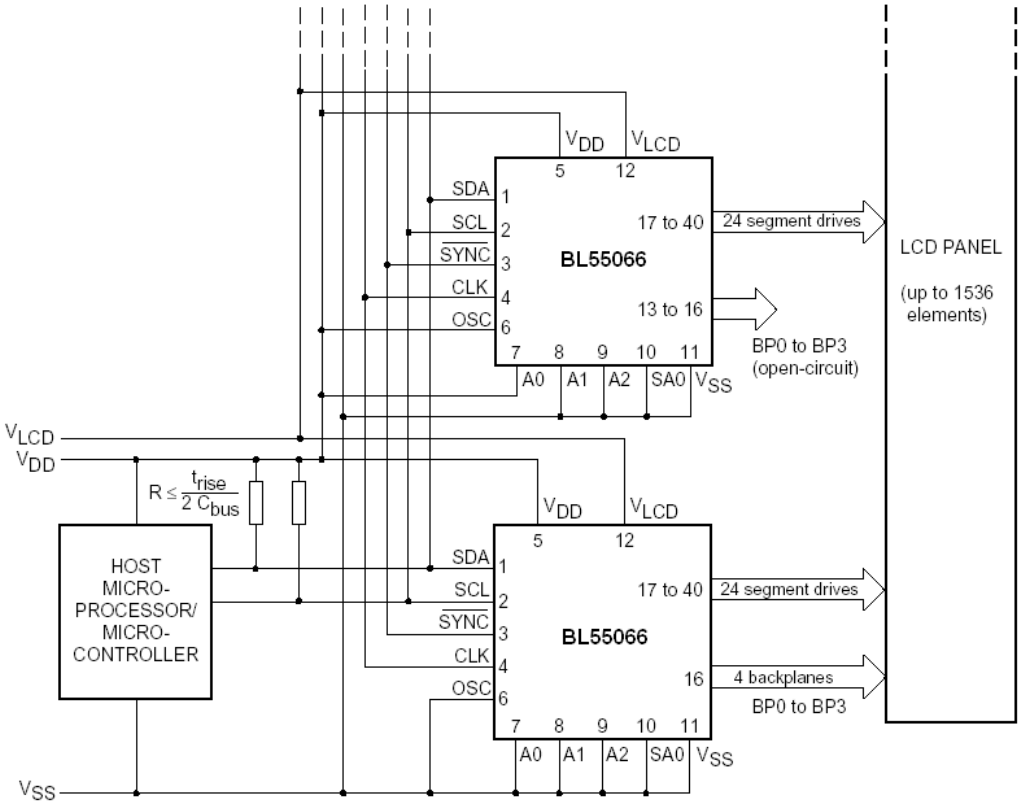

VDD
VLCD
5
12
SDA
SCL
SYNC
CLK
OSC
1
2
3
4
6
BL55066
17 to 40
24 segment drives
13 to 16
BP0 to BP3
(open-circuit)
7
8
9
10
11
A0
A1
A2
SA0
VSS
LCD PANEL
(up to 1536
elements)
VLCD
VDD
R ≤ trise / 2 Cbus
HOST
MICRO-
PROCESSOR/
MICRO-
CONTROLLER
16
4 backplanes
BP0 to BP3
VSS

Fig 7

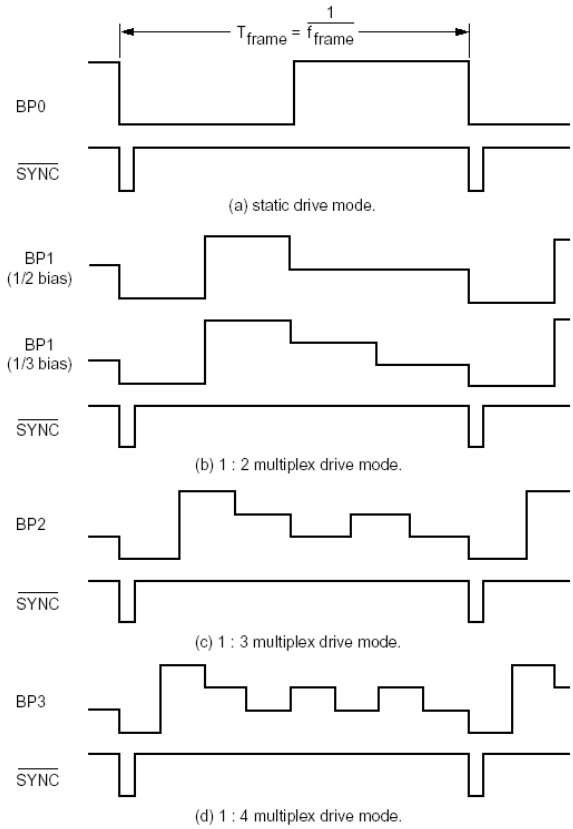

Tframe = 1 / fframe
BP0
SYNC
(a) static drive mode.
BP1
(1/2 bias)
BP1
(1/3 bias)
SYNC
(b) 1 : 2 multiplex drive mode.
BP2
SYNC
(c) 1 : 3 multiplex drive mode.
BP3
SYNC
(d) 1 : 4 multiplex drive mode.

Fig 8

Absolute Maximum Rating

Parameter	Symbol	MIN.	MAX.	Unit
Supply Voltage	V_{DD}	－0.5	+7.0	V
LCD supply voltage	V_{LCD}	V_{DD}－7.0	V_{DD}	V
Input voltage（SCL、SDA、A0～A2、OSC、CLK、$\overline{SYNC}$、SA0）	V_{I1}	V_{SS}－0.5	V_{DD}+0.5	V
Output（S0～S23、BP0～BP3）	V_O	V_{LCD}－0.5	V_{DD}+0.5	V
DC input current	$\pm I_I$	-20	+20	mA
DC output current	$\pm I_O$	-25	+25	mA
V_{DD}、V_{SS} or V_{LCD} current	$\pm I_{DD}$、$\pm I_{SS}$、$\pm I_{LCD}$	-50	+50	mA
Power dissapation per package	P_{tot}	-	400	mW
Power dissapation per output	P_O	-	100	mW
Storage temperature	T_{atg}	－65	+150	℃

Table 16

DC Characteristic

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage	V_{DD}	2.5	-	6	V
LCD supply voltage	V_{LCD}	V_{DD}－6	-	V_{DD}－2.5	V
Operating supply current（Normal mode），f_{LCD}=200kHz （1）	I_{DD}	-	25	90	μA
Power saving mode supplycurrent，V_{DD}=3.5V，V_{LCD}=0V，f_{CLK}=35kHz 1）	I_{LP}	-	12	40	μA
Logic					
Low level input voltage	V_{IL}	V_{SS}	-	0.3 V_{DD}	V
High level input voltage （SDA,SCL, CLK, SYNC ,SA0,OSC,A0 to A2）	V_{IH1}	0.7V_{DD}	-	V_{DD}	V
Low level output voltage（IO=0mA）	V_{OL}	-	-	0.05	V
High level output voltage（IO=0mA）	V_{OH}	V_{DD}－0.05	-	-	V
Low level output current（CLK，SYNC），V_{OL}=1V, V_{DD}=5V	I_{OL1}	1	-	-	mA
High level output current（CLK），V_{OH}=4V, V_{DD}=5V	I_{OH}	-	-	-1	mA
Low level output current（SDA，SCL），V_{OL}=0.4V, V_{DD}=5V	I_{OL2}	3	-	-	mA
Leakage current（SA0，A0～A2，CLK，SCL，SDA），V_I=V_{ss} or V_{DD}	$\pm I_{L1}$	-1	-	+1	μA
Leakage current（OSC），V_I=V_{DD}	$\pm I_{12}$	-1	-	+1	μA
Pull down current（A0,A1,A2,OSC）V_I=1V; V_{DD}=5V	I_{pd}	15	50	150	μA
Pull up resistor（SYNC）	R_{SYNC}	15	25	60	kΩ
Powron reset level （2）	V_{REF}	-	1.3	2	V

Tolerable spike width on bus	t_{SW}	-	-	100	ns
Input capacitance（3）	C_I	-	-	7	pF
LCD output					
DC voltage component（BP0～BP3），C_{BP}=35nF	$\pm V_{BP}$	-20	-	＋20	mV
DC voltage component（S0～S23），C_S=5nF	$\pm V_S$	-20	-	＋20	mV
Output impedance（BP0～BP3），$V_{LCD}=V_{DD}$-5V （4）	R_{BP}	-	1	5	kΩ
Output impedance（S0～S23），$V_{LCD}=V_{DD}$-5V （4）	R_S	-	3	7	kΩ

Table 17

Notes

1. Outputs open; inputs at VSS or VDD; external clock with 50% duty factor; I2C-bus inactive.
2. Resets all logic when VDD < Vref.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.

AC Characteristic

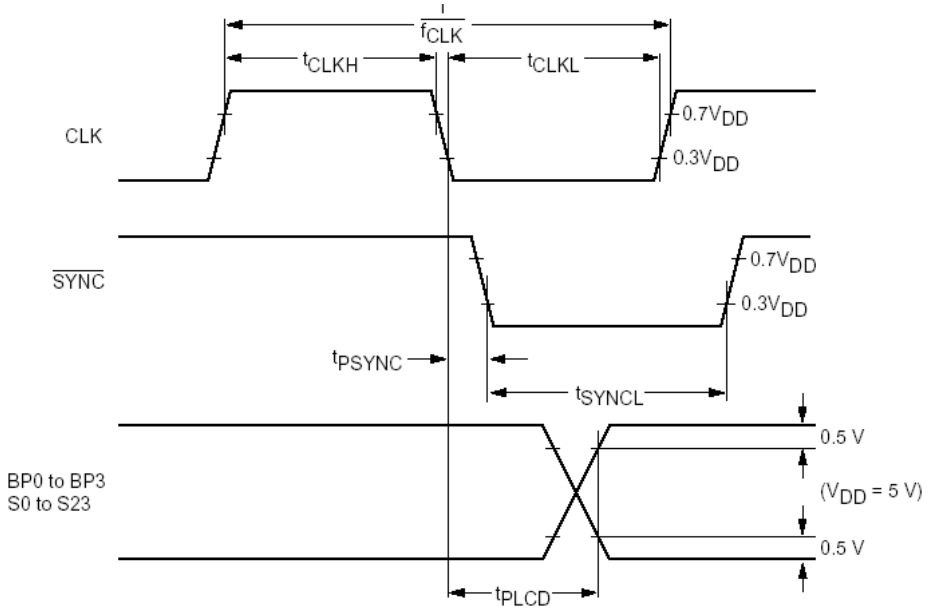
Ta=25°C

Parameter	Symbol	Min	Typ	Max	Unit
Oscilator frequency（Normal mode）V_{DD}=5V	f_{clk}	125	200	315	kHz
Oscilator frequency（Power saving mode）V_{DD}=3.5V	f_{clkP}	21	31	48	kHz
CLK high time	t_{clkH}	1	-	-	μs
CLK low time	t_{clkL}	1	-	-	μs
SYNC propagation delay	t_{PSYNC}	-	-	400	ns
SYNC low time	$t_{\overline{SYNCL}}$	1	-	-	μs
Driver delays with load, VLCD=VDD-5V	t_{PLCD}	-	-	30	μs
IIC-bus					
Bus free time	t_{BUF}	4.7	-	-	μs
START condition hold time	$t_{HD;STA}$	4.0	-	-	μs
START condition setup time	$t_{SU;STA}$	4.7	-	-	μs
SCL low time	t_{LOW}	4.7	-	-	μs
SCL high time	t_{HIGH}	4.0	-	-	μs
SCL/SDA rise timr	t_r	-	-	1	μs
SCL/SDA fall time	t_f	-	-	0.3	μs
Line capacitor	C_B	-	-	400	pF
Data setup time	$t_{SU;DAT}$	250	-	-	ns
Data hold time	$t_{HD;DAT}$	0	-	-	μs
STOP condition setup time	$t_{SU;STO}$	4.0	-	-	μs

Table 18

Notes

1. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
2. At f_{CLK} < 125 kHz, I²C-bus maximum transmission speed is derated.



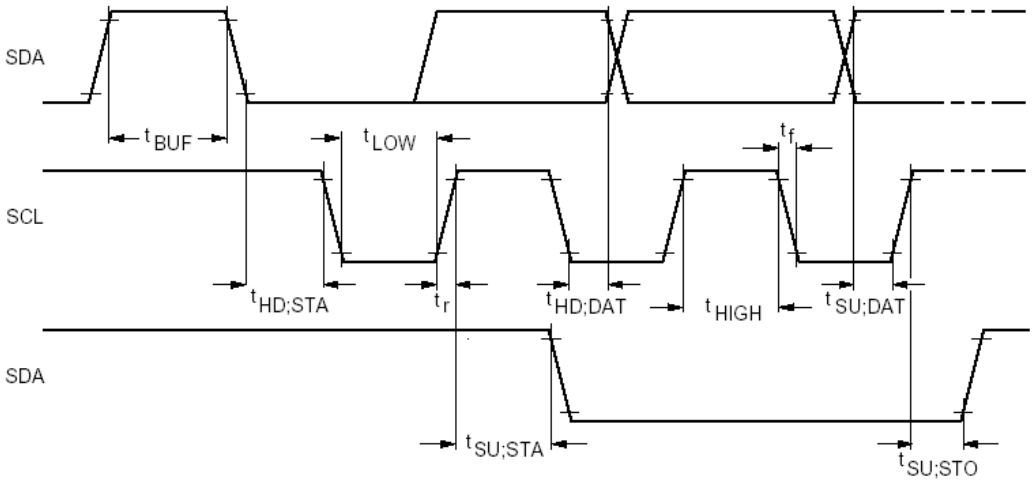


Fig 9

Package Outlines

LQFP44(10x10)

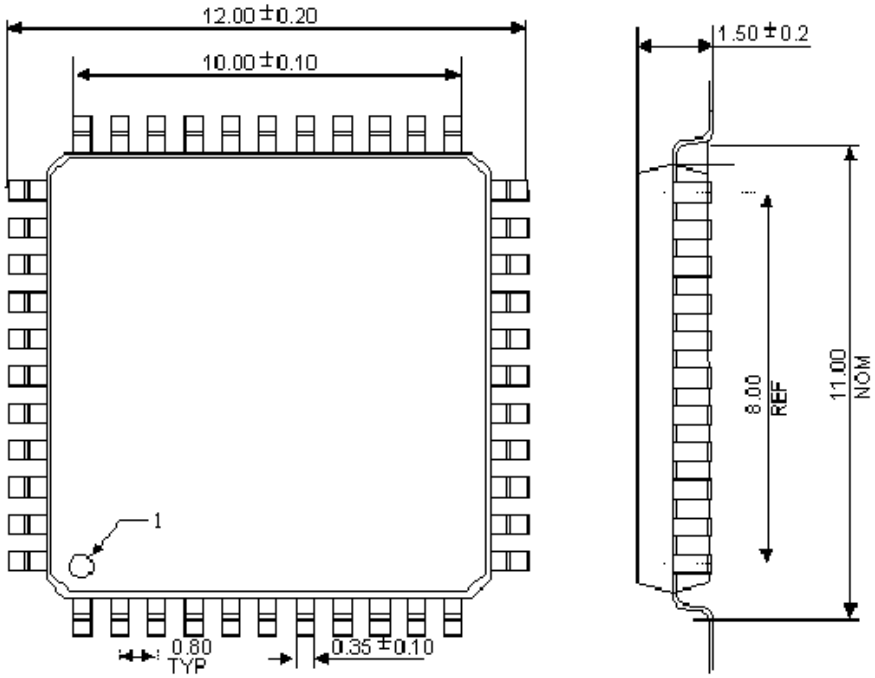


Fig 10