

# DATA SHEET



## **SAA7114**

PAL/NTSC/SECAM video decoder  
with adaptive PAL/NTSC comb  
filter, VBI data slicer and high  
performance scaler

Product specification  
Supersedes data of 2000 Mar 15

2004 Mar 03

# **PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler**

**SAA7114**

|                                                               |           |                                                                                |
|---------------------------------------------------------------|-----------|--------------------------------------------------------------------------------|
| <b>CONTENTS</b>                                               | <b>10</b> | <b>BOUNDARY SCAN TEST</b>                                                      |
| 1 FEATURES                                                    | 10.1      | Initialization of boundary scan circuit                                        |
| 1.1 Video decoder                                             | 10.2      | Device identification codes                                                    |
| 1.2 Video scaler                                              | 11        | LIMITING VALUES                                                                |
| 1.3 Vertical Blanking Interval (VBI) data decoder and slicer  | 12        | THERMAL CHARACTERISTICS                                                        |
| 1.4 Audio clock generation                                    | 13        | CHARACTERISTICS                                                                |
| 1.5 Digital I/O interfaces                                    | 14        | APPLICATION INFORMATION                                                        |
| 1.6 Miscellaneous                                             | 15        | I <sup>2</sup> C-BUS DESCRIPTION                                               |
| 2 APPLICATIONS                                                | 15.1      | I <sup>2</sup> C-bus format                                                    |
| 3 GENERAL DESCRIPTION                                         | 15.2      | I <sup>2</sup> C-bus details                                                   |
| 4 QUICK REFERENCE DATA                                        | 15.3      | Programming register audio clock generation                                    |
| 5 ORDERING INFORMATION                                        | 15.4      | Programming register VBI data slicer                                           |
| 6 BLOCK DIAGRAM                                               | 15.5      | Programming register interfaces and scaler part                                |
| 7 PINNING                                                     | 16        | PROGRAMMING START SET-UP                                                       |
| 8 FUNCTIONAL DESCRIPTION                                      | 16.1      | Decoder part                                                                   |
| 8.1 Decoder                                                   | 16.2      | Audio clock generation part                                                    |
| 8.2 Decoder output formatter                                  | 16.3      | Data slicer and data type control part                                         |
| 8.3 Scaler                                                    | 16.4      | Scaler and interfaces                                                          |
| 8.4 VBI data decoder and capture (subaddresses 40H to 7FH)    | 17        | PACKAGE OUTLINES                                                               |
| 8.5 Image port output formatter (subaddresses 84H to 87H)     | 18        | SOLDERING                                                                      |
| 8.6 Audio clock generation (subaddresses 30H to 3FH)          | 18.1      | Introduction to soldering surface mount packages                               |
| 9 INPUT/OUTPUT INTERFACES AND PORTS                           | 18.2      | Reflow soldering                                                               |
| 9.1 Analog terminals                                          | 18.3      | Wave soldering                                                                 |
| 9.2 Audio clock signals                                       | 18.4      | Manual soldering                                                               |
| 9.3 Clock and real-time synchronization signals               | 18.5      | Suitability of surface mount IC packages for wave and reflow soldering methods |
| 9.4 Video expansion port (X port)                             | 19        | DATA SHEET STATUS                                                              |
| 9.5 Image port (I port)                                       | 20        | DEFINITIONS                                                                    |
| 9.6 Host port for 16-bit extension of video data I/O (H port) | 21        | DISCLAIMERS                                                                    |
| 9.7 Basic input and output timing diagrams I port and X port  | 22        | PURCHASE OF PHILIPS I <sup>2</sup> C COMPONENTS                                |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 1 FEATURES

### 1.1 Video decoder

- Six analog inputs, internal analog source selectors, e.g.  $6 \times$  CVBS or  $(2 \times$  Y/C and  $2 \times$  CVBS) or  $(1 \times$  Y/C and  $4 \times$  CVBS)
- Two analog preprocessing channels in differential CMOS style inclusive built-in analog anti-alias filters
- Fully programmable static gain or Automatic Gain Control (AGC) for the selected CVBS or Y/C channel
- Automatic Clamp Control (ACC) for CVBS, Y and C
- Switchable white peak control
- Two 9-bit video CMOS Analog-to-Digital Converters (ADCs), digitized CVBS or Y/C signals are available on the expansion port
- On-chip line-locked clock generation in accordance with "ITU 601"
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources e.g. consumer grade VTR
- Requires only one crystal (32.11 or 24.576 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL B, G, D, H, I and N, combination PAL N, PAL M, NTSC M, NTSC-Japan, NTSC 4.43 and SECAM
- Adaptive 2/4-line comb filter for two dimensional chrominance/luminance separation:
  - Increased luminance and chrominance bandwidth for all PAL and NTSC standards
  - Reduced cross colour and cross luminance artefacts
- PAL delay line for correcting PAL phase errors
- Independent Brightness Contrast Saturation (BCS) adjustment for decoder part
- User programmable sharpness control
- Independent gain and offset adjustment for raw data path.



### 1.2 Video scaler

- Horizontal and vertical downscaling and upscaling to randomly sized windows
- Horizontal and vertical scaling range: variable zoom to  $\frac{1}{64}$  (icon) (it should be noted that the H and V zoom are restricted by the transfer data rates)
- Anti-alias and accumulating filter for horizontal scaling
- Vertical scaling with linear phase interpolation and accumulating filter for anti-aliasing (6-bit phase accuracy)
- Horizontal phase correct up and downscaling for improved signal quality of scaled data, especially for compression and video phone applications, with 6-bit phase accuracy (1.2 ns step width)
- Two independent programming sets for scaler part, to define two 'ranges' per field or sequences over frames
- Fieldwise switching between decoder part and expansion port (X port) input
- Brightness, contrast and saturation controls for scaled outputs.

### 1.3 Vertical Blanking Interval (VBI) data decoder and slicer

- Versatile VBI data decoder, slicer, clock regeneration and byte synchronization e.g. for World Standard Teletext (WST), North American Broadcast Text System (NABTS), close caption, Wide Screen Signalling (WSS), etc.

### 1.4 Audio clock generation

- Generation of a field-locked audio master clock to support a constant number of audio clocks per video field
- Generation of an audio serial and left/right (channel) clock signal.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 1.5 Digital I/O interfaces

- Real-time signal port (R port), inclusive continuous line-locked reference clock and real-time status information supporting RTC level 3.1 (refer to document “*RTC Functional Specification*” for details)
- Bidirectional expansion port (X port) with half duplex functionality (D1), 8-bit Y-C<sub>B</sub>-C<sub>R</sub>:
  - Output from decoder part, real-time and unscaled
  - Input to scaler part, e.g. video from MPEG decoder (extension to 16-bit possible)
- Video image port (I port) configurable for 8-bit data (extension to 16-bit possible) in master mode (own clock), or slave mode (external clock), with auxiliary timing and handshake signals
- Discontinuous data streams supported
- 32-word × 4-byte FIFO register for video output data
- 28-word × 4-byte FIFO register for decoded VBI data output
- Scaled 4 : 2 : 2, 4 : 1 : 1, 4 : 2 : 0, 4 : 1 : 0 Y-C<sub>B</sub>-C<sub>R</sub> output
- Scaled 8-bit luminance only and raw CVBS data output
- Sliced, decoded VBI data output.

## 1.6 Miscellaneous

- Power-on control
- 5 V tolerant digital inputs and I/O ports
- Software controlled power saving standby modes supported
- Programming via serial I<sup>2</sup>C-bus, full read back ability by an external controller, bit rate up to 400 kbits/s
- Boundary scan test circuit complies with the “*IEEE Std. 1149.b1 - 1994*”.

## 2 APPLICATIONS

- Desktop video
- Multimedia
- Digital television
- Image processing
- Video phone applications.

## 3 GENERAL DESCRIPTION

The SAA7114 is a video capture device for applications at the image port of VGA controllers.

The SAA7114 is a combination of a two-channel analog preprocessing circuit including source selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multistandard decoder containing two-dimensional chrominance/luminance separation by an adaptive comb filter and a high performance scaler, including variable horizontal and vertical up and downscaling and a brightness, contrast and saturation control circuit.

It is a highly integrated circuit for desktop video and similar applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU 601 compatible colour component values. The SAA7114 accepts CVBS or S-video (Y/C) as analog inputs from TV or VCR sources, including weak and distorted signals. An expansion port (X port) for digital video (bidirectional half duplex, D1 compatible) is also supported to connect to MPEG or a video phone codec. At the so called image port (I port) the SAA7114 supports 8 or 16-bit wide output data with auxiliary reference data for interfacing to VGA controllers.

The target application for the SAA7114 is to capture and scale video images, to be provided as a digital video stream through the image port of a VGA controller, for display via the frame buffer of the VGA, or for capture to system memory.

In parallel SAA7114 also incorporates provisions for capturing the serially coded data in the vertical blanking interval (VBI data). Two principal functions are available:

1. To capture raw video samples, after interpolation to the required output data rate, via the scaler
2. A versatile data slicer (data recovery) unit.

The SAA7114 also incorporates field-locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a field, or a set of fields. This prevents the loss of synchronization between video and audio during capture or playback.

The circuit is I<sup>2</sup>C-bus controlled (full write/read capability for all programming registers, bit rate up to 400 kbits/s).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 4 QUICK REFERENCE DATA

| SYMBOL              | PARAMETER                            | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------------|--------------------------------------|------------|------|------|------|------|
| V <sub>DDD</sub>    | digital supply voltage               |            | 3.0  | 3.3  | 3.6  | V    |
| V <sub>DDD(C)</sub> | digital core supply voltage          |            | 3.0  | 3.3  | 3.6  | V    |
| V <sub>DDA</sub>    | analog supply voltage                |            | 3.1  | 3.3  | 3.5  | V    |
| T <sub>amb</sub>    | ambient temperature                  |            | 0    | –    | 70   | °C   |
| P <sub>A+D</sub>    | analog and digital power dissipation | note 1     | –    | 0.45 | –    | W    |

### Note

- Power dissipation is measured in CVBS input mode (only one ADC active) and 8-bit image port output mode, expansion port is 3-stated.

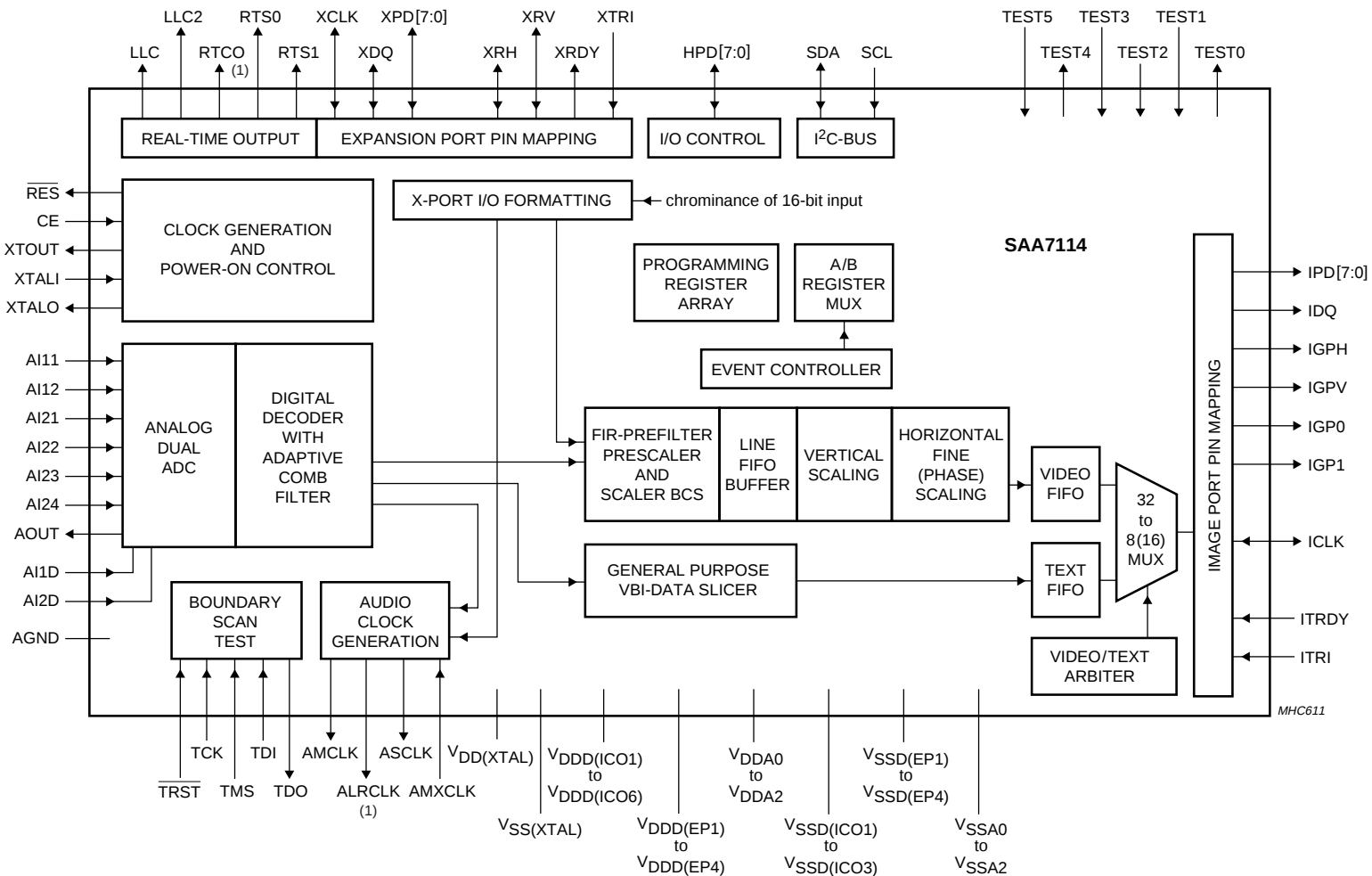
## 5 ORDERING INFORMATION

| TYPE<br>NUMBER | PACKAGE |                                                                         |          |
|----------------|---------|-------------------------------------------------------------------------|----------|
|                | NAME    | DESCRIPTION                                                             | VERSION  |
| SAA7114E       | BGA156  | plastic ball grid array package; 156 balls; body 15 × 15 × 1.15 mm      | SOT472-1 |
| SAA7114H       | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 6 BLOCK DIAGRAM



(1) The pins RTCO and ALRCLK are used for configuration of the I²C-bus interface and the definition of the crystal oscillator frequency at RESET (pin strapping).

Fig.1 Block diagram.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 7 PINNING

| SYMBOL                 | PIN     |          | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                    |
|------------------------|---------|----------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
|                        | LQFP100 | BGA156   |                     |                                                                                                                                                |
| V <sub>DDD(EP1)</sub>  | 1       | L7       | P                   | external digital pad supply voltage 1 (+3.3 V)                                                                                                 |
| TDO                    | 2       | N5       | O                   | test data output for boundary scan test; note 2                                                                                                |
| TDI                    | 3       | N6       | I/pu                | test data input for boundary scan test; note 2                                                                                                 |
| XTOUT                  | 4       | P4       | O                   | crystal oscillator output signal; auxiliary signal                                                                                             |
| V <sub>SS(XTAL)</sub>  | 5       | P5       | P                   | ground for crystal oscillator                                                                                                                  |
| XTALO                  | 6       | P3       | O                   | 24.576 MHz (32.11 MHz) crystal oscillator output; not connected if TTL clock input of XTALI is used                                            |
| XTALI                  | 7       | P2       | I                   | input terminal for 24.576 MHz (32.11 MHz) crystal oscillator or connection of external oscillator with TTL compatible square wave clock signal |
| V <sub>DD(XTAL)</sub>  | 8       | L8       | P                   | supply voltage for crystal oscillator                                                                                                          |
| V <sub>SSA2</sub>      | 9       | M7, N7   | P                   | ground for analog inputs AI2n                                                                                                                  |
| AI24                   | 10      | P6       | I                   | analog input 24                                                                                                                                |
| V <sub>DDA2</sub>      | 11      | M8       | P                   | analog supply voltage for analog inputs AI2n (+3.3 V)                                                                                          |
| AI23                   | 12      | P7       | I                   | analog input 23                                                                                                                                |
| AI2D                   | 13      | P8       | I                   | differential input for ADC channel 2 (pins AI24, AI23, AI22 and AI21)                                                                          |
| AI22                   | 14      | P9       | I                   | analog input 22                                                                                                                                |
| V <sub>SSA1</sub>      | 15      | N8, N9   | P                   | ground for analog inputs AI1n                                                                                                                  |
| AI21                   | 16      | P10      | I                   | analog input 21                                                                                                                                |
| V <sub>DDA1</sub>      | 17      |          | P                   | analog supply voltage for analog inputs AI1n (+3.3 V)                                                                                          |
| AI12                   | 18      | P11      | I                   | analog input 12                                                                                                                                |
| AI1D                   | 19      | P12      | I                   | differential input for ADC channel 1 (pins AI12 and AI11)                                                                                      |
| AI11                   | 20      | P13      | I                   | analog input 11                                                                                                                                |
| AGND                   | 21      | N10      | P                   | analog ground connection                                                                                                                       |
| AOUT                   | 22      | M10      | O                   | do not connect; analog test output                                                                                                             |
| V <sub>DDA0</sub>      | 23      | N11      | P                   | analog supply voltage (+3.3 V) for internal Clock Generation Circuit (CGC)                                                                     |
| V <sub>SSA0</sub>      | 24      | N12, N13 | P                   | ground for internal clock generation circuit                                                                                                   |
| V <sub>DDD(EP2)</sub>  | 25      | L9       | P                   | external digital pad supply voltage 2 (+3.3 V)                                                                                                 |
| V <sub>SSD(EP1)</sub>  | 26      | M13      | P                   | external digital pad supply ground 1                                                                                                           |
| CE                     | 27      | N14      | I/pu                | chip enable or reset input (with internal pull-up)                                                                                             |
| LLC                    | 28      | M14      | O                   | line-locked system clock output (27 MHz nominal)                                                                                               |
| LLC2                   | 29      | L14      | O                   | line-locked ½ clock output (13.5 MHz nominal)                                                                                                  |
| RES                    | 30      | M12      | O                   | reset output (active LOW)                                                                                                                      |
| SCL                    | 31      | M11      | I(O)                | serial clock input (I <sup>2</sup> C-bus) with inactive output path                                                                            |
| SDA                    | 32      | L12      | I/O                 | serial data input/output (I <sup>2</sup> C-bus)                                                                                                |
| V <sub>DDD(IC01)</sub> | 33      | L11      | P                   | internal digital core supply voltage 1 (+3.3 V)                                                                                                |
| RTS0                   | 34      | K13      | O                   | real-time status or sync information, controlled by subaddresses 11H and 12H; see Section 15.2.18, 15.2.19 and 15.2.20                         |
| RTS1                   | 35      | L10      | O                   |                                                                                                                                                |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| SYMBOL                 | PIN     |        | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                       |
|------------------------|---------|--------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                        | LQFP100 | BGA156 |                     |                                                                                                                                                                                                                                                                                                                                                                   |
| RTCO                   | 36      | L13    | (I/O)               | real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence (see external document “ <i>RTC Functional Description</i> ”, available on request); the RTCO pin is enabled via I <sup>2</sup> C-bus bit RTCE; see Table 36 and notes 3 and 4 |
| AMCLK                  | 37      | K12    | O                   | audio master clock output, up to 50% of crystal clock                                                                                                                                                                                                                                                                                                             |
| V <sub>SSD(ICO1)</sub> | 38      | K11    | P                   | internal digital core supply ground 1                                                                                                                                                                                                                                                                                                                             |
| ASCLK                  | 39      | K14    | O                   | audio serial clock output                                                                                                                                                                                                                                                                                                                                         |
| ALRCLK                 | 40      | J13    | (I/O)               | audio left/right clock output; can be strapped to supply via a 3.3 k $\Omega$ resistor to indicate that the default 24.576 MHz crystal (ALRCLK = 0; internal pull-down) has been replaced by a 32.110 MHz crystal (ALRCLK = 1); notes 3 and 5                                                                                                                     |
| AMXCLK                 | 41      | J12    | I                   | audio master external clock input                                                                                                                                                                                                                                                                                                                                 |
| ITRDY                  | 42      | J14    | I/pu                | target ready input, image port (with internal pull-up)                                                                                                                                                                                                                                                                                                            |
| V <sub>DDD(ICO2)</sub> | 43      | J11    | P                   | internal digital core supply voltage 2 (+3.3 V)                                                                                                                                                                                                                                                                                                                   |
| TEST0                  | 44      | H13    | O                   | do not connect; reserved for future extensions and for testing: scan output                                                                                                                                                                                                                                                                                       |
| ICLK                   | 45      | H12    | I/O                 | clock output signal for image port, or optional asynchronous back-end clock input                                                                                                                                                                                                                                                                                 |
| IDQ                    | 46      | H14    | O                   | output data qualifier for image port (optional: gated clock output)                                                                                                                                                                                                                                                                                               |
| ITRI                   | 47      | G14    | I(O)                | image port output control signal, effects all input port pins inclusive ICLK, enable and active polarity is under software control (bits IPE in subaddress 87H); output path used for testing: scan output                                                                                                                                                        |
| IGP0                   | 48      | F14    | O                   | general purpose output signal 0; image port (controlled by subaddresses 84H and 85H)                                                                                                                                                                                                                                                                              |
| IGP1                   | 49      | G13    | O                   | general purpose output signal 1; image port (controlled by subaddresses 84H and 85H)                                                                                                                                                                                                                                                                              |
| V <sub>SSD(EP2)</sub>  | 50      | H11    | P                   | external digital pad supply ground 2                                                                                                                                                                                                                                                                                                                              |
| V <sub>DDD(EP3)</sub>  | 51      | G11    | P                   | external digital pad supply voltage 3 (+3.3 V)                                                                                                                                                                                                                                                                                                                    |
| IGPV                   | 52      | F13    | O                   | multi purpose vertical reference output signal; image port (controlled by subaddresses 84H and 85H)                                                                                                                                                                                                                                                               |
| IGPH                   | 53      | G12    | O                   | multi purpose horizontal reference output signal; image port (controlled by subaddresses 84H and 85H)                                                                                                                                                                                                                                                             |
| IPD7                   | 54      | E14    | O                   | MSB of image port data output                                                                                                                                                                                                                                                                                                                                     |
| IPD6                   | 55      | D14    | O                   | MSB – 1 of image port data output                                                                                                                                                                                                                                                                                                                                 |
| IPD5                   | 56      | C14    | O                   | MSB – 2 of image port data output                                                                                                                                                                                                                                                                                                                                 |
| IPD4                   | 57      | B14    | O                   | MSB – 3 of image port data output                                                                                                                                                                                                                                                                                                                                 |
| V <sub>DDD(ICO3)</sub> | 58      | F11    | P                   | internal digital core supply voltage 3 (+3.3 V)                                                                                                                                                                                                                                                                                                                   |
| IPD3                   | 59      | E13    | O                   | MSB – 4 of image port data output                                                                                                                                                                                                                                                                                                                                 |
| IPD2                   | 60      | D13    | O                   | MSB – 5 of image port data output                                                                                                                                                                                                                                                                                                                                 |
| IPD1                   | 61      | C13    | O                   | MSB – 6 of image port data output                                                                                                                                                                                                                                                                                                                                 |
| IPD0                   | 62      | B13    | O                   | LSB of image port data output                                                                                                                                                                                                                                                                                                                                     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| SYMBOL                 | PIN     |        | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                     |
|------------------------|---------|--------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                        | LQFP100 | BGA156 |                     |                                                                                                                                                                                 |
| V <sub>SSD(ICO2)</sub> | 63      | E11    | P                   | internal digital core supply ground 2                                                                                                                                           |
| HPD7                   | 64      | A13    | I/O                 | MSB of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                             |
| HPD6                   | 65      | D12    | I/O                 | MSB – 1 of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                         |
| HPD5                   | 66      | C12    | I/O                 | MSB – 2 of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                         |
| HPD4                   | 67      | B12    | I/O                 | MSB – 3 of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                         |
| V <sub>DDD(ICO4)</sub> | 68      | D11    | P                   | internal digital core supply voltage 4 (+3.3 V)                                                                                                                                 |
| HPD3                   | 69      | A12    | I/O                 | MSB – 4 of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                         |
| HPD2                   | 70      | C11    | I/O                 | MSB – 5 of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                         |
| HPD1                   | 71      | B11    | I/O                 | MSB – 6 of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                         |
| HPD0                   | 72      | A11    | I/O                 | LSB of host port data I/O, carries C <sub>B</sub> -C <sub>R</sub> chrominance information in 16-bit video I/O modes                                                             |
| TEST1                  | 73      | B10    | I                   | do not connect; reserved for future extensions and for testing: scan input                                                                                                      |
| TEST2                  | 74      | C10    | I                   | do not connect; reserved for future extensions and for testing: scan input                                                                                                      |
| V <sub>DDD(EP4)</sub>  | 75      | D10    | P                   | external digital pad supply voltage 4 (+3.3 V)                                                                                                                                  |
| V <sub>SSD(EP3)</sub>  | 76      | H4     | P                   | external digital pad supply ground 3                                                                                                                                            |
| TEST3                  | 77      | J3     | I                   | do not connect; reserved for future extensions and for testing: scan input                                                                                                      |
| TEST4                  | 78      | J1     | O                   | do not connect; reserved for future extensions and for testing: scan output                                                                                                     |
| TEST5                  | 79      | J2     | I                   | do not connect; reserved for future extensions and for testing: scan input                                                                                                      |
| XTRI                   | 80      | K1     | I                   | X port output control signal, affects all X port pins (XPD7 to XPD0, XRH, XRV, XDQ and XCLK), enable and active polarity is under software control (bits XPE in subaddress 83H) |
| XPD7                   | 81      | K2     | I/O                 | MSB of expansion port data                                                                                                                                                      |
| XPD6                   | 82      | K3     | I/O                 | MSB – 1 of expansion port data                                                                                                                                                  |
| V <sub>DDD(ICO5)</sub> | 83      | J4     | P                   | internal digital core supply voltage 5 (+3.3 V)                                                                                                                                 |
| XPD5                   | 84      | L1     | I/O                 | MSB – 2 of expansion port data                                                                                                                                                  |
| XPD4                   | 85      | L2     | I/O                 | MSB – 3 of expansion port data                                                                                                                                                  |
| XPD3                   | 86      | L3     | I/O                 | MSB – 4 of expansion port data                                                                                                                                                  |
| XPD2                   | 87      | M1     | I/O                 | MSB – 5 of expansion port data                                                                                                                                                  |
| V <sub>SSD(ICO3)</sub> | 88      | K4     | P                   | internal digital core supply ground 3                                                                                                                                           |
| XPD1                   | 89      | M2     | I/O                 | MSB – 6 of expansion port data                                                                                                                                                  |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

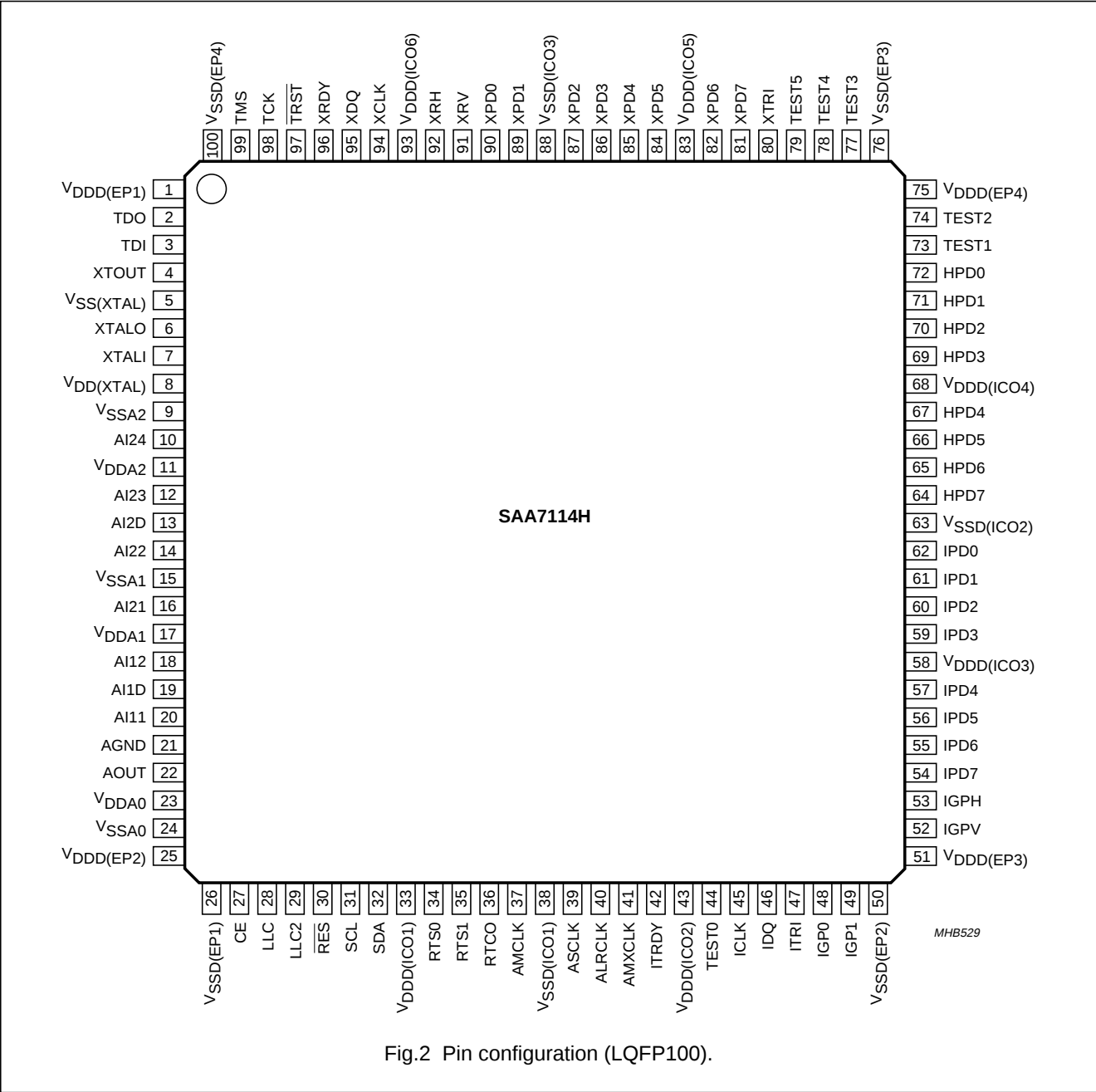
| SYMBOL                | PIN     |        | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                  |
|-----------------------|---------|--------|---------------------|----------------------------------------------------------------------------------------------|
|                       | LQFP100 | BGA156 |                     |                                                                                              |
| XPD0                  | 90      | N1     | I/O                 | LSB of expansion port data                                                                   |
| XRV                   | 91      | L5     | I/O                 | vertical reference I/O expansion port                                                        |
| XRH                   | 92      | N2     | I/O                 | horizontal reference I/O expansion port                                                      |
| V <sub>DD(ICO6)</sub> | 93      | L4     | P                   | internal digital core supply voltage 6 (+3.3 V)                                              |
| XCLK                  | 94      | M3     | I/O                 | clock I/O expansion port                                                                     |
| XDQ                   | 95      | M4     | I/O                 | data qualifier I/O expansion port                                                            |
| XRDY                  | 96      | N3     | O                   | task flag or ready signal from scaler, controlled by XRQT                                    |
| TRST                  | 97      | N4     | I/pu                | test reset input (active LOW), for boundary scan test (with internal pull-up); notes 6 and 7 |
| TCK                   | 98      | M6     | I/pu                | test clock for boundary scan test; note 2                                                    |
| TMS                   | 99      | M5     | I/pu                | test mode select input for boundary scan test or scan test; note 2                           |
| V <sub>SSD(EP4)</sub> | 100     | L6     | P                   | external digital pad supply ground 4                                                         |

## Notes

1. I = input, O = output, P = power, pu = pull-up.
2. In accordance with the "IEEE1149.1" standard the pads TDI, TMS, TCK and TRST are input pads with an internal pull-up transistor and TDO is a 3-state output pad.
3. Pin strapping is done by connecting the pin to the supply via a 3.3 kΩ resistor. During the power-up reset sequence the corresponding pins are switched to input mode to read the strapping level. For the default setting no strapping resistor is necessary (internal pull-down).
4. Pin RTCO operates as I<sup>2</sup>C-bus slave address pin; RTCO = 0 slave address 42H/43H (default); RTCO = 1 slave address 40H/41H.
5. Pin ALRCLK: 0 = 24.576 MHz crystal (default); 1 = 32.110 MHz crystal.
6. For board design without boundary scan implementation connect the TRST pin to ground.
7. This pin provides easy initialization of the Boundary Scan Test (BST) circuit. TRST can be used to force the Test Access Port (TAP) controller to the TEST\_LOGIC\_RESET state (normal operation) at once.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

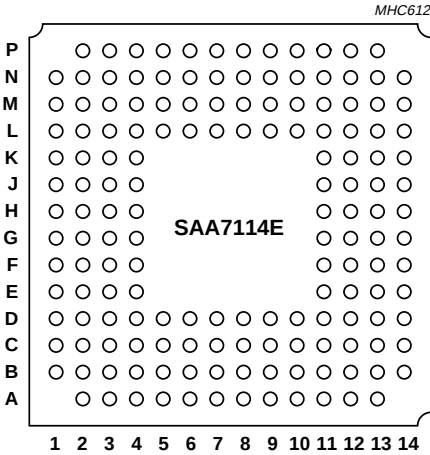


Fig.3 Pin configuration (BGA156).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

**SAA7114**
**Table 1** Pin assignment (top view)

|          | 1     | 2     | 3     | 4                        | 5                      | 6                      | 7                      | 8                      | 9                      | 10                     | 11                      | 12                      | 13                     | 14    |
|----------|-------|-------|-------|--------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|-------------------------|-------------------------|------------------------|-------|
| <b>A</b> |       | n.c.  | n.c.  | n.c.                     | n.c.                   | n.c.                   | n.c.                   | n.c.                   | n.c.                   | n.c.                   | HPD0                    | HPD3                    | HPD7                   |       |
| <b>B</b> | n.c.  | n.c.  | n.c.  | n.c.                     | n.c.                   | n.c.                   | n.c.                   | n.c.                   | n.c.                   | TEST1                  | HPD1                    | HPD4                    | IPD0                   | IPD4  |
| <b>C</b> | n.c.  | n.c.  | n.c.  | n.c.                     | n.c.                   | n.c.                   | n.c.                   | n.c.                   | n.c.                   | TEST2                  | HPD2                    | HPD5                    | IPD1                   | IPD5  |
| <b>D</b> | n.c.  | n.c.  | n.c.  | n.c.                     | n.c.                   | n.c.                   | n.c.                   | n.c.                   | n.c.                   | V <sub>DDD</sub> (EP4) | V <sub>DDD</sub> (IC04) | HPD6                    | IPD2                   | IPD6  |
| <b>E</b> | n.c.  | n.c.  | n.c.  | n.c.                     |                        |                        |                        |                        |                        |                        | V <sub>SSD</sub> (IC02) | n.c.                    | IPD3                   | IPD7  |
| <b>F</b> | n.c.  | n.c.  | n.c.  | n.c.                     |                        |                        |                        |                        |                        |                        | V <sub>DDD</sub> (IC03) | n.c.                    | IGPV                   | IGP0  |
| <b>G</b> | n.c.  | n.c.  | n.c.  | n.c.                     |                        |                        |                        |                        |                        |                        | V <sub>DDD</sub> (EP3)  | IGPH                    | IGP1                   | ITRI  |
| <b>H</b> | n.c.  | n.c.  | n.c.  | V <sub>SSD</sub> (EP3)   |                        |                        |                        |                        |                        |                        | V <sub>SSD</sub> (EP2)  | ICLK                    | TEST0                  | IDQ   |
| <b>J</b> | TEST4 | TEST5 | TEST3 | V <sub>DDD</sub> (IC05)  |                        |                        |                        |                        |                        |                        | V <sub>DDD</sub> (IC02) | AMXCLK                  | ALRCLK                 | ITRDY |
| <b>K</b> | XTRI  | XPD7  | XPD6  | V <sub>SSD</sub> (IC03)  |                        |                        |                        |                        |                        |                        | V <sub>SSD</sub> (IC01) | AMCLK                   | RTS0                   | ASCLK |
| <b>L</b> | XPD5  | XPD4  | XPD3  | V <sub>DDD</sub> (IC06)  | XRv                    | V <sub>SSD</sub> (EP4) | V <sub>DDD</sub> (EP1) | V <sub>DD</sub> (XTAL) | V <sub>DDD</sub> (EP2) | RTS1                   | V <sub>DDD</sub> (IC01) | SDA                     | RTCO                   | LLC2  |
| <b>M</b> | XPD2  | XPD1  | XCLK  | XDQ                      | TMS                    | TCK                    | V <sub>SSA2</sub>      | V <sub>DDA2</sub>      | V <sub>DDA1</sub>      | AOUT                   | SCL                     | $\overline{\text{RES}}$ | V <sub>SSD</sub> (EP1) | LLC   |
| <b>N</b> | XPD0  | XRH   | XRDY  | $\overline{\text{TRST}}$ | TDO                    | TDI                    |                        | V <sub>SSA1</sub>      |                        | AGND                   | V <sub>DDA0</sub>       | V <sub>SSA0</sub>       |                        | CE    |
| <b>P</b> |       | XTALI | XTALO | XTOUT                    | V <sub>SS</sub> (XTAL) | AI24                   | AI23                   | AI2D                   | AI22                   | AI21                   | AI12                    | AI1D                    | AI11                   |       |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

**SAA7114**
**Table 2** 8-bit/16-bit and alternative pin function configurations

| PIN <sup>(1)</sup>                                                        | SYMBOL          | 8-BIT<br>INPUT<br>MODES          | 16-BIT INPUT<br>MODES (ONLY<br>FOR I <sup>2</sup> C-BUS<br>PROGRAMMING) | ALTERNATIVE<br>INPUT<br>FUNCTIONS | 8-BIT<br>OUTPUT<br>MODES                                  | 16-BIT OUTPUT<br>MODES (ONLY<br>FOR I <sup>2</sup> C-BUS<br>PROGRAMMING) | ALTERNATIVE<br>OUTPUT<br>FUNCTIONS | I/O<br>CONFIGURATION<br>PROGRAMMING<br>BITS                           |
|---------------------------------------------------------------------------|-----------------|----------------------------------|-------------------------------------------------------------------------|-----------------------------------|-----------------------------------------------------------|--------------------------------------------------------------------------|------------------------------------|-----------------------------------------------------------------------|
| K2, K3,<br>L1 to L3,<br>M1, M2,<br>N1 (81,<br>82, 84 to<br>87, 89,<br>90) | XPD7 to<br>XPD0 | D1 data<br>input                 | Y data input                                                            |                                   | D1<br>decoder<br>output                                   |                                                                          |                                    | XCODE[92H[3]]<br>XPE[1:0] 83H[1:0]<br>+ pin XTRI                      |
| M3 (94)                                                                   | XCLK            | clock<br>input                   |                                                                         | gated clock<br>input              | decoder<br>clock<br>output                                |                                                                          |                                    | XPE[1:0] 83H[1:0]<br>+ pin XTRI<br>XPCK[1:0] 83H[5:4]<br>XCKS[92H[0]] |
| M4 (95)                                                                   | XDQ             | data<br>qualifier<br>input       |                                                                         |                                   | data<br>qualifier<br>output<br>(HREF and<br>VREF<br>gate) |                                                                          |                                    | XDQ[92H[1]]<br>XPE[1:0] 83H[1:0]<br>+ pin XTRI                        |
| N3 (96)                                                                   | XRDY            | input<br>ready<br>output         |                                                                         | active task A/B<br>flag           |                                                           |                                                                          |                                    | XRQT[83H[2]]<br>XPE[1:0] 83H[1:0]<br>+ pin XTRI                       |
| N2 (92)                                                                   | XRH             | horizontal<br>reference<br>input |                                                                         |                                   | decoder<br>horizontal<br>reference<br>output              |                                                                          |                                    | XDH[92H[2]]<br>XPE[1:0] 83H[1:0]<br>+ pin XTRI                        |
| L5 (91)                                                                   | XRV             | vertical<br>reference<br>input   |                                                                         |                                   | decoder<br>vertical<br>reference<br>output                |                                                                          |                                    | XDV[1:0] 92H[5:4]<br>XPE[1:0] 83H[1:0]<br>+ pin XTRI                  |
| K1 (80)                                                                   | XTRI            | output<br>enable<br>input        |                                                                         |                                   |                                                           |                                                                          |                                    | XPE[1:0] 83H[1:0]                                                     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

**SAA7114**

| PIN <sup>(1)</sup>                                                                  | SYMBOL          | 8-BIT<br>INPUT<br>MODES | 16-BIT INPUT<br>MODES (ONLY<br>FOR I <sup>2</sup> C-BUS<br>PROGRAMMING) | ALTERNATIVE<br>INPUT<br>FUNCTIONS | 8-BIT<br>OUTPUT<br>MODES    | 16-BIT OUTPUT<br>MODES (ONLY<br>FOR I <sup>2</sup> C-BUS<br>PROGRAMMING) | ALTERNATIVE<br>OUTPUT<br>FUNCTIONS          | I/O<br>CONFIGURATION<br>PROGRAMMING<br>BITS                                             |
|-------------------------------------------------------------------------------------|-----------------|-------------------------|-------------------------------------------------------------------------|-----------------------------------|-----------------------------|--------------------------------------------------------------------------|---------------------------------------------|-----------------------------------------------------------------------------------------|
| A13,<br>D12,<br>C12,<br>B12,<br>A12,<br>C11,<br>B11, A11<br>(64 to 67,<br>69 to 72) | HPD7 to<br>HPD0 |                         | C <sub>B</sub> -C <sub>R</sub> data input                               |                                   |                             | C <sub>B</sub> -C <sub>R</sub> scaler<br>output                          |                                             | ICODE[93H[7]]<br>ISWP[1:0] 85H[7:6]<br>I8_16[93H[6]]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI |
| E14,<br>D14,<br>C14,<br>B14,<br>E13,<br>D13,<br>C13, B13<br>(54 to 57,<br>59 to 62) | IPD7 to<br>IPD0 |                         |                                                                         |                                   | D1 scaler<br>output         | Y scaler output                                                          |                                             | ICODE[93H[7]]<br>ISWP[1:0] 85H[7:6]<br>I8_16[93H[6]]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI |
| H12 (45)                                                                            | ICLK            |                         |                                                                         |                                   | clock<br>output             |                                                                          | clock input                                 | ICKS[1:0] 80H[1:0]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI                                   |
| H14 (46)                                                                            | IDQ             |                         |                                                                         |                                   | data<br>qualifier<br>output |                                                                          | gated clock<br>output                       | ICKS[3:2] 80H[3:2]<br>IDQP[85H[0]]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI                   |
| J14 (42)                                                                            | ITRDY           |                         |                                                                         |                                   | target<br>ready input       |                                                                          |                                             |                                                                                         |
| G12 (53)                                                                            | IGPH            |                         |                                                                         |                                   | H gate<br>output            |                                                                          | extended<br>H gate,<br>horizontal<br>pulses | IDH[1:0] 84H[1:0]<br>IRHP[85H[1]]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI                    |
| F13 (52)                                                                            | IGPV            |                         |                                                                         |                                   | V gate<br>output            |                                                                          | V-sync, vertical<br>pulses                  | IDV[1:0] 84H[3:2]<br>IRVP[85H[2]]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI                    |

**PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler**

**SAA7114**

| <b>PIN<sup>(1)</sup></b> | <b>SYMBOL</b> | <b>8-BIT<br/>INPUT<br/>MODES</b> | <b>16-BIT INPUT<br/>MODES (ONLY<br/>FOR I<sup>2</sup>C-BUS<br/>PROGRAMMING)</b> | <b>ALTERNATIVE<br/>INPUT<br/>FUNCTIONS</b> | <b>8-BIT<br/>OUTPUT<br/>MODES</b> | <b>16-BIT OUTPUT<br/>MODES (ONLY<br/>FOR I<sup>2</sup>C-BUS<br/>PROGRAMMING)</b> | <b>ALTERNATIVE<br/>OUTPUT<br/>FUNCTIONS</b> | <b>I/O<br/>CONFIGURATION<br/>PROGRAMMING<br/>BITS</b>                 |
|--------------------------|---------------|----------------------------------|---------------------------------------------------------------------------------|--------------------------------------------|-----------------------------------|----------------------------------------------------------------------------------|---------------------------------------------|-----------------------------------------------------------------------|
| G13 (49)                 | IGP1          |                                  |                                                                                 |                                            | general<br>purpose                |                                                                                  |                                             | IDG1[1:0] 84H[5:4]<br>IG1P[85H[3]]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI |
| F14 (48)                 | IGP0          |                                  |                                                                                 |                                            | general<br>purpose                |                                                                                  |                                             | IDG0[1:0] 84H[7:6]<br>IG0P[85H[4]]<br>IPE[1:0] 87H[1:0]<br>+ pin ITRI |
| G14 (47)                 | ITRI          |                                  |                                                                                 |                                            | output<br>enable<br>input         |                                                                                  |                                             |                                                                       |

**Note**

1. Pin numbers for LQFP100 in parenthesis.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

**SAA7114**

## 8 FUNCTIONAL DESCRIPTION

### 8.1 Decoder

#### 8.1.1 ANALOG INPUT PROCESSING

The SAA7114 offers six analog signal inputs, two analog main channels with source switch, clamp circuit, analog amplifier, anti-alias filter and video 9-bit CMOS ADC; see Fig.7.

#### 8.1.2 ANALOG CONTROL CIRCUITS

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. The characteristic is shown in Fig.4. During the vertical blanking period gain and clamping control are frozen.

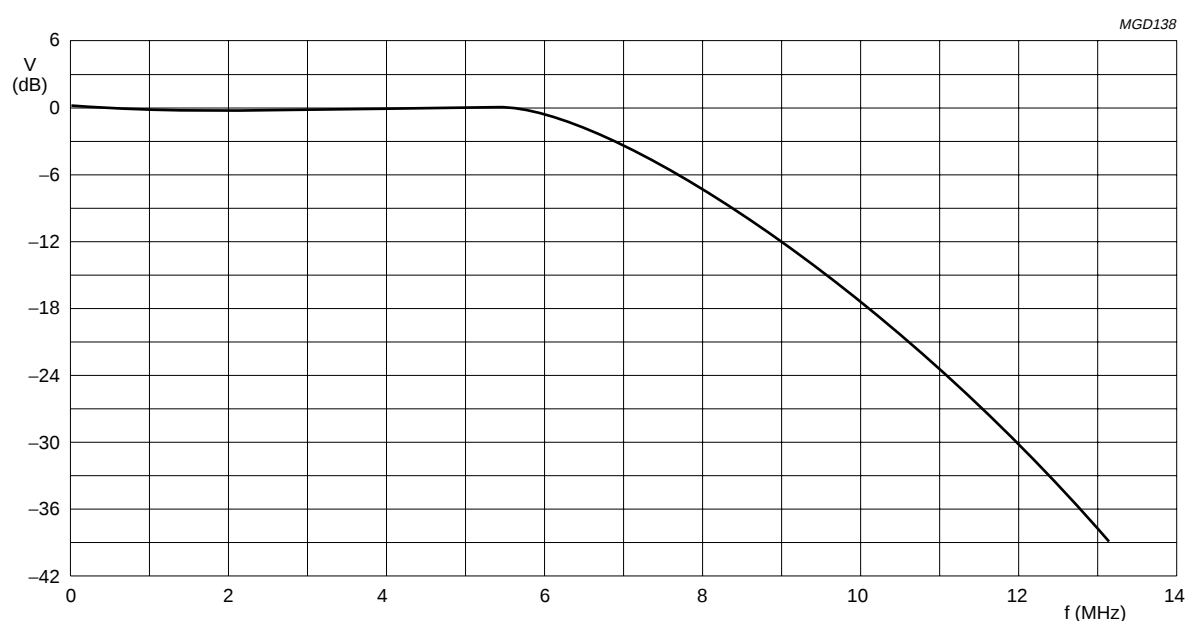


Fig.4 Anti-alias filter.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

8.1.2.1 Clamping

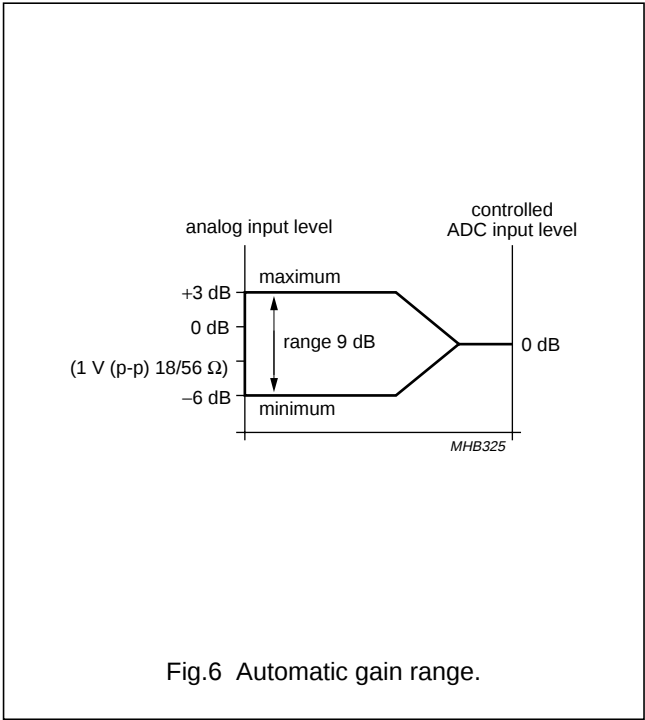
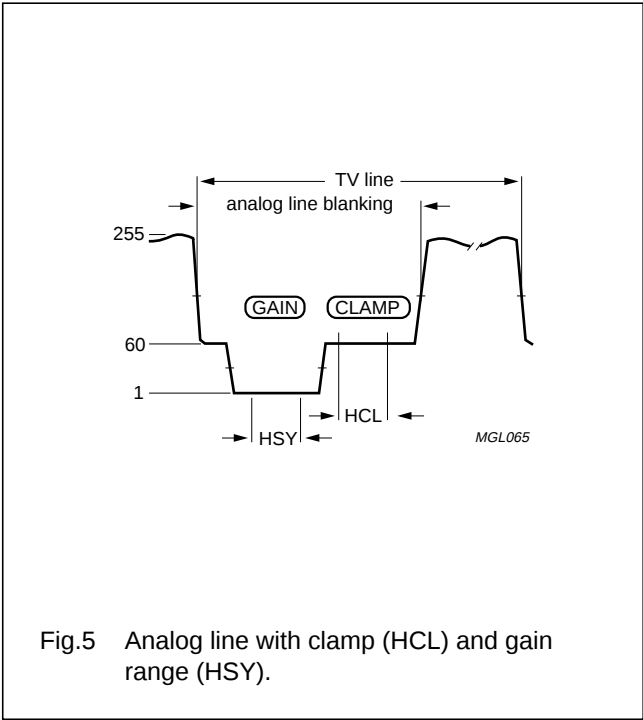
The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse on the back porch of the video signal.

8.1.2.2 Gain control

The gain control circuit receives (via the I<sup>2</sup>C-bus) the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built-in Automatic Gain Control (AGC) as part of the Analog Input Control (AICO).

The AGC (automatic gain control for luminance) is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal.

Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figs 8 and 9) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.



# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

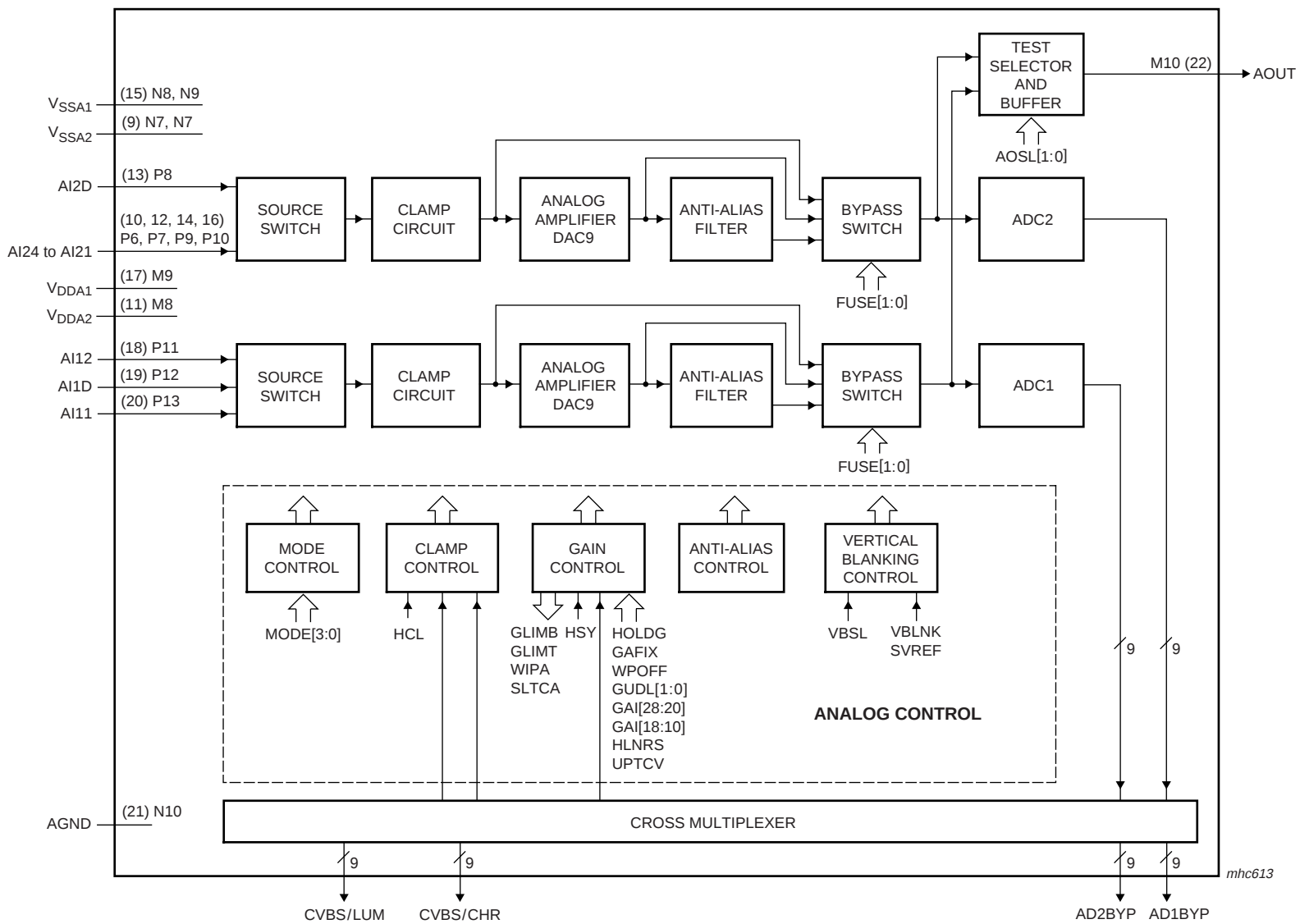
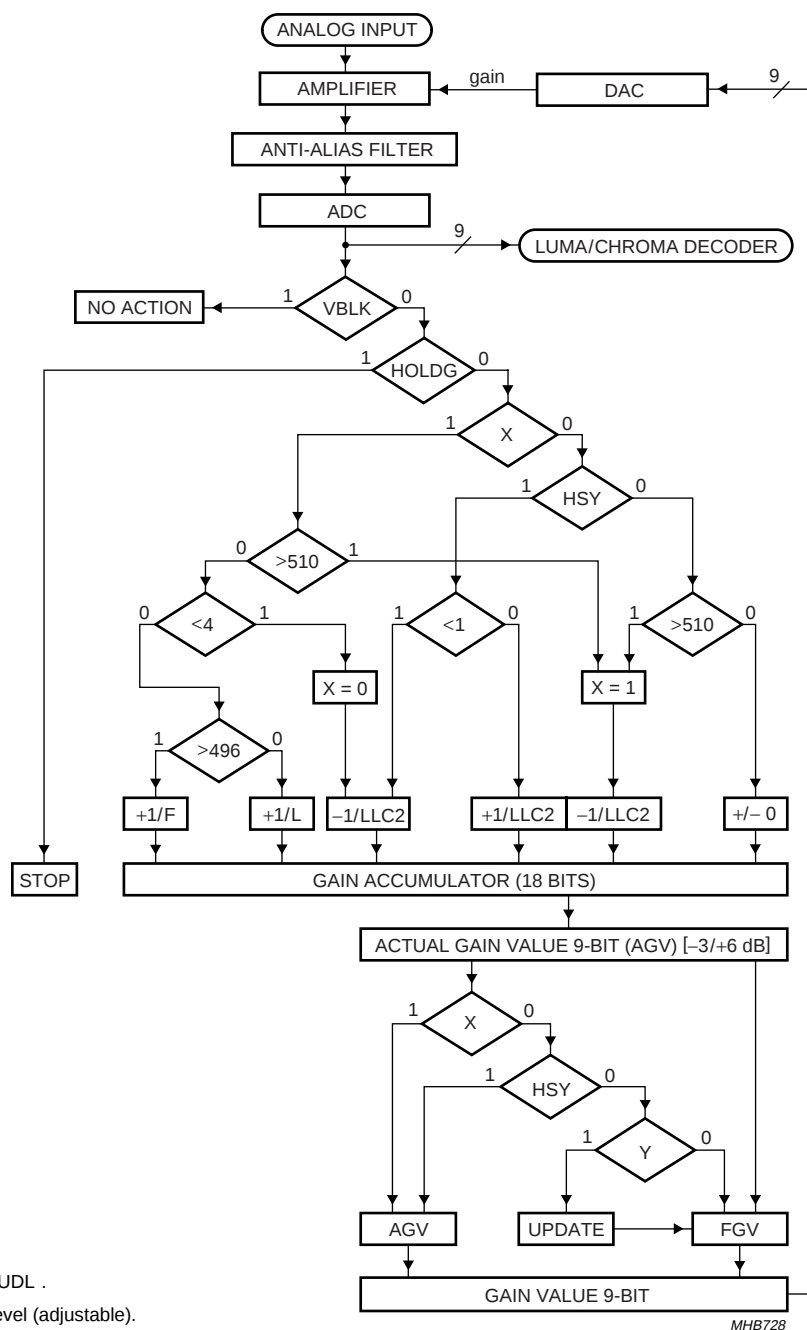


Fig.7 Analog input processing using the SAA7114 as differential front-end with 9-bit ADC.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

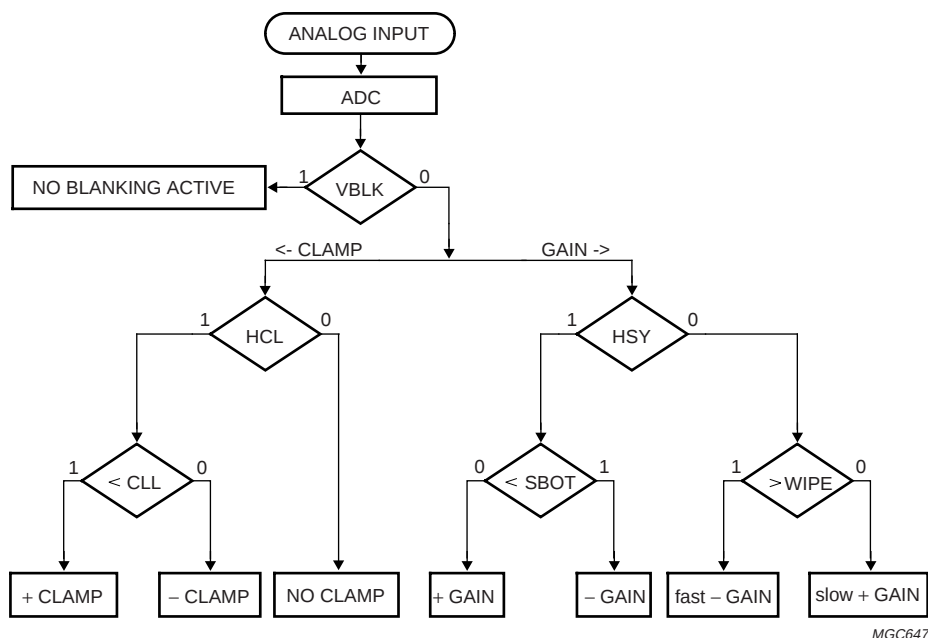


MHB728

Fig.8 Gain flow chart.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



WIPE = white peak level (254).  
 SBOT = sync bottom level (1).  
 CLL = clamp level [60 Y (128 C)].  
 HSY = horizontal sync pulse.  
 HCL = horizontal clamp pulse.

Fig.9 Clamp and gain flow chart.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.1.3 CHROMINANCE AND LUMINANCE PROCESSING

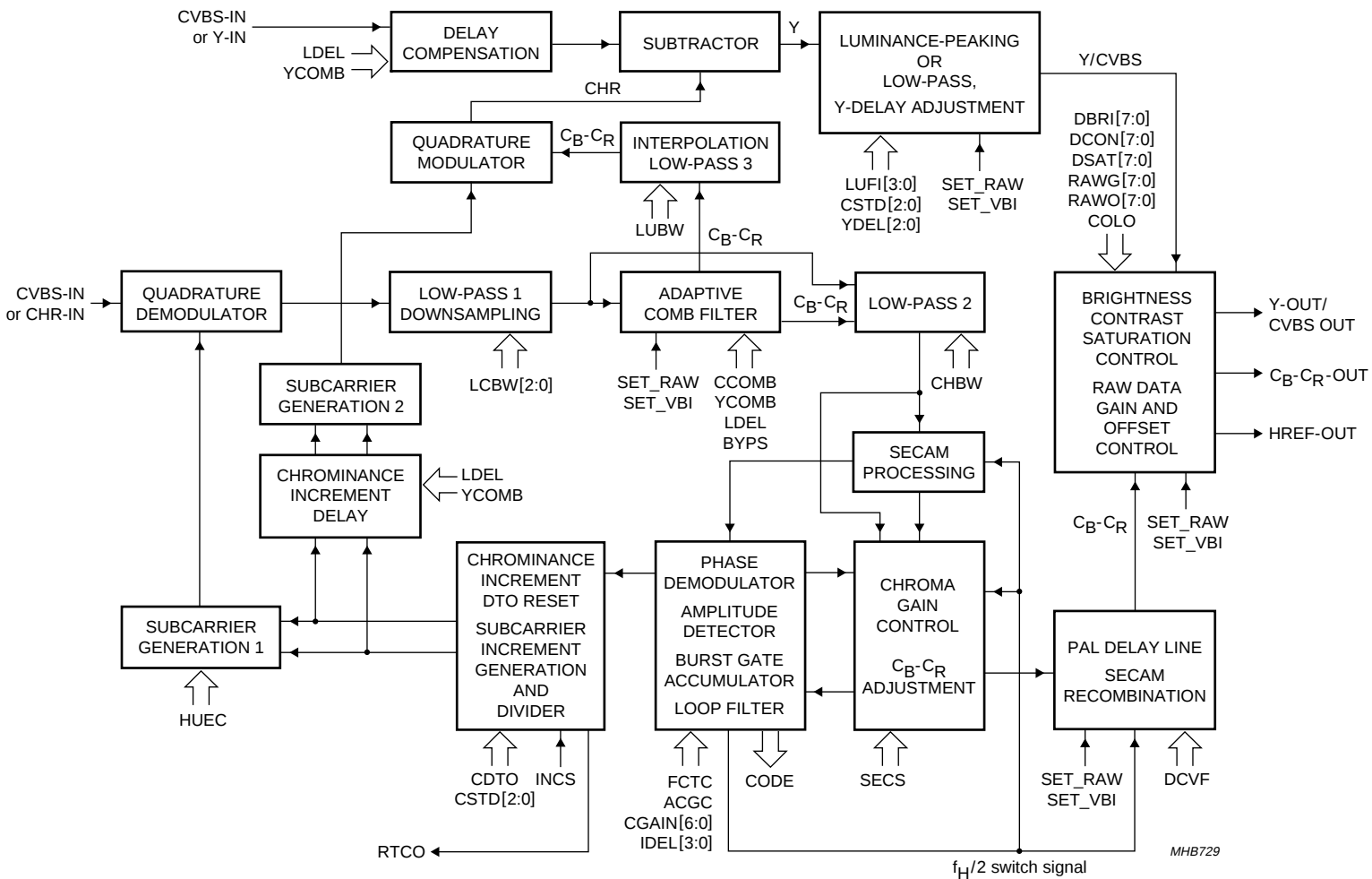


Fig.10 Chrominance and luminance processing.

## PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

### 8.1.3.1 Chrominance path

The 9-bit CVBS or chrominance input signal is fed to the input of a quadrature demodulator, where it is multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 1 ( $0^\circ$  and  $90^\circ$  phase relationship to the demodulator axis). The frequency is dependent on the chosen colour standard.

The time-multiplexed output signals of the multipliers are low-pass filtered (low-pass 1). Eight characteristics are programmable via LCWB3 to LCWB0 to achieve the desired bandwidth for the colour difference signals (PAL, NTSC) or the  $0^\circ$  and  $90^\circ$  FM signals (SECAM).

The chrominance low-pass 1 characteristic also influences the grade of cross-luminance reduction during horizontal colour transients (large chrominance bandwidth means strong suppression of cross-luminance). If the Y-comb filter is disabled by YCOMB = 0 the filter influences directly the width of the chrominance notch within the luminance path (a large chrominance bandwidth means wide chrominance notch resulting in a lower luminance bandwidth).

The low-pass filtered signals are fed to the adaptive comb filter block. The chrominance components are separated from the luminance via a two-line vertical stage (four lines for PAL standards) and a decision logic between the filtered and the non-filtered output signals. This block is bypassed for SECAM signals. The comb filter logic can be enabled independently for the succeeding luminance and chrominance processing by YCOMB (subaddress 09H, bit D6) and/or CCOMB (subaddress 0EH, bit D0). It is always bypassed during VBI or raw data lines programmable by the LCRn registers (subaddresses 41H to 57H); see Section 8.2.

The separated  $C_B$ - $C_R$  components are further processed by a second filter stage (low-pass 2) to modify the chrominance bandwidth without influencing the luminance path. Its characteristic is controlled by CHBW (subaddress 10H, bit D3). For the complete transfer characteristic of low-passes 1 and 2 see Figs 11 and 12.

The SECAM processing (bypassed for QAM standards) contains the following blocks:

- Baseband 'bell' filters to reconstruct the amplitude and phase equalized  $0^\circ$  and  $90^\circ$  FM signals
- Phase demodulator and differentiator (FM-demodulation)
- De-emphasis filter to compensate the pre-emphasized input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM switch signal).

The succeeding chrominance gain control block amplifies or attenuates the  $C_B$ - $C_R$  signal according to the required ITU 601/656 levels. It is controlled by the output signal from the amplitude detection circuit within the burst processing block.

The burst processing block provides the feedback loop of the chrominance PLL and contains the following:

- Burst gate accumulator
- Colour identification and colour killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)
- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, H/2-switch generation.

The increment generation circuit produces the Discrete Time Oscillator (DTO) increment for both subcarrier generation blocks. It contains a division by the increment of the line-locked clock generator to create a stable phase-locked sine signal under all conditions (e.g. for non-standard signals).

The PAL delay line block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC colour standards the delay line can be used as an additional vertical filter. If desired, it can be switched off by DCVF = 1. It is always disabled during VBI or raw data lines programmable by the LCRn registers (subaddresses 41H to 57H); see Section 8.2. The embedded line delay is also used for SECAM recombination (cross-over switches).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

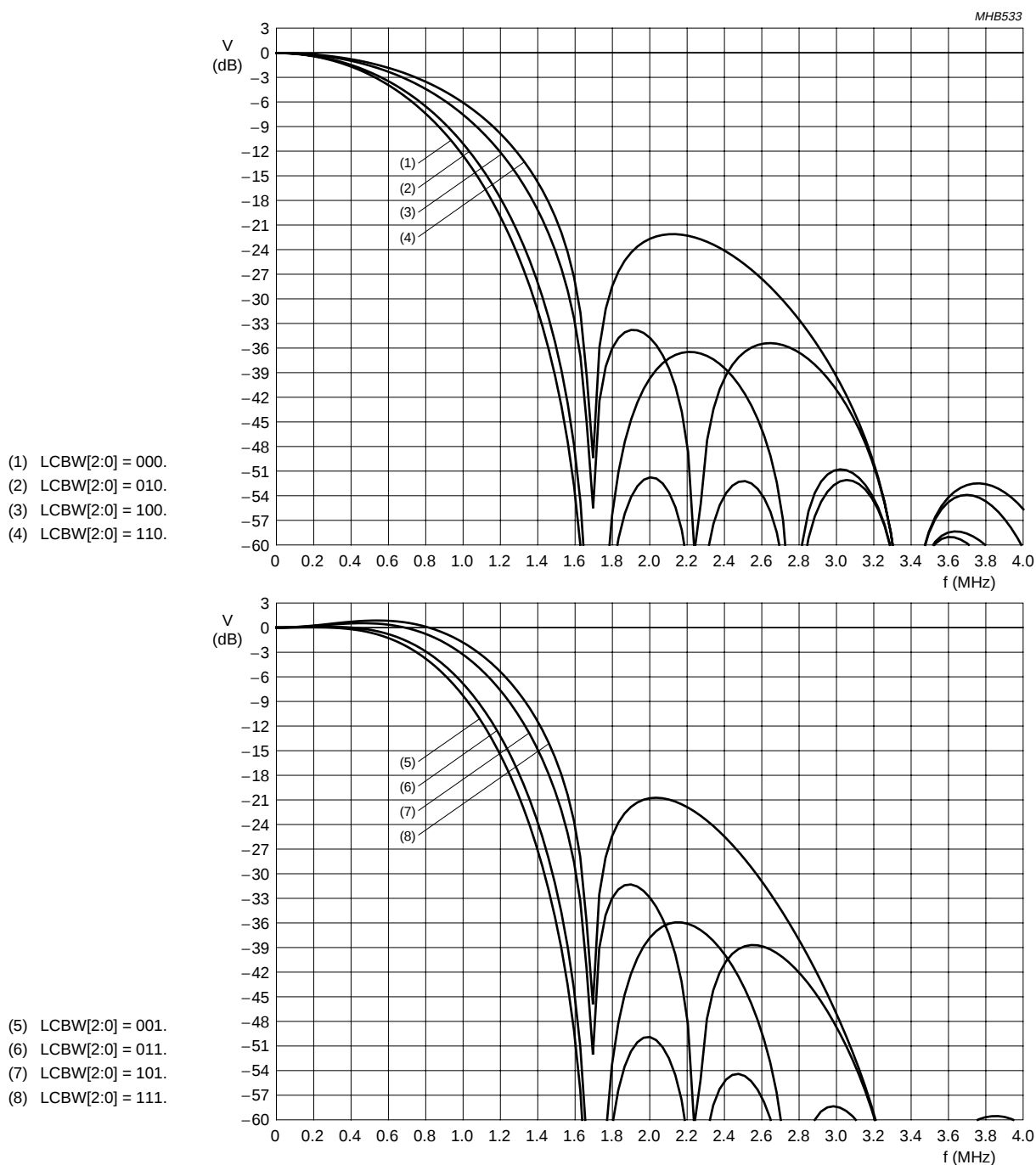


Fig.11 Transfer characteristics of the chrominance low-pass at CHBW = 0.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

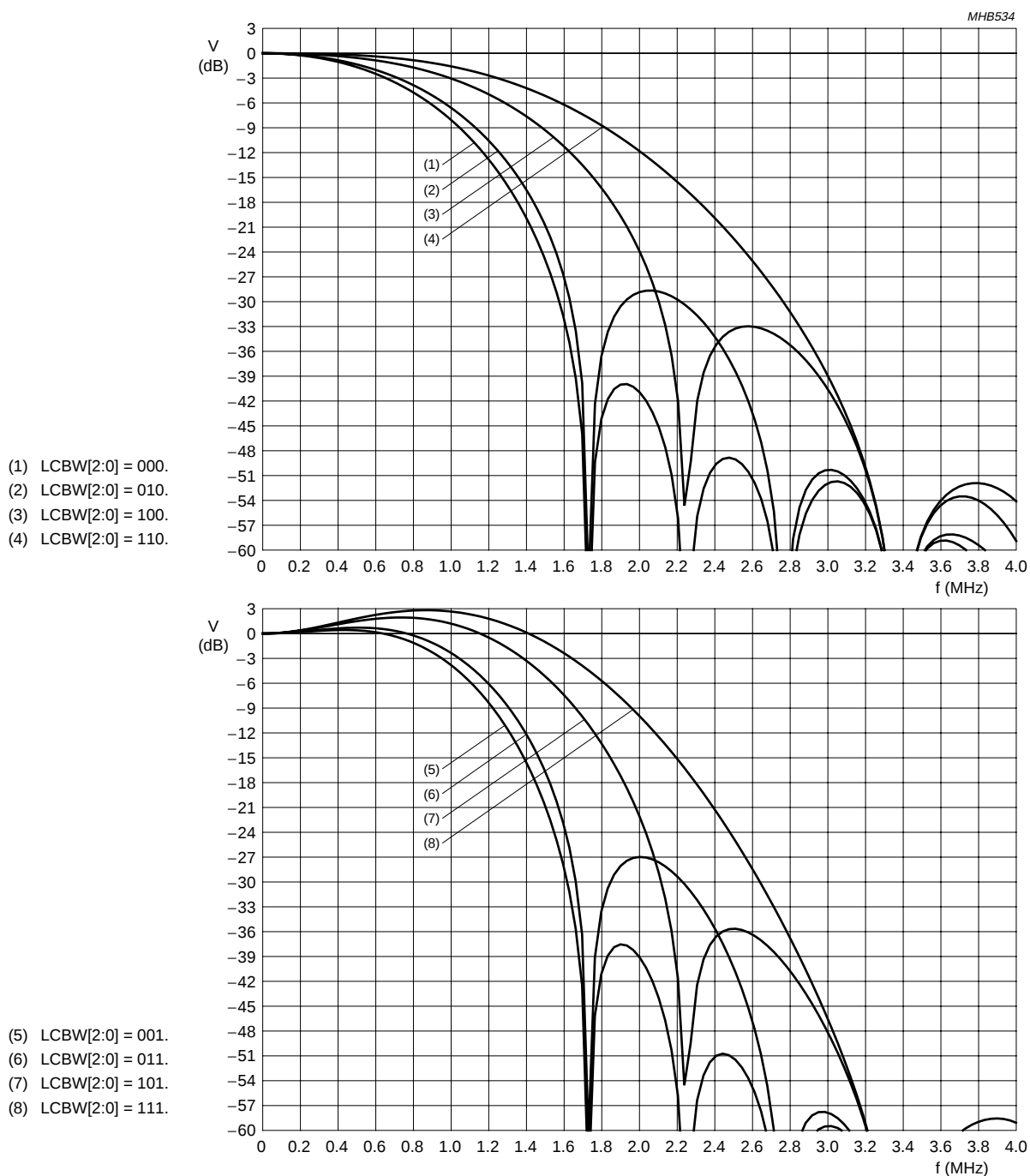


Fig.12 Transfer characteristics of the chrominance low-pass at CHBW = 1.

---

## PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

---

SAA7114

### 8.1.3.2 Luminance path

The rejection of the chrominance components within the 9-bit CVBS or Y input signal is achieved by subtracting the remodulated chrominance signal from the CVBS input.

The comb filtered  $C_B$ - $C_R$  components are interpolated (upsampled) by the low-pass 3 block. Its characteristic is controlled by LUBW (subaddress 09H, bit D4) to modify the width of the chrominance 'notch' without influencing the chrominance path. The programmable frequency characteristics available, in conjunction with the LCBW2 to LCBW0 settings, can be seen in Figs 13 to 16. It should be noted that these frequency curves are only valid for Y-comb disabled filter mode (YCOMB = 0). In comb filter mode the frequency response is flat. The centre frequency of the notch is automatically adapted to the chosen colour standard.

The interpolated  $C_B$ - $C_R$  samples are multiplied by two time-multiplexed subcarrier signals from the subcarrier generation block 2. This second DTO is locked to the first subcarrier generator by an increment delay circuit matched to the processing delay, which is different for PAL and NTSC standards according to the chosen comb filter algorithm. The two modulated signals are finally added to build the remodulated chrominance signal.

The frequency characteristic of the separated luminance signal can be further modified by the succeeding luminance filter block. It can be configured as peaking (resolution enhancement) or low-pass block by LUF13 to LUF10 (subaddress 09H, bits D3 to D0). The 16 resulting frequency characteristics can be seen in Fig.17. The LUF13 to LUF10 settings can be used as a user programmable sharpness control.

The luminance filter block also contains the adjustable Y-delay part; programmable by YDEL2 to YDEL0 (subaddress 11H, bits D2 to D0).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

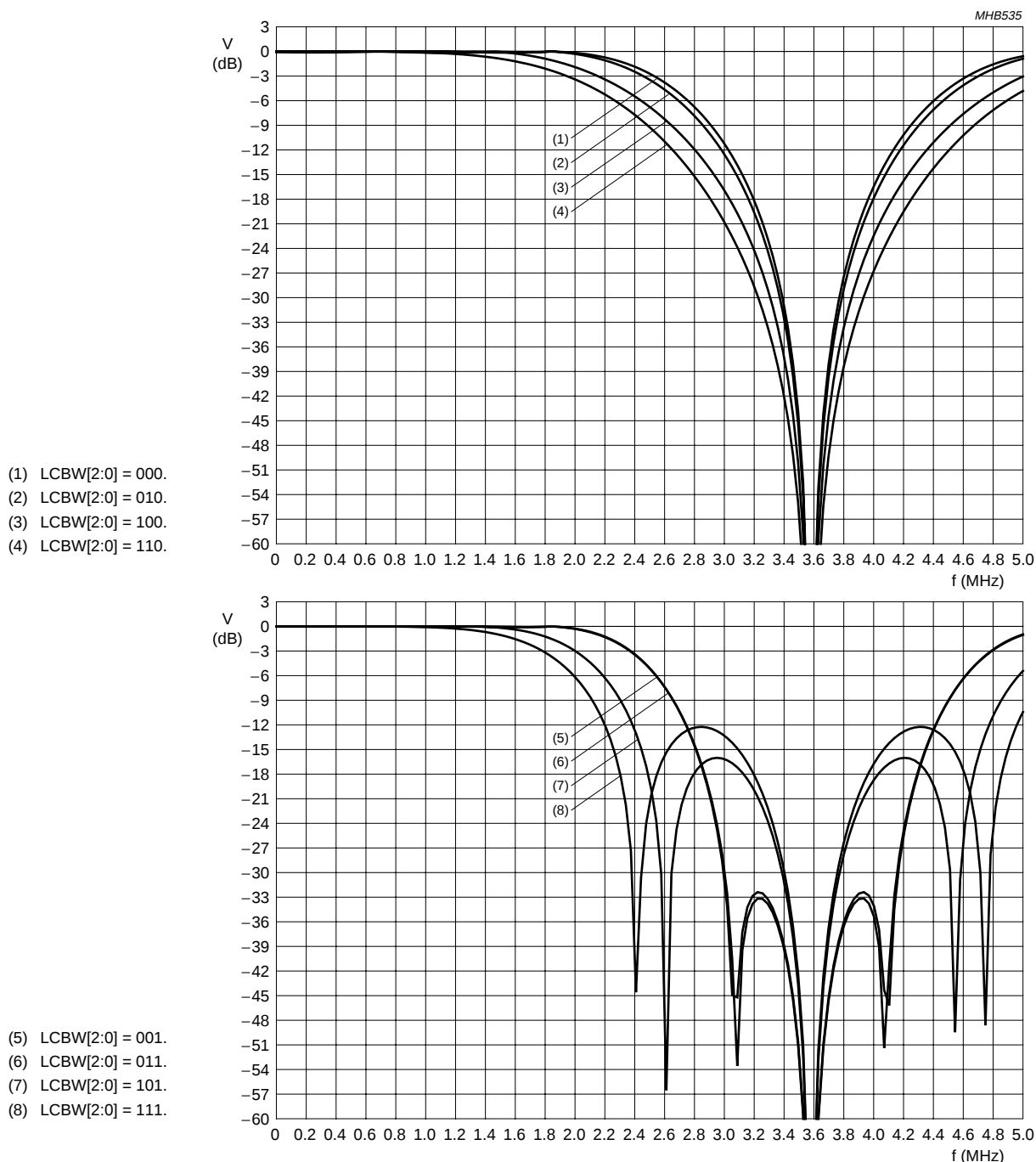


Fig.13 Transfer characteristics of the luminance notch filter in 3.58 MHz mode (Y-comb filter disabled) at LUBW = 0.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

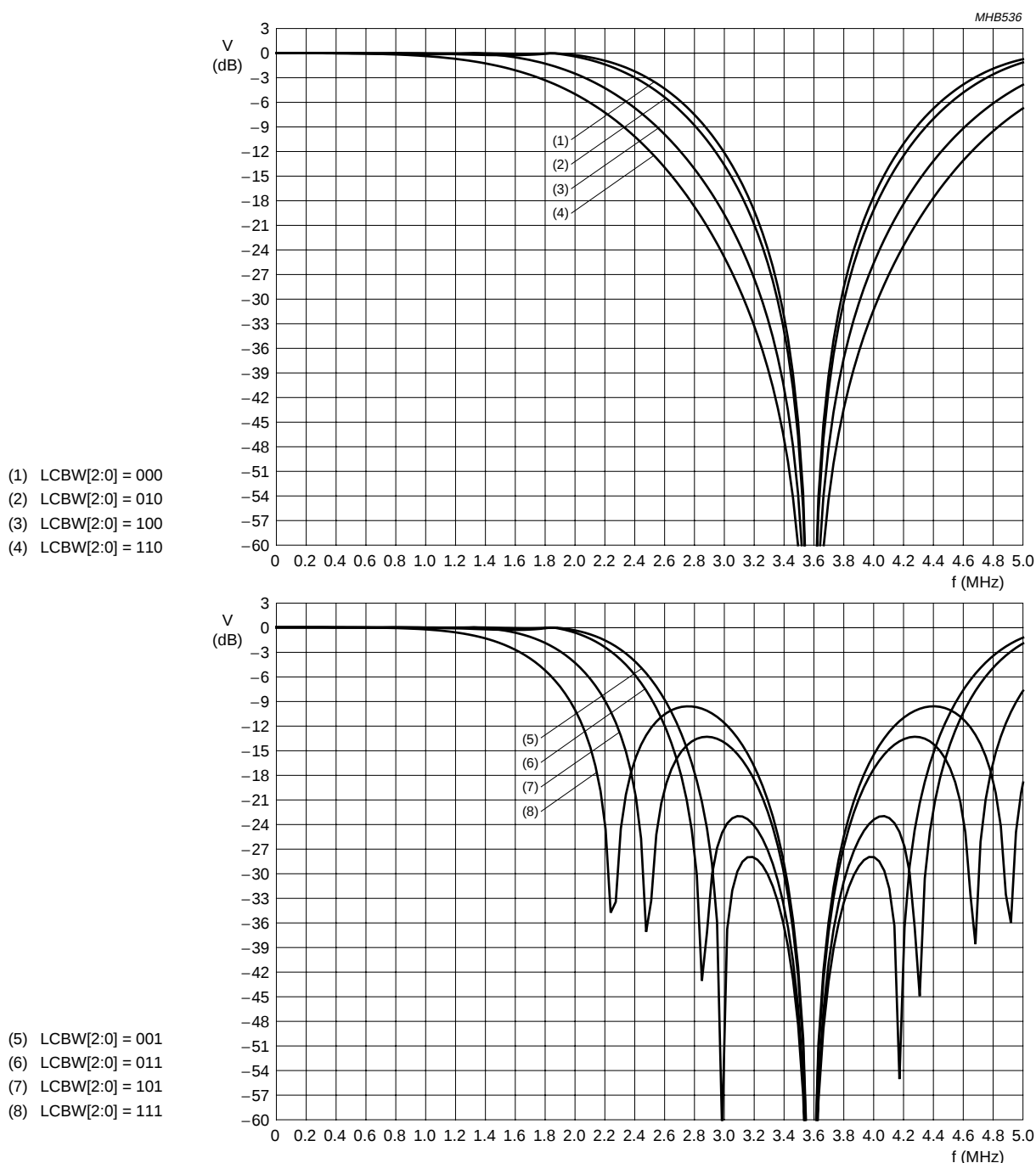


Fig.14 Transfer characteristics of the luminance notch filter in 3.58 MHz mode (Y-comb filter disabled) at LUBW = 1.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

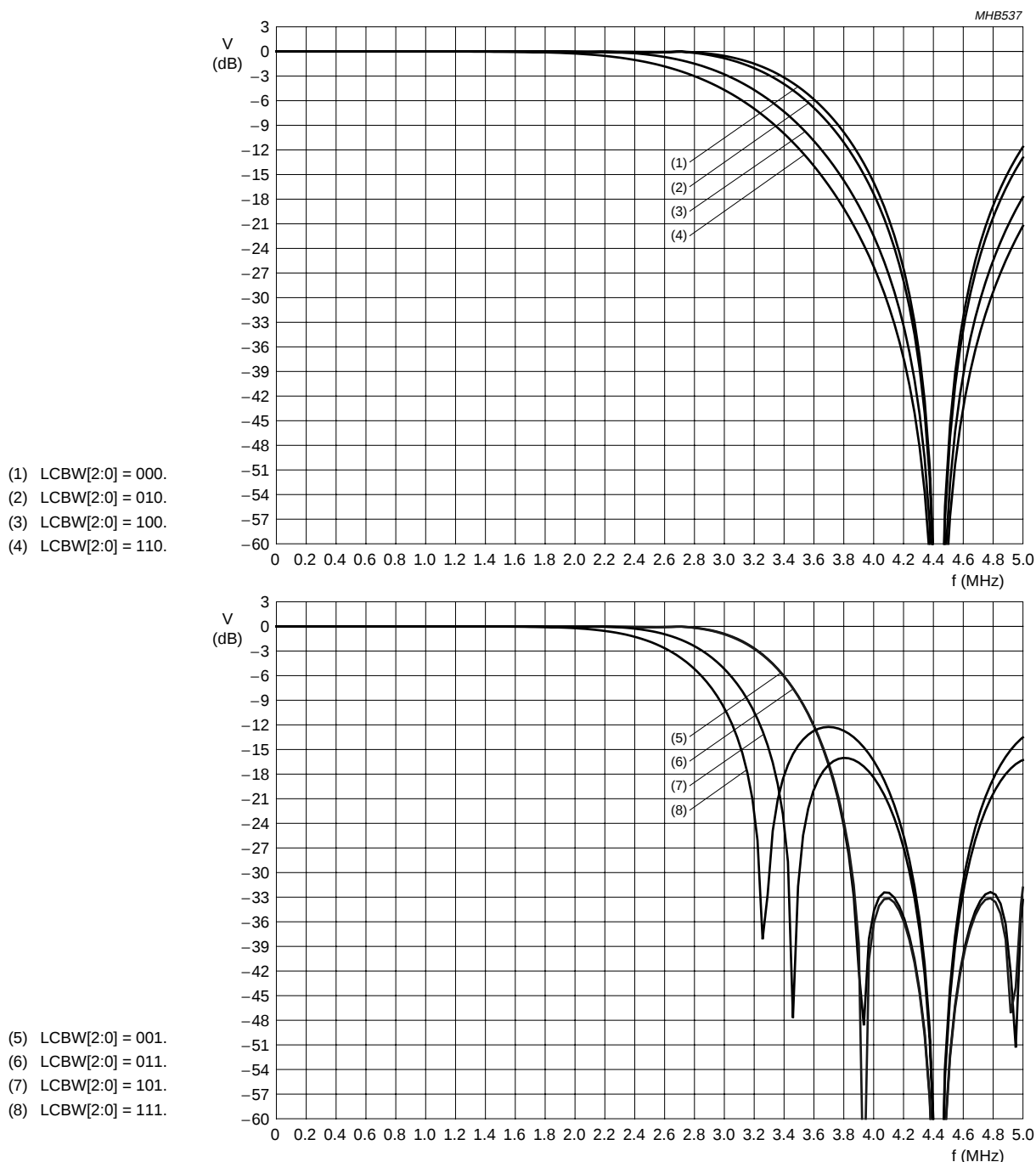


Fig.15 Transfer characteristics of the luminance notch filter in 4.43 MHz mode (Y-comb filter disabled) at LUBW = 0.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

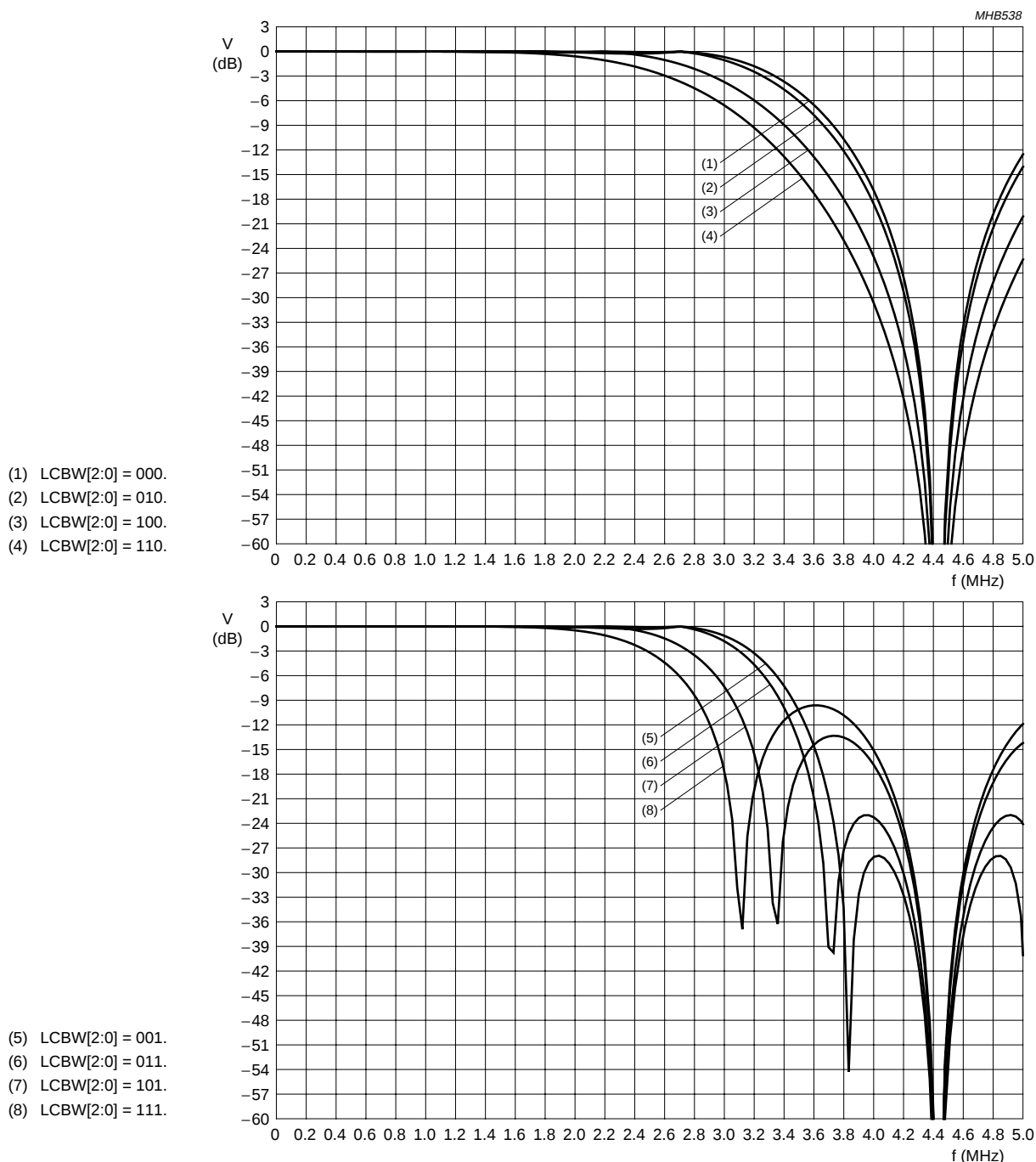


Fig.16 Transfer characteristics of the luminance notch filter in 4.43 MHz mode (Y-comb filter disabled) at LUBW = 1.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

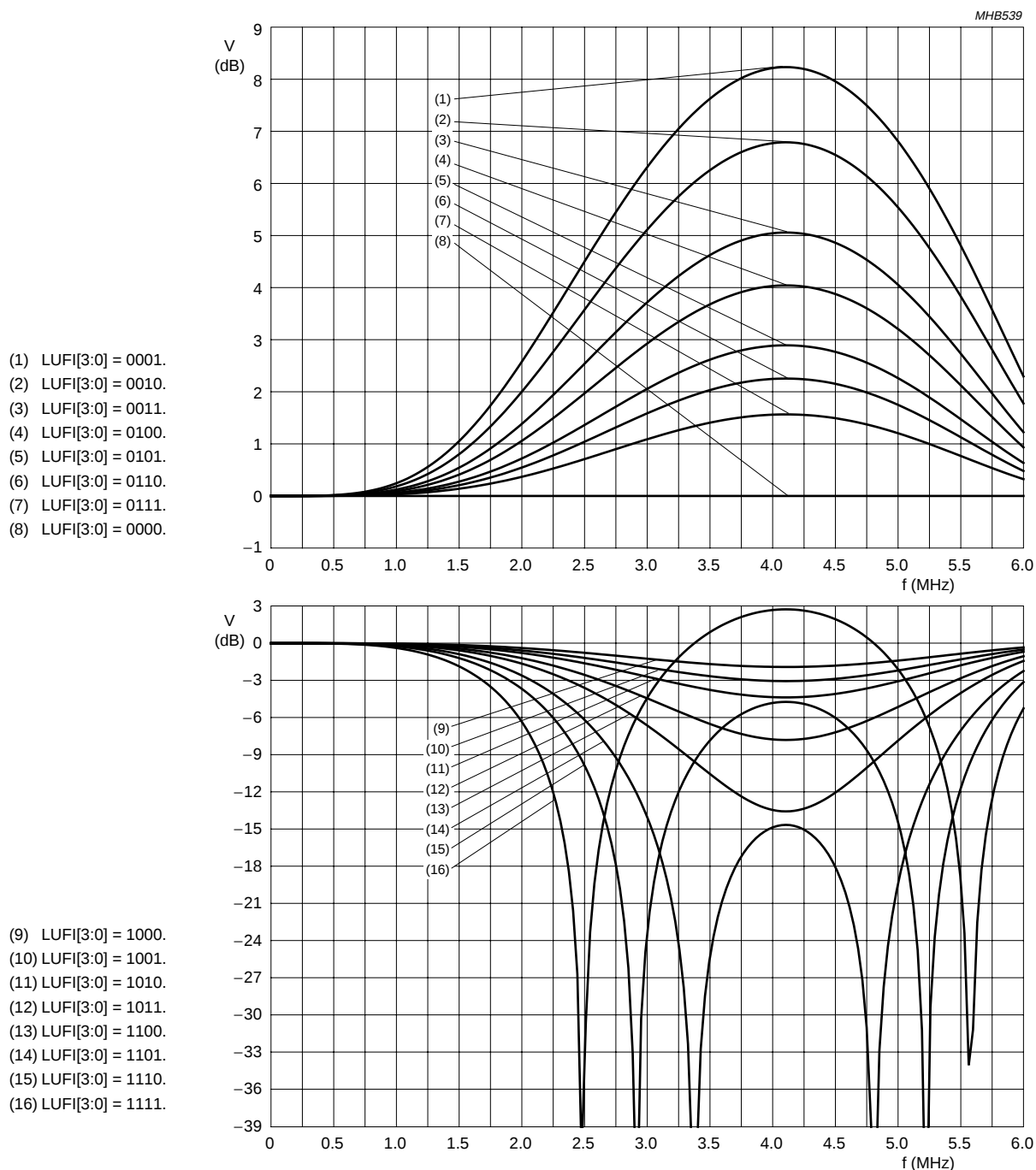


Fig.17 Transfer characteristics of the luminance peaking/low-pass filter (sharpness).

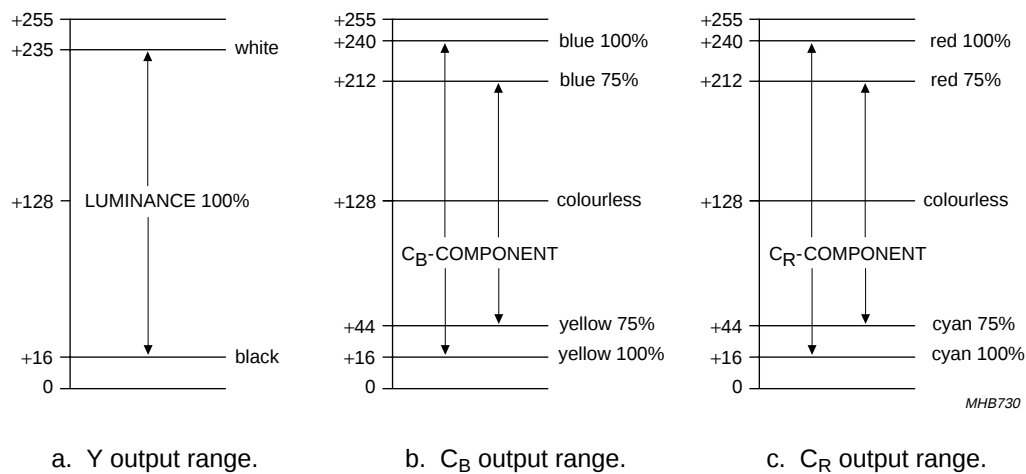
# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.1.3.3 Brightness Contrast Saturation (BCS) control and decoder output levels

The resulting Y (CVBS) and C<sub>B</sub>-C<sub>R</sub> signals are fed to the BCS block, which contains the following functions:

- Chrominance saturation control by DSAT7 to DSAT0
- Luminance contrast and brightness control by DCON7 to DCON0 and DBRI7 to DBRI0
- Raw data (CVBS) gain and offset adjustment by RAWG7 to RAWG0 and RAWO7 to RAWO0
- Limiting Y-C<sub>B</sub>-C<sub>R</sub> or CVBS to the values 1 (minimum) and 254 (maximum) to fulfil "ITU Recommendation 601/656".



"ITU Recommendation 601/656" digital levels with default BCS (decoder) settings DCON[7:0] = 44H, DBRI[7:0] = 80H and DSAT[7:0] = 40H. Equations for modification to the Y-C<sub>B</sub>-C<sub>R</sub> levels via BCS control I<sup>2</sup>C-bus bytes DBRI, DCON and DSAT.

$$\text{Luminance: } Y_{\text{OUT}} = \text{Int} \left[ \frac{\text{DCON}}{68} \times (Y - 128) \right] + \text{DBRI}$$

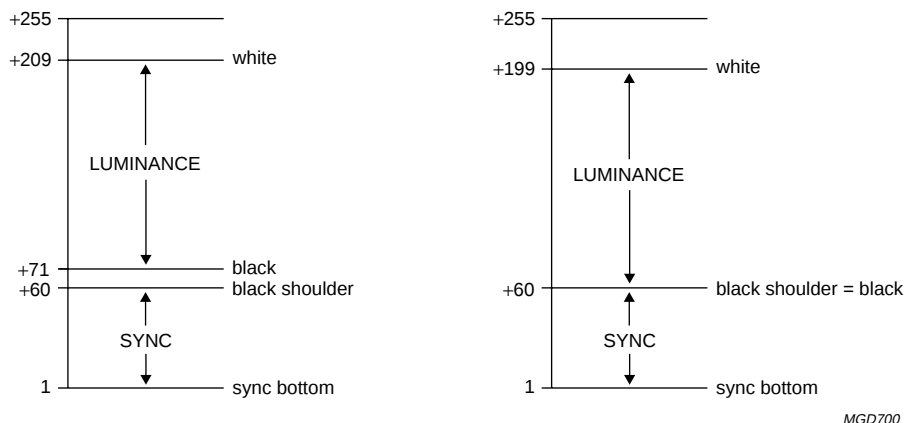
$$\text{Chrominance: } (C_R C_B)_{\text{OUT}} = \text{Int} \left[ \frac{\text{DSAT}}{64} \times (C_R, C_B - 128) \right] + 128$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with "ITU Recommendation 601/656".

Fig.18 Y-C<sub>B</sub>-C<sub>R</sub> range for scaler input and X port output.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



a. Sources containing 7.5 IRE black level offset (e.g. NTSC M).

b. Sources not containing black level offset.

CVBS levels with default settings RAWG[7:0] = 64 and RAWO[7:0] = 128.

Equation for modification of the raw data levels via bytes RAWG and RAWO:

$$CVBS_{OUT} = \text{Int} \left[ \frac{RAWG}{64} \times (CVBS_{nom} - 128) \right] + RAWO$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with "ITU Recommendation 601/656".

Fig.19 CVBS (raw data) range for scaler input, data slicer and X port output.

## 8.1.4 SYNCHRONIZATION

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is further reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e.g. HCL and HSY) are generated in accordance with analog front-end requirements. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO; see Fig.20.

The detection of 'pseudo syncs' as part of the Macrovision copy protection standard is also achieved within the synchronization circuit.

The result is reported as flag COPRO within the decoder status byte at subaddress 1FH.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

8.1.5   CLOCK GENERATION CIRCUIT

The internal CGC generates all clock signals required for the video input processor.

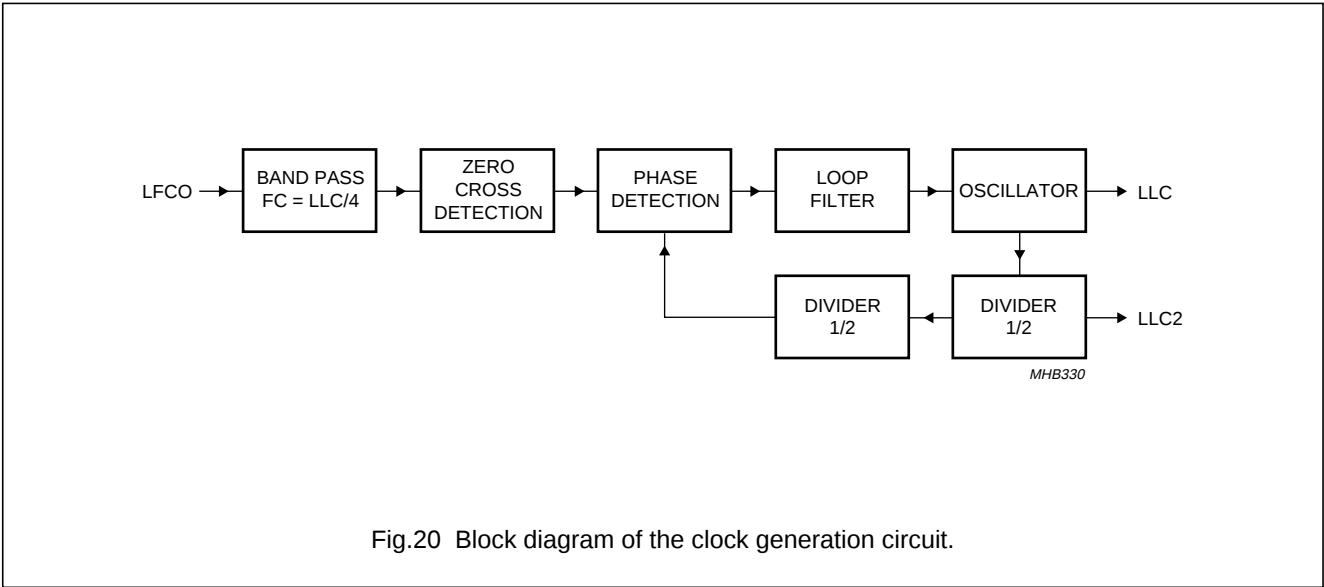
The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency:

$$6.75\text{ MHz} = 429 \times f_H\text{ (50 Hz), or}$$
$$6.75\text{ MHz} = 432 \times f_H\text{ (60 Hz).}$$

The LFCO signal is multiplied by a factor of 2 and 4 in the internal PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the output clock signals. The rectangular output clocks have a 50% duty factor.

Table 3   Decoder clock frequencies

| CLOCK           | FREQUENCY (MHz)  |
|-----------------|------------------|
| XTALO           | 24.576 or 32.110 |
| LLC             | 27               |
| LLC2            | 13.5             |
| LLC4 (internal) | 6.75             |
| LLC8 (virtual)  | 3.375            |



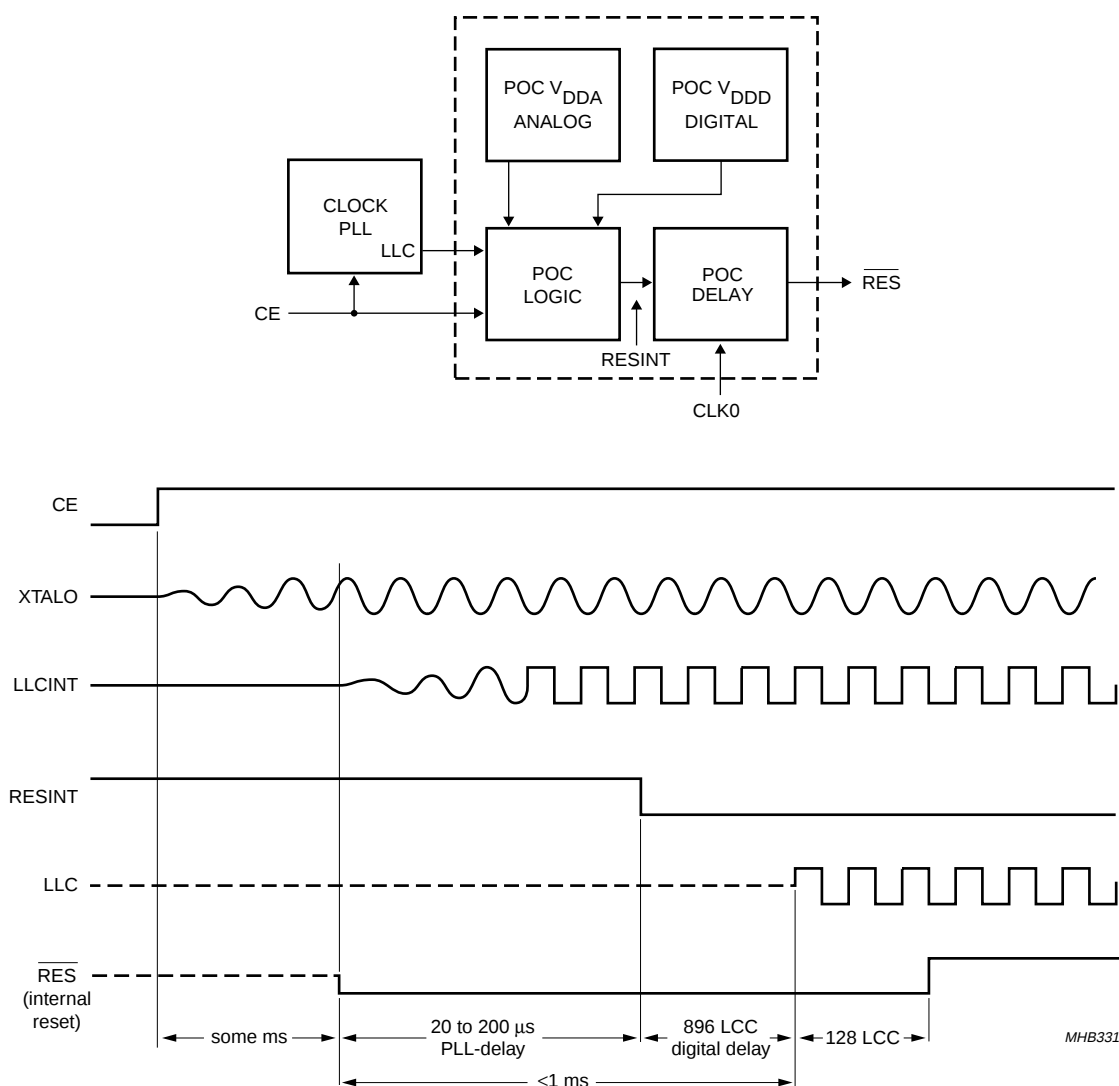
8.1.6   POWER-ON RESET AND CHIP ENABLE (CE) INPUT

A missing clock, insufficient digital or analog  $V_{DDA0}$  supply voltages (below 2.7 V) will start the reset sequence; all outputs are forced to 3-state (see Fig.21). The indicator output  $\overline{\text{RES}}$  is LOW for approximately 128 LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

It is possible to force a reset by pulling the Chip Enable pin (CE) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2 and SDA return from 3-state to active, while the other signals have to be activated via programming.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



POC = Power-on control.  
CE = chip enable input.  
XTALO = crystal oscillator output.  
LLCINT = internal system clock.  
RESINT = internal reset.  
LLC = line-locked clock output.  
RES = reset output.

Fig.21 Power-on control circuit.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.2 Decoder output formatter

The output interface block of the decoder part contains the ITU 656 formatter for the expansion port data output XPD7 to XPD0 (for a detailed description see Section 9.4.1) and the control circuit for the signals needed for the internal paths to the scaler and data slicer part. It also controls the selection of the reference signals for the RT port (RTCO, RTS0 and RTS1) and the expansion port (XRH, XRV and XDQ).

The generation of the decoder data type control signals SET\_RAW and SET\_VBI is also done within this block. These signals are decoded from the requested data type for the scaler input and/or the data slicer, selectable by the control registers LCR2 to LCR24 (see also Chapter 15; subaddresses 41H to 57H).

For each LCR value from 2 to 23 the data type can be programmed individually; LCR2 to LCR23 refer to line numbers. The selection in LCR24 values is valid for the rest of the corresponding field. The upper nibble contains the value for field 1 (odd), the lower nibble for field 2 (even). The relationship between LCR values and line numbers can be adjusted via VOFF8 to VOFF0, located in subaddresses 5BH (bit D4) and 5AH (bits D7 to D0) and F0FF subaddress 5BH (bit D7). The recommended values are VOFF[8:0] = 03H for 50 Hz sources (with F0FF = 0) and VOFF[8:0] = 06H for 60 Hz sources (with F0FF = 1), to accommodate line number conventions as used for PAL, SECAM and NTSC standards; see Tables 5 to 8.

**Table 4** Data formats at decoder output

| DATA TYPE NUMBER | DATA TYPE                                   | DECODER OUTPUT DATA FORMAT                 |
|------------------|---------------------------------------------|--------------------------------------------|
| 0                | teletext EuroWST, CCST                      | raw                                        |
| 1                | European closed caption                     | raw                                        |
| 2                | Video Programming Service (VPS)             | raw                                        |
| 3                | wide screen signalling bits                 | raw                                        |
| 4                | US teletext (WST)                           | raw                                        |
| 5                | US closed caption (line 21)                 | raw                                        |
| 6                | video component signal, VBI region          | Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 |
| 7                | CVBS data                                   | raw                                        |
| 8                | teletext                                    | raw                                        |
| 9                | VITC/EBU time codes (Europe)                | raw                                        |
| 10               | VITC/SMPTE time codes (USA)                 | raw                                        |
| 11               | reserved                                    | raw                                        |
| 12               | US NABTS                                    | raw                                        |
| 13               | MOJI (Japanese)                             | raw                                        |
| 14               | Japanese format switch (L20/22)             | raw                                        |
| 15               | video component signal, active video region | Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 |

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 5** Relationship of LCR to line numbers in 525 lines/60 Hz systems (part 1)

Vertical line offset, VOFF[8:0] = 06H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 1 (subaddress 5BH[7])

|                                    |              |     |     |     |     |                     |     |     |                  |     |     |                     |     |     |
|------------------------------------|--------------|-----|-----|-----|-----|---------------------|-----|-----|------------------|-----|-----|---------------------|-----|-----|
| <b>Line number<br/>(1st field)</b> | 521          | 522 | 523 | 524 | 525 | 1                   | 2   | 3   | 4                | 5   | 6   | 7                   | 8   | 9   |
|                                    | active video |     |     |     |     | equalization pulses |     |     | serration pulses |     |     | equalization pulses |     |     |
| <b>Line number<br/>(2nd field)</b> | 259          | 260 | 261 | 262 | 263 | 264                 | 265 | 266 | 267              | 268 | 269 | 270                 | 271 | 272 |
|                                    | active video |     |     |     |     | equalization pulses |     |     | serration pulses |     |     | equalization pulses |     |     |
| <b>LCR</b>                         | 24           |     |     |     |     | 2                   |     | 3   | 4                | 5   | 6   | 7                   | 8   | 9   |

**Table 6** Relationship of LCR to line numbers in 525 lines/60 Hz systems (part 2)

Vertical line offset, VOFF[8:0] = 06H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 1 (subaddress 5BH[7])

|                            |                      |     |     |     |     |     |     |     |     |     |     |     |              |     |     |     |
|----------------------------|----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|--------------|-----|-----|-----|
| Line number<br>(1st field) | 10                   | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22           | 23  | 24  | 25  |
|                            | nominal VBI lines F1 |     |     |     |     |     |     |     |     |     |     |     | active video |     |     |     |
| Line number<br>(2nd field) | 273                  | 274 | 275 | 276 | 277 | 278 | 279 | 280 | 281 | 282 | 283 | 284 | 285          | 286 | 287 | 288 |
|                            | nominal VBI lines F2 |     |     |     |     |     |     |     |     |     |     |     | active video |     |     |     |
| LCR                        | 10                   | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22           | 23  | 24  |     |

**Table 7** Relationship of LCR to line numbers in 625 lines/50 Hz systems (part 1)

Vertical line offset, VOFF[8:0] = 03H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 0 (subaddress 5BH[7])

|                            |              |     |                     |                     |     |                  |     |                     |                     |     |
|----------------------------|--------------|-----|---------------------|---------------------|-----|------------------|-----|---------------------|---------------------|-----|
| Line number<br>(1st field) | 621          | 622 | 623                 | 624                 | 625 | 1                | 2   | 3                   | 4                   | 5   |
|                            | active video |     |                     | equalization pulses |     | serration pulses |     |                     | equalization pulses |     |
| Line number<br>(2nd field) | 309          | 310 | 311                 | 312                 | 313 | 314              | 315 | 316                 | 317                 | 318 |
|                            | active video |     | equalization pulses |                     |     | serration pulses |     | equalization pulses |                     |     |
| LCR                        | 24           |     |                     |                     |     |                  | 2   | 3                   | 4                   | 5   |

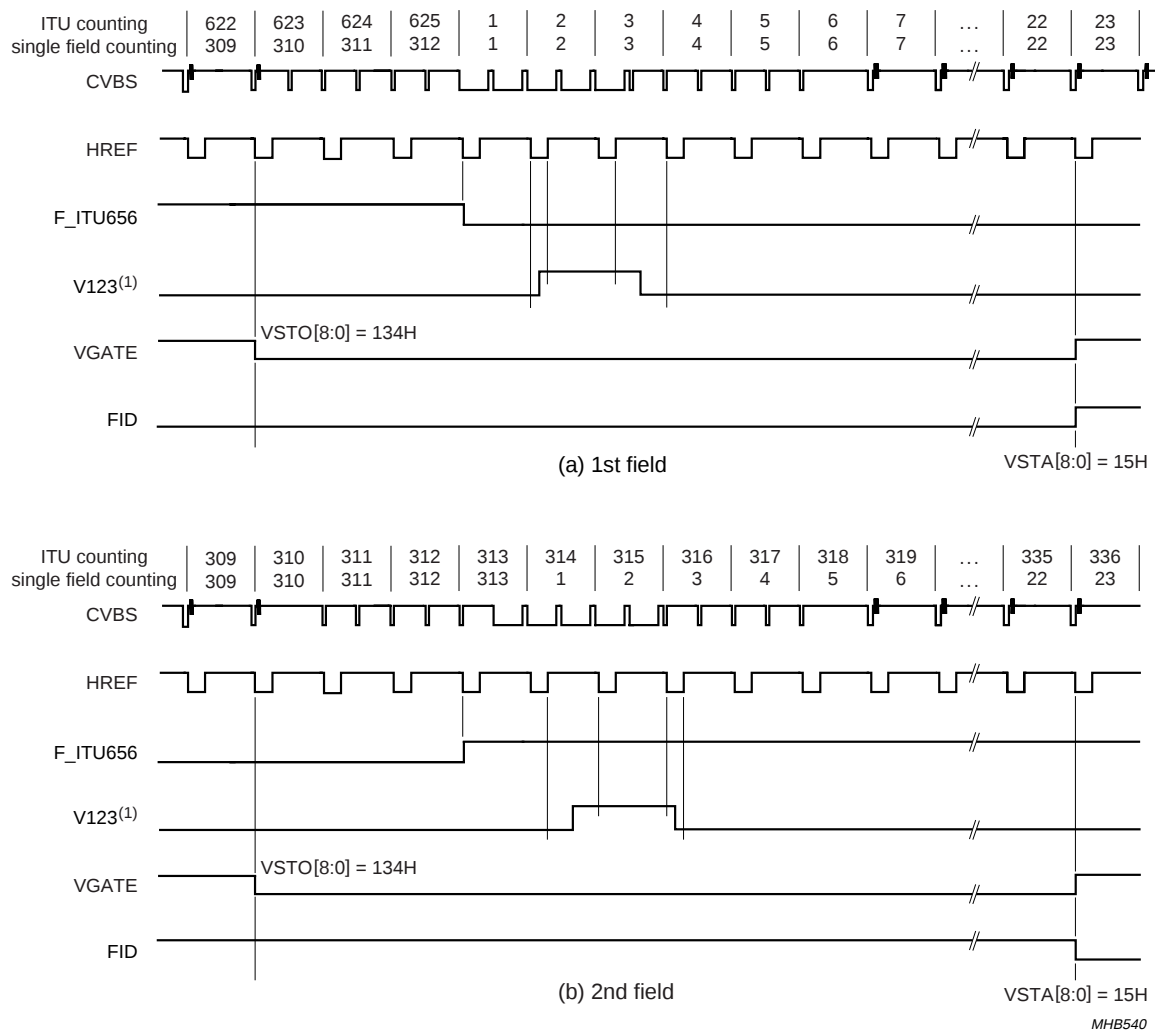
**Table 8** Relationship of LCR to line numbers in 625 lines/50 Hz systems (part 2)

Vertical line offset, VOFF[8:0] = 03H (subaddresses 5BH[4] and 5AH[7:0]); horizontal pixel offset, HOFF[10:0] = 347H (subaddresses 5BH[2:0] and 59H[7:0]); FOFF = 0 (subaddress 5BH[7])

|                                    |                      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |              |     |
|------------------------------------|----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|--------------|-----|
| <b>Line number<br/>(1st field)</b> | 6                    | 7   | 8   | 9   | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24           | 25  |
|                                    | nominal VBI lines F1 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | active video |     |
| <b>Line number<br/>(2nd field)</b> | 319                  | 320 | 321 | 322 | 323 | 324 | 325 | 326 | 327 | 328 | 329 | 330 | 331 | 332 | 333 | 334 | 335 | 336 | 337          | 338 |
|                                    | nominal VBI lines F2 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | active video |     |
| <b>LCR</b>                         | 6                    | 7   | 8   | 9   | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24           |     |

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114



(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.

The control signals listed above are available on pins RTS0, RTS1, XRH and XRV according to the following table:

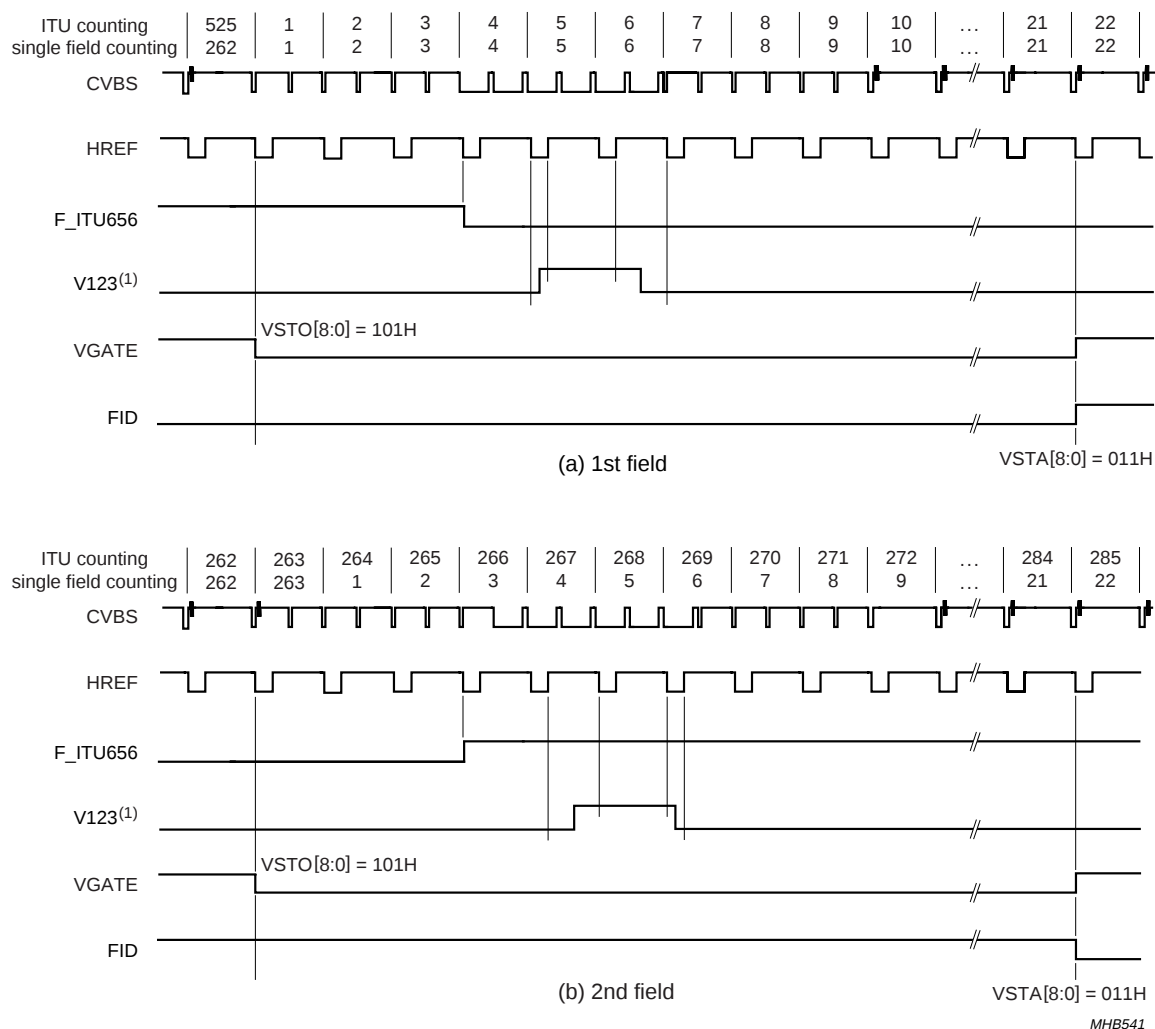
| NAME     | RTS0 | RTS1 | XRH | XRV |
|----------|------|------|-----|-----|
| HREF     | X    | X    | X   | —   |
| F_ITU656 | —    | —    | —   | X   |
| V123     | X    | X    | —   | X   |
| VGATE    | X    | X    | —   | —   |
| FID      | X    | X    | —   | —   |

For further information see Section 15.2: Tables 57, 58 and 59.

Fig.22 Vertical timing diagram for 50 Hz/625 line systems.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114



(1) The inactive going edge of the V123 signal indicates whether the field is odd or even. If HREF is active during the falling edge of V123, the field is ODD (field 1). If HREF is inactive during the falling edge of V123, the field is EVEN. The specific position of the slope is dependent on the internal processing delay and may change a few clock cycles from version to version.

The control signals listed above are available on pins RTS0, RTS1, XRH and XRV according to the following table:

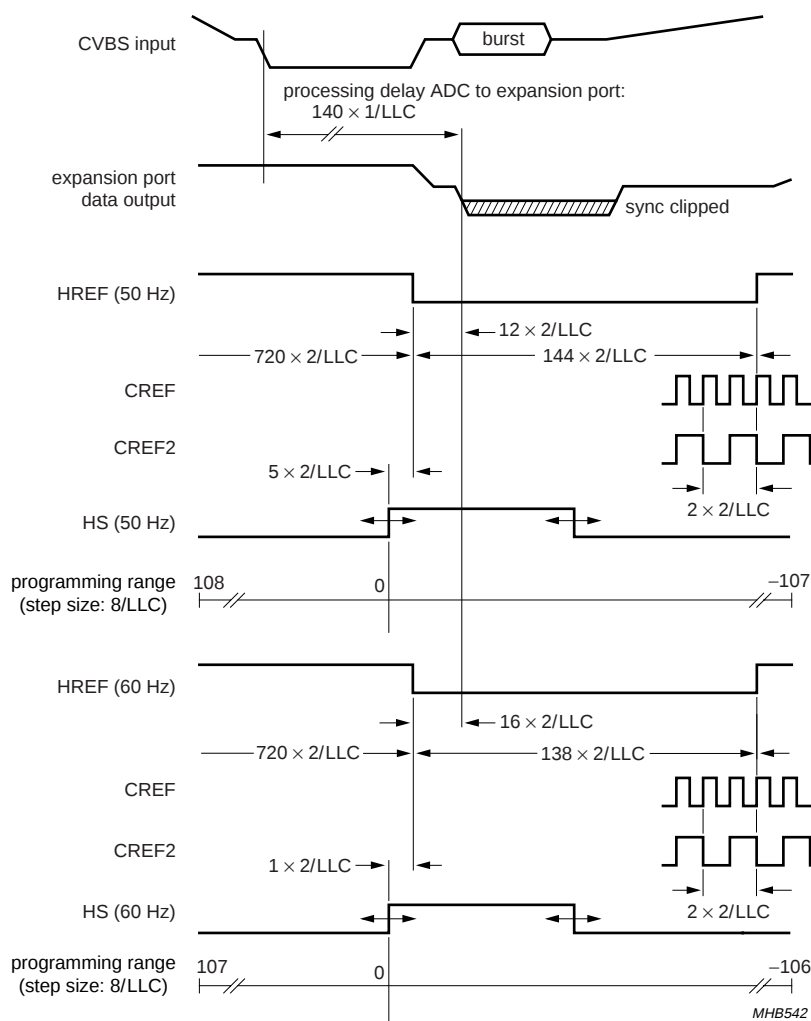
| NAME     | RTS0 | RTS1 | XRH | XRV |
|----------|------|------|-----|-----|
| HREF     | X    | X    | X   | —   |
| F_ITU656 | —    | —    | —   | X   |
| V123     | X    | X    | —   | X   |
| VGATE    | X    | X    | —   | —   |
| FID      | X    | X    | —   | —   |

For further information see Section 15.2: Tables 57, 58 and 59.

Fig.23 Vertical timing diagram for 60 Hz/525 line systems.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



The signals HREF, HS, CREF2 and CREF are available on pins RTS0 and/or RTS1 (see Section 15.2.19 Tables 57 and 58); their polarity can be inverted via RTP0 and/or RTP1.

The signals HREF and HS are available on pin XRH (see Section 15.2.20 Table 59).

Fig.24 Horizontal timing diagram (50/60 Hz).

## PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

### 8.3 Scaler

The High Performance video Scaler (HPS) is based on the system as implemented in previous products (e.g. SAA7140), but with some aspects enhanced. Vertical upsampling is supported and the processing pipeline buffer capacity is enhanced, to allow more flexible video stream timing at the image port, discontinuous transfers, and handshake. The internal data flow from block to block is discontinuous dynamically, due to the scaling process.

The flow is controlled by internal data valid and data request flags (internal handshake signalling) between the sub-blocks; therefore the entire scaler acts as a pipeline buffer. Depending on the actually programmed scaling parameters the effective buffer can exceed to an entire line. The access/bandwidth requirements to the VGA frame buffer are reduced significantly.

The high performance video scaler in the SAA7114 has the following major blocks:

- Acquisition control (horizontal and vertical timer) and task handling (the region/field/frame based processing)
- Prescaler, for horizontal downscaling by an integer factor, combined with appropriate band limiting filters, especially anti-aliasing for CIF format
- Brightness, saturation, contrast control for scaled output data
- Line buffer, with asynchronous read and write, to support vertical upscaling (e.g. for videophone application, converting 240 into 288 lines, Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 2)
- Vertical scaling, with phase accurate Linear Phase Interpolation (LPI) for zoom and downscale, or phase accurate Accumulation Mode (ACM) for large downscaling ratios and better alias suppression
- Variable Phase Delay (VPD), operates as horizontal phase accurate interpolation for arbitrary non-integer scaling ratios, supporting conversion between square and rectangular pixel sampling
- Output formatter for scaled Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 2, Y-C<sub>B</sub>-C<sub>R</sub> 4 : 1 : 1 and Y only (format also used for raw data)
- FIFO, 32-bit wide, with 64 pixel capacity in Y-C<sub>B</sub>-C<sub>R</sub> formats
- Output interface, 8 or 16-bit (only if extended by H port) data pins wide, synchronous or asynchronous operation, with stream events on discrete pins, or coded in the data stream.

The overall H and V zooming (HV\_zoom) is restricted by the input/output data rate relationships. With a safety margin of 2% for running in and running out, the maximum HV\_zoom is equal to:

$$0.98 \times \frac{T_{\text{input\_field}} - T_{\text{v\_blanking}}}{\text{in\_pixel} \times \text{in\_lines} \times \text{out\_cycle\_per\_pix} \times T_{\text{out\_clk}}}$$

For example:

1. Input from decoder: 50 Hz, 720 pixel, 288 lines, 16-bit data at 13.5 MHz data rate, 1 cycle per pixel; output: 8-bit data at 27 MHz, 2 cycles per pixel; the maximum HV\_zoom is equal to:

$$0.98 \times \frac{20 \text{ ms} - 24 \times 64 \mu\text{s}}{720 \times 288 \times 2 \times 37 \text{ ns}} = 1.18$$

2. Input from X port: 60 Hz, 720 pixel, 240 lines, 8-bit data at 27 MHz data rate (ITU 656), 2 cycles per pixel; output via I + H port: 16-bit data at 27 MHz clock, 1 cycle per pixel; the maximum HV\_zoom is equal to:

$$0.98 \times \frac{16.666 \text{ ms} - 22 \times 64 \mu\text{s}}{720 \times 240 \times 1 \times 37 \text{ ns}} = 2.34$$

The video scaler receives its input signal from the video decoder or from the expansion port (X port). It gets 16-bit Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 2 input data at a continuous rate of 13.5 MHz from the decoder. Discontinuous data stream can be accepted from the expansion port (X port), normally 8-bit wide ITU 656 such as Y-C<sub>B</sub>-C<sub>R</sub> data, accompanied by a pixel qualifier on XDQ.

The input data stream is sorted into two data paths, one for luminance (or raw samples) and one for time multiplexed chrominance C<sub>B</sub> and C<sub>R</sub> samples. An Y-C<sub>B</sub>-C<sub>R</sub> 4 : 1 : 1 input format is converted to 4 : 2 : 2 for the horizontal prescaling and vertical filter scaling operation.

The scaler operation is defined by two programming pages A and B, representing two different tasks, that can be applied field alternating or to define two regions in a field (e.g. with different scaling range, factors and signal source during odd and even fields).

Each programming page contains control:

- For signal source selection and formats
- For task handling and trigger conditions
- For input and output acquisition window definition
- For H-prescaler, V-scaler and H-phase scaling.

Raw VBI data is handled as a specific input format and needs its own programming page (equals own task).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

In VBI pass through operation the processing of prescaler and vertical scaling has to be set to no-processing, however, the horizontal fine scaling VPD can be activated. Upscaling (oversampling, zooming), free of frequency folding, up to a factor of 3.5 can be achieved, as required by some software data slicing algorithms.

These raw samples are transported through the image port as valid data and can be output as Y only format. The lines are framed by SAV and EAV codes.

## 8.3.1 ACQUISITION CONTROL AND TASK HANDLING (SUBADDRESSES 80H, 90H, 91H, 94H TO 9FH AND C4H TO CFH)

The acquisition control receives horizontal and vertical synchronization signals from the decoder section or from the X port. The acquisition window is generated via pixel and line counters at the appropriate places in the data path. From X port only qualified pixels and lines (lines with qualified pixel) are counted.

The acquisition window parameters are as follows:

- Signal source selection regarding input video stream and formats from the decoder, or from X port (programming bits SCSRC[1:0] 91H[5:4] and FSC[2:0] 91H[2:0])
- **Remark:** The input of raw VBI data from the internal decoder should be controlled via the decoder output formatter and the LCR registers; see Section 8.2
- Vertical offset defined in lines of the video source, parameter YO[11:0] 99H[3:0] 98H[7:0]
- Vertical length defined in lines of the video source, parameter YS[11:0] 9BH[3:0] 9AH[7:0]
- Vertical length defined in number of target lines, as a result of vertical scaling, parameter YD[11:0] 9FH[3:0] 9EH[7:0]
- Horizontal offset defined in number of pixels of the video source, parameter XO[11:0] 95H[3:0] 94H[7:0]
- Horizontal length defined in number of pixels of the video source, parameter XS[11:0] 97H[3:0] 96H[7:0]
- Horizontal destination size, defined in target pixels after fine scaling, parameter XD[11:0] 9DH[3:0] 9CH[7:0].

The source start offset (XO11 to XO0 and YO11 to YO0) opens the acquisition window, and the target size (XD11 to XD0 and YD11 to YD0) closes the window, however the window is cut vertically if there are less output lines than expected. The trigger events for the pixel and line counts are the horizontal and vertical reference edges as defined in subaddress 92H. The task handling is controlled by subaddress 90H; see Section 8.3.1.2.

### 8.3.1.1 Input field processing

The trigger event for the field sequence detection from external signals (X port) are defined in subaddress 92H. From the X port the state of the scalers H reference signal at the time of the V reference edge is taken as field sequence identifier FID. For example, if the falling edge of the XRV input signal is the reference and the state of XRH input is logic 0 at that time, the detected field ID is logic 0.

The bits XFDV[92H[7]] and XFDH[92H[6]] define the detection event and state of the flag from the X port. For the default setting of XFDV and XFDH at '00' the state of the H-input at the falling edge of the V-input is taken.

The scaler directly gets a corresponding field ID information from the SAA7114 decoder path.

The FID flag is used to determine whether the first or second field of a frame is going to be processed within the scaler and it is used as trigger condition for the task handling (see bits STRC[1:0] 90H[1:0]).

According to ITU 656, when FID is at logic 0 means first field of a frame. To ease the application, the polarities of the detection results on the X port signals and the internal decoder ID can be changed via XFDH.

As the V-sync from the decoder path has a half line timing (due to the interlaced video signal), but the scaler processing only knows about full lines, during 1st fields from the decoder the line count of the scaler possibly shifts by one line, compared to the 2nd field. This can be compensated for by switching the V-trigger event, as defined by XDVO, to the opposite V-sync edge or by using the vertical scalers phase offsets. The vertical timing of the decoder can be seen in Figs 22 and 23.

As the H and V reference events inside the ITU 656 data stream (from X port) and the real-time reference signals from the decoder path are processed differently, the trigger events for the input acquisition also have to be programmed differently.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 9** Processing trigger and start

| XDV1<br>92H[5] | XDV0<br>92H[4] | XDH<br>92H[2] | DESCRIPTION                                                                                                                                                                                               |
|----------------|----------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                |                |               | <b>Internal decoder:</b> The processing triggers at the falling edge of the V123 pulse [see Figs 22 (50 Hz) and 23 (60 Hz)], and starts earliest with the rising edge of the decoder HREF at line number: |
| 0              | 1              | 0             | 4/7 (50/60 Hz, 1st field), respectively 3/6 (50/60 Hz, 2nd field) (decoder count)                                                                                                                         |
| 0              | 0              | 0             | 2/5 (50/60 Hz, 1st field), respectively 2/5 (50/60 Hz, 2nd field) (decoder count)                                                                                                                         |
| 0              | 0              | 0             | <b>External ITU 656 stream:</b> The processing starts earliest with SAV at line number 23 (50 Hz system), respectively line 20 (60 Hz system) (according to ITU 656 count)                                |

## 8.3.1.2 Task handling

The task handler controls the switching between the two programming register sets. It is controlled by subaddresses 90H and C0H. A task is enabled via the global control bits TEA[80H[4]] and TEB[80H[5]].

The handler is then triggered by events, which can be defined for each register set.

In the event of a programming error the task handling and the complete scaler can be reset to the initial states by setting the software reset bit SWRST[88H[5]] to logic 0. Especially if the programming registers, related acquisition window and scale are reprogrammed while a task is active, a software reset **must** be performed after programming.

Contrary to the disabling/enabling of a task, which is evaluated at the end of a running task, when SWRST is at logic 0 it sets the internal state machines directly to their idle states.

The start condition for the handler is defined by bits STRC[1:0] 90H[1:0] and means: start immediately, wait for next V-sync, next FID at logic 0 or next FID at logic 1. The FID is evaluated, if the vertical and horizontal offsets are reached.

When RPTSK[90H[2]] is at logic 1 the actual running task is repeated (under the defined trigger conditions), before handing control over to the alternate task.

To support field rate reduction, the handler is also enabled to skip fields (bits FSKP[2:0] 90H[5:3]) before executing the task. A TOGGLE flag is generated (used for the correct output field processing), which changes state at the beginning of a task, every time a task is activated; examples are given in Section 8.3.1.3.

## Remarks:

- **To activate a task the start condition must be fulfilled and the acquisition window offsets must be reached.**

For example, in case of 'start immediately', and two regions are defined for one field, the offset of the lower region must be greater than (offset + length) of the upper region, if not, the actual counted H and V position at the end of the upper task is beyond the programmed offsets and the processing will 'wait for next V'.

- **Basically the trigger conditions are checked, when a task is activated.** It is important to realize, that they are not checked while a task is inactive. So you can not trigger to next logic 0 or logic 1 with overlapping offset and active video ranges between the tasks (e.g. task A STRC[2:0] = 2, YO[11:0] = 310 and task B STRC[2:0] = 3, YO[11:0] = 310 results in output field rate of  $50\frac{2}{3}$  Hz).
- **After power-on or software reset (via SWRST[88H[5]]) task B gets priority over task A.**

## 8.3.1.3 Output field processing

As a reference for the output field processing, two signals are available for the back-end hardware.

These signals are the input field ID from the scaler source and a TOGGLE flag, which shows that an active task is used an odd (1, 3, 5...) or even (2, 4, 6...) number of times. Using a single or both tasks and reducing the field or frame rate with the task handling function, the TOGGLE information can be used to reconstruct an interlaced scaled picture at a reduced frame rate. The TOGGLE flag isn't synchronized to the input field detection, as it is only dependent on the interpretation of this information by the external hardware, whether the output of the scaler is processed correctly; see Section 8.3.3.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

With OFIDC = 0, the scalers input field ID is available as output field ID on bit D6 of SAV and EAV, respectively on pin IGP0 (IGP1), if FID output is selected.

When OFIDC[90H[6]] = 1, the TOGGLE information is available as output field ID on bit D6 of SAV and EAV, respectively on pin IGP0 (IGP1), if FID output is selected.

Additionally the bit D7 of SAV and EAV can be defined via CONLH[90H[7]]. CONLH[90H[7]] = 0 (default) sets D7 to logic 1, a logic 1 inverts the SAV/EAV bit D7. So it is possible to mark the output of the both tasks by different SAV/EAV codes. This bit can also be seen as 'task flag' on the pins IGP0 (IGP1), if TASK output is selected.

**Table 10** Examples for field processing

| SUBJECT                                                            | FIELD SEQUENCE FRAME/FIELD |               |               |                             |               |               |               |                                |               |               |               |               |               |                                |               |               |                  |               |               |
|--------------------------------------------------------------------|----------------------------|---------------|---------------|-----------------------------|---------------|---------------|---------------|--------------------------------|---------------|---------------|---------------|---------------|---------------|--------------------------------|---------------|---------------|------------------|---------------|---------------|
|                                                                    | EXAMPLE 1 <sup>(1)</sup>   |               |               | EXAMPLE 2 <sup>(2)(3)</sup> |               |               |               | EXAMPLE 3 <sup>(2)(4)(5)</sup> |               |               |               |               |               | EXAMPLE 4 <sup>(2)(4)(6)</sup> |               |               |                  |               |               |
|                                                                    | 1/1                        | 1/2           | 2/1           | 1/1                         | 1/2           | 2/1           | 2/2           | 1/1                            | 1/2           | 2/1           | 2/2           | 3/1           | 3/2           | 1/1                            | 1/2           | 2/1           | 2/2              | 3/1           | 3/2           |
| Processed by task                                                  | A                          | A             | A             | B                           | A             | B             | A             | B                              | B             | A             | B             | B             | A             | B                              | B             | A             | B                | B             | A             |
| State of detected ITU 656 FID                                      | 0                          | 1             | 0             | 0                           | 1             | 0             | 1             | 0                              | 1             | 0             | 1             | 0             | 1             | 0                              | 1             | 0             | 1                | 0             | 1             |
| TOGGLE flag                                                        | 1                          | 0             | 1             | 1                           | 1             | 0             | 0             | 1                              | 0             | 1             | 1             | 0             | 0             | 0 <sup>(7)</sup>               | 1             | 1             | 1 <sup>(7)</sup> | 0             | 0             |
| Bit D6 of SAV/EAV byte                                             | 0                          | 1             | 0             | 0                           | 1             | 0             | 1             | 1                              | 0             | 1             | 1             | 0             | 0             | 0 <sup>(7)</sup>               | 1             | 1             | 1 <sup>(7)</sup> | 0             | 0             |
| Required sequence conversion at the vertical scaler <sup>(8)</sup> | UP<br>↓<br>UP              | LO<br>↓<br>LO | UP<br>↓<br>UP | UP<br>↓<br>UP               | LO<br>↓<br>LO | UP<br>↓<br>UP | LO<br>↓<br>LO | UP<br>↓<br>LO                  | LO<br>↓<br>UP | UP<br>↓<br>LO | LO<br>↓<br>LO | UP<br>↓<br>UP | LO<br>↓<br>UP | UP<br>↓<br>UP                  | LO<br>↓<br>LO | UP<br>↓<br>LO | LO<br>↓<br>LO    | UP<br>↓<br>UP | LO<br>↓<br>UP |
| Output <sup>(9)</sup>                                              | O                          | O             | O             | O                           | O             | O             | O             | O                              | O             | O             | O             | O             | O             | NO                             | O             | O             | NO               | O             | O             |

**Notes**

1. Single task every field; OFIDC = 0; subaddress 90H at 40H; TEB[80H[5]] = 0.
2. Tasks are used to scale to different output windows, priority on task B after SWRST.
3. Both tasks at  $\frac{1}{2}$  frame rate; OFIDC = 0; subaddresses 90H at 43H and C0H at 42H.
4. In examples 3 and 4 the association between input FID and tasks can be flipped, dependent on which time the SWRST is de-asserted.
5. Task B at  $\frac{2}{3}$  frame rate constructed from neighbouring motion phases; task A at  $\frac{1}{3}$  frame rate of equidistant motion phases; OFIDC = 1; subaddresses 90H at 41H and C0H at 45H.
6. Task A and B at  $\frac{1}{3}$  frame rate of equidistant motion phases; OFIDC = 1; subaddresses 90H at 41H and C0H at 49H.
7. State of prior field.
8. It is assumed that input/output FID = 0 (= upper lines); UP = upper lines; LO = lower lines.
9. O = data output; NO = no output.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.3.2 HORIZONTAL SCALING

The overall horizontal required scaling factor has to be split into a binary and a rational value according to the equation:

$$\text{H-scale ratio} = \frac{\text{output pixel}}{\text{input pixel}}$$

$$\text{H-scale ratio} = \frac{1}{\text{XPSC}[5:0]} \times \frac{1024}{\text{XSCY}[12:0]}$$

where the parameter of prescaler  $\text{XPSC}[5:0] = 1$  to 63 and the parameter of VPD phase interpolation  $\text{XSCY}[12:0] = 300$  to 8191 (0 to 299 are only theoretical values). For example,  $\frac{1}{3.5}$  is to split in  $\frac{1}{4} \times 1.14286$ . The binary factor is processed by the prescaler, the arbitrary non-integer ratio is achieved via the variable phase delay VPD circuitry, called horizontal fine scaling. The latter calculates horizontally interpolated new samples with a 6-bit phase accuracy, which relates to less than 1 ns jitter for regular sampling scheme. Prescaler and fine scaler create the horizontal scaler of the SAA7114.

Using the accumulation length function of the prescaler ( $\text{XACL}[5:0]$  A1H[5:0]), application and destination dependent (e.g. scale for display or for a compression machine), a compromise between visible bandwidth and alias suppression can be determined.

### 8.3.2.1 Horizontal prescaler (subaddresses A0H to A7H and D0H to D7H)

The prescaling function consists of an FIR anti-alias filter stage and an integer prescaler, which creates an adaptive prescale dependent low-pass filter to balance sharpness and aliasing effects.

The FIR prefilter stage implements different low-pass characteristics to reduce alias for downscales in the range of 1 to  $\frac{1}{2}$ . A CIF optimized filter is built-in, which reduces artefacts for CIF output formats (to be used in combination with the prescaler set to  $\frac{1}{2}$  scale); see Table 11.

The function of the prescaler is defined by:

- An integer prescaling ratio  $\text{XPSC}[5:0]$  A0H[5:0] (equals 1 to 63), which covers the integer downscale range 1 to  $\frac{1}{63}$
- An averaging sequence length  $\text{XACL}[5:0]$  A1H[5:0] (equals 0 to 63); range 1 to 64
- A DC gain renormalization  $\text{XDCG}[2:0]$  A2H[2:0]; 1 down to  $\frac{1}{128}$

- The bit  $\text{XC2\_1}[A2H[3]]$ , which defines the weighting of the incoming pixels during the averaging process:

- $\text{XC2\_1} = 0 \Rightarrow 1 + 1 \dots + 1 + 1$
- $\text{XC2\_1} = 1 \Rightarrow 1 + 2 \dots + 2 + 1$ .

The prescaler creates a prescale dependent FIR low-pass, with up to (64 + 7) filter taps. The parameter  $\text{XACL}[5:0]$  can be used to vary the low-pass characteristic for a given integer prescale of  $\frac{1}{\text{XPSC}[5:0]}$ . The user can therefore decide between signal bandwidth (sharpness impression) and alias.

Equation for  $\text{XPSC}[5:0]$  calculation is:

$$\text{XPSC}[5:0] = \text{lower integer of } \frac{\text{Npix\_in}}{\text{Npix\_out}}$$

Where:

the range is 1 to 63 (**value 0 is not allowed**);

Npix\_in = number of input pixel, and

Npix\_out = number of desired output pixel over the complete horizontal scaler.

**The use of the prescaler results in a  $\text{XACL}[5:0]$  and  $\text{XC2\_1}$  dependent gain amplification.** The amplification can be calculated according to the equation:

$$\text{DC gain} = (\text{XC2\_1} + 1) \times \text{XACL}[5:0] + (1 - \text{XC2\_1})$$

It is recommended to use sequence lengths and weights, which results in a  $2^N$  DC gain amplification, as these amplitudes can be renormalized by the  $\text{XDCG}[2:0]$

controlled  $\frac{1}{2^N}$  shifter of the prescaler.

The renormalization range of  $\text{XDCG}[2:0]$  is 1,  $\frac{1}{2}$  down to  $\frac{1}{128}$ .

Other amplifications have to be normalized by using the following BCS control circuitry. In these cases the prescaler has to be set to an overall gain of  $\leq 1$ , e.g. for an accumulation sequence of '1 + 1 + 1' ( $\text{XACL}[5:0] = 2$  and  $\text{XC2\_1} = 0$ ),  $\text{XDCG}[2:0]$  must be set to '010', this equals  $\frac{1}{4}$  and the BCS has to amplify the signal to  $\frac{4}{3}$  ( $\text{SATN}[7:0]$  and  $\text{CONT}[7:0]$  value = lower integer of  $\frac{4}{3} \times 64$ ).

**The use of  $\text{XACL}[5:0]$  is  $\text{XPSC}[5:0]$  dependent.  $\text{XACL}[5:0]$  must be  $< 2 \times \text{XPSC}[5:0]$ .**

$\text{XACL}[5:0]$  can be used to find a compromise between bandwidth (sharpness) and alias effects.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Remark:** Due to bandwidth considerations XPSC[5:0] and XACL[5:0] can be chosen differently to the previously mentioned equations or Table 12, as the H-phase scaling is able to scale in the range from zooming up by factor 3 to downscaling by a factor of  $1024/8191$ .

Figures 27 and 28 show some resulting frequency characteristics of the prescaler.

Table 12 shows the recommended prescaler programming. Other programmings, other than given in Table 12, may result in better alias suppression, but the resulting DC gain amplification needs to be compensated by the BCS control, according to the equation:

$$\text{CONT}[7:0] = \text{SATN}[7:0] = \text{lower integer of } \frac{2^{\text{XDCG}[2:0]}}{\text{DC gain} \times 64}$$

Where:

$$2^{\text{XDCG}[2:0]} \geq \text{DC gain}$$

$$\text{DC gain} = (\text{XC2\_1} + 1) \times \text{XACL}[5:0] + (1 - \text{XC2\_1}).$$

For example, if XACL[5:0] = 5, XC2\_1 = 1, then the DC gain = 10 and the required XDCG[2:0] = 4.

The horizontal source acquisition timing and the prescaling ratio is identical for both the luminance path and chrominance path, but the FIR filter settings can be defined differently in the two channels.

Fade-in and fade-out of the filters is achieved by copying an original source sample each as first and last pixel after prescaling.

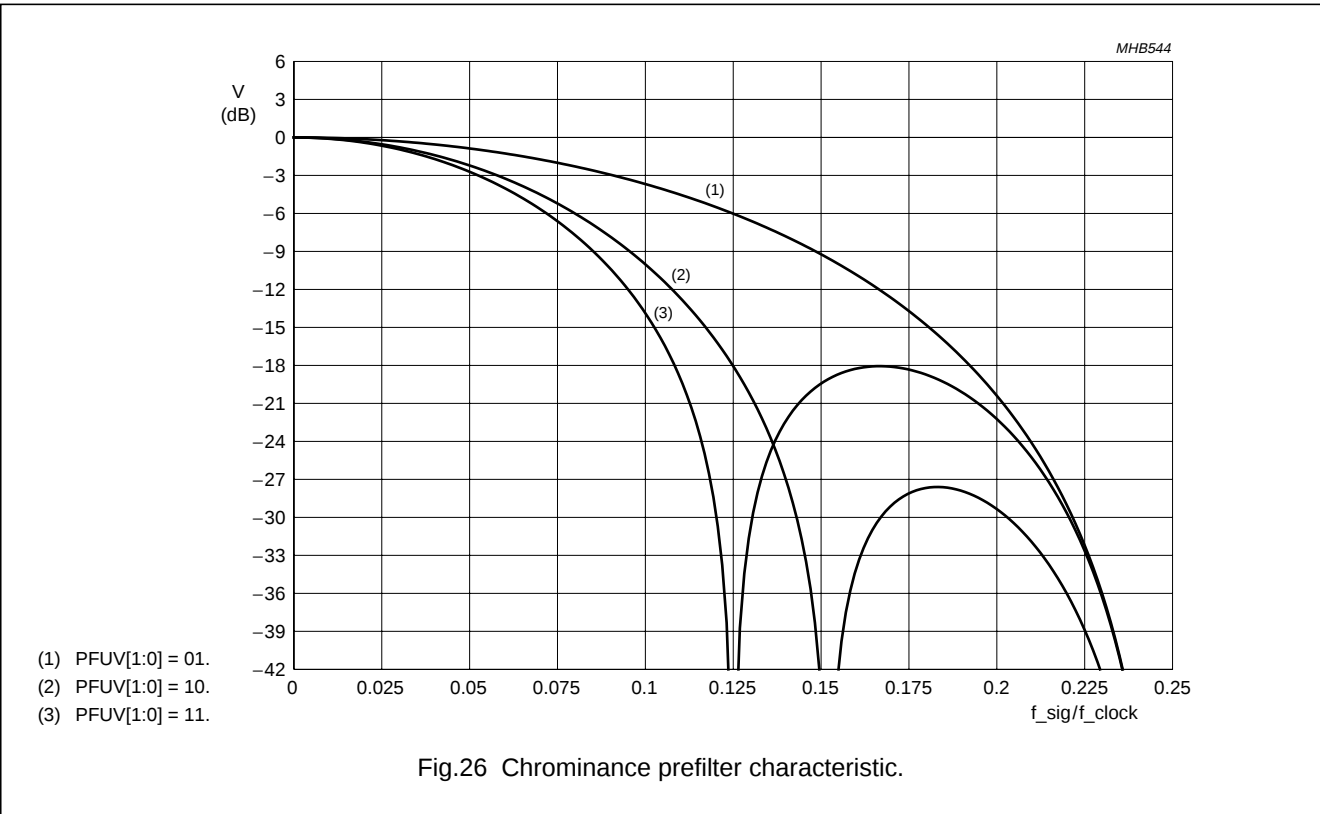
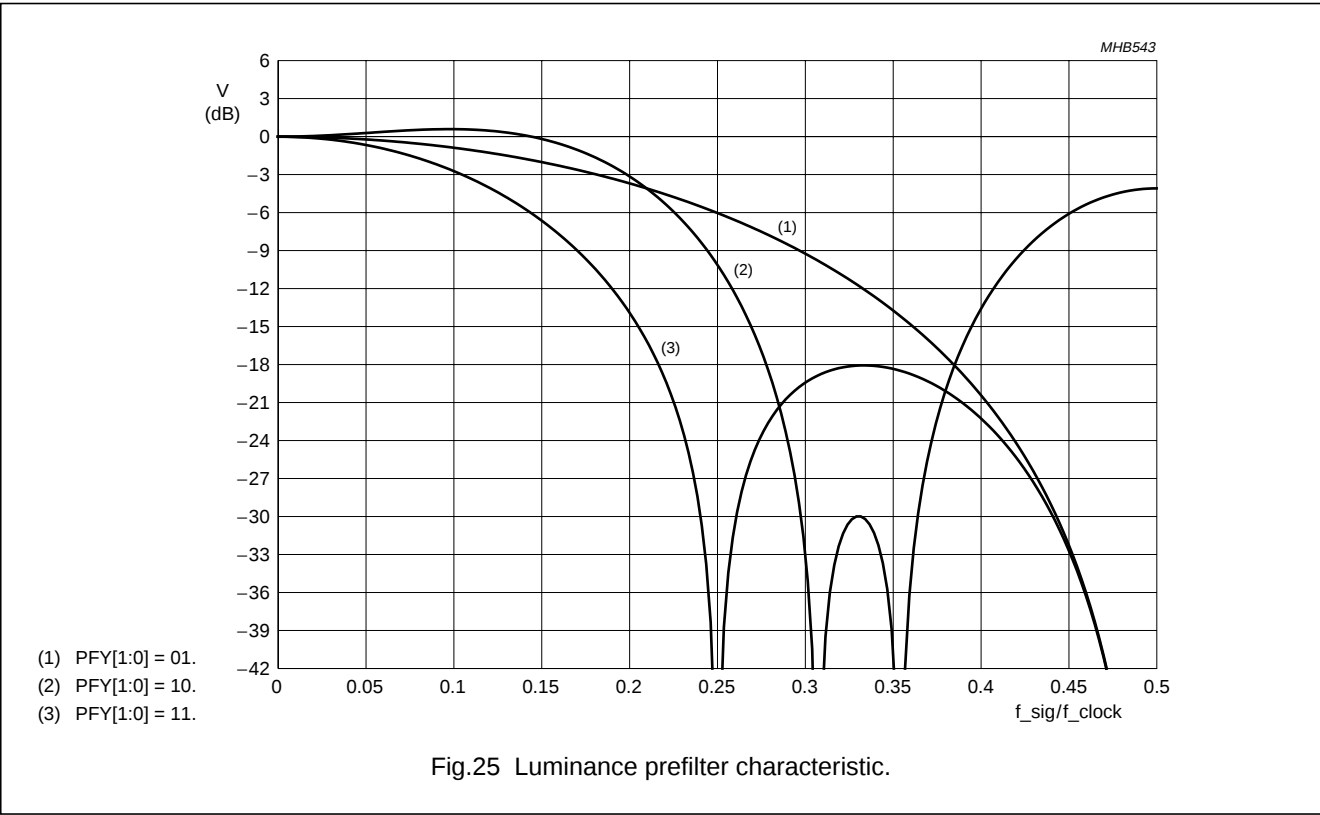
Figures 25 and 26 show the frequency characteristics of the selectable FIR filters.

**Table 11** FIR prefilter functions

| PFUV[1:0] A2H[7:6]<br>PFY[1:0] A2H[5:4] | LUMINANCE FILTER<br>COEFFICIENTS | CHROMINANCE COEFFICIENTS |
|-----------------------------------------|----------------------------------|--------------------------|
| 00                                      | bypassed                         | bypassed                 |
| 01                                      | 1 2 1                            | 1 2 1                    |
| 10                                      | -1 1 1.75 4.5 1.75 1 -1          | 3 8 10 8 3               |
| 11                                      | 1 2 2 2 1                        | 1 2 2 2 1                |

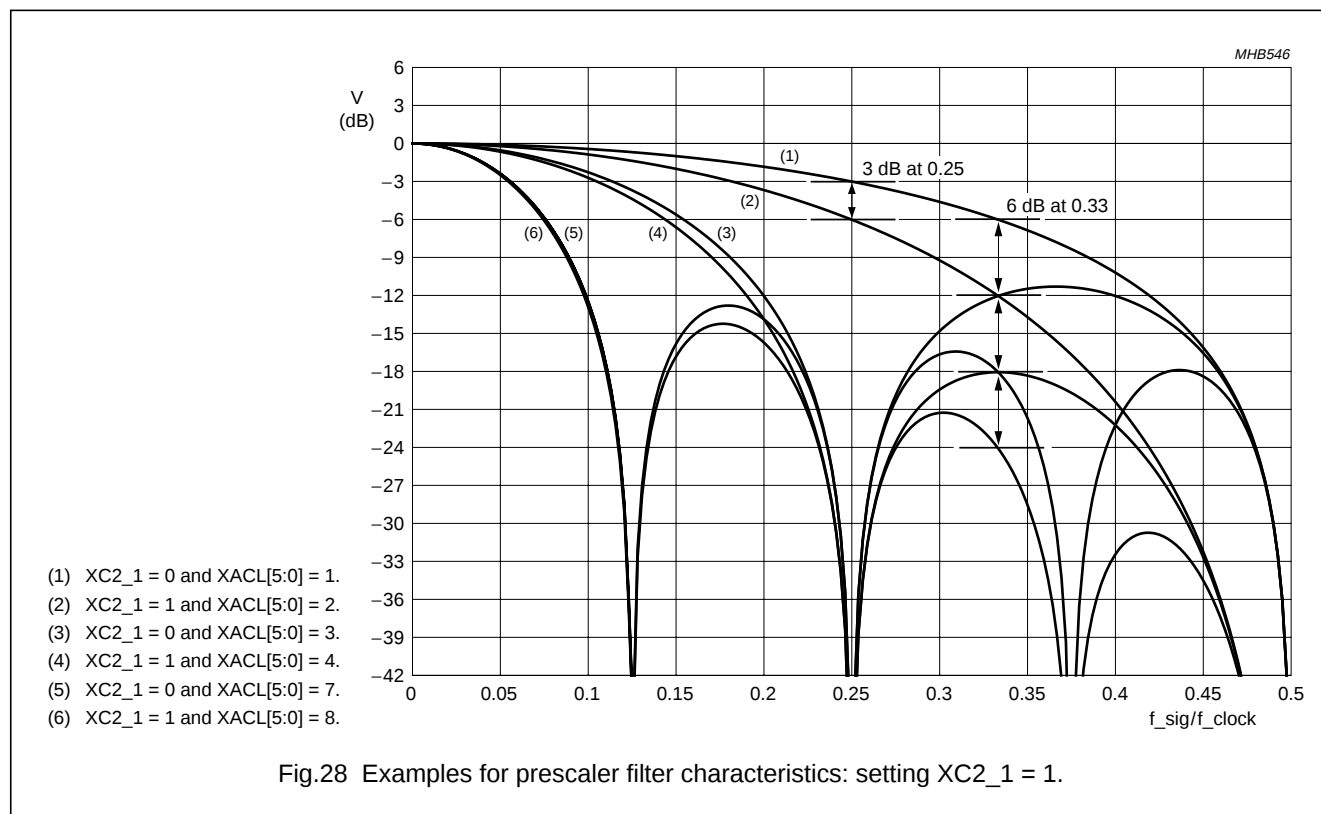
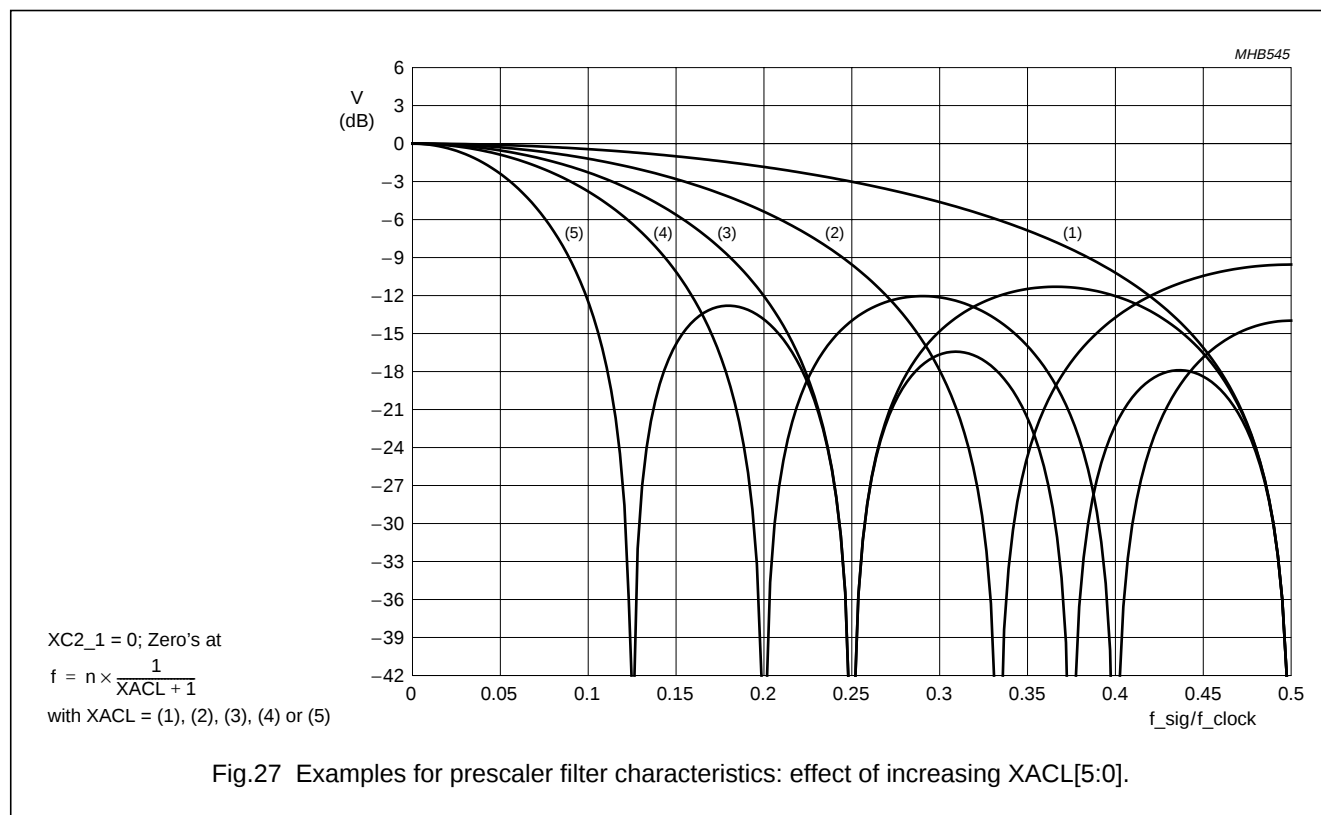
PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114



# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 12** XACL[5:0] example of usage

| PRESCALE<br>RATIO | XPSC<br>[5:0] | RECOMMENDED VALUES                                                              |       |           |                                                         |       |           | FIR<br>PREFILTER<br>PFY[1:0]/<br>PFUV[1:0] |
|-------------------|---------------|---------------------------------------------------------------------------------|-------|-----------|---------------------------------------------------------|-------|-----------|--------------------------------------------|
|                   |               | FOR LOWER BANDWIDTH<br>REQUIREMENTS                                             |       |           | FOR HIGHER BANDWIDTH<br>REQUIREMENTS                    |       |           |                                            |
|                   |               | XACL[5:0]                                                                       | XC2_1 | XDCG[2:0] | XACL[5:0]                                               | XC2_1 | XDCG[2:0] |                                            |
| 1                 | 1             | 0                                                                               | 0     | 0         | 0                                                       | 0     | 0         | 0 to 2                                     |
| $\frac{1}{2}$     | 2             | 2                                                                               | 1     | 2         | 1                                                       | 0     | 1         | 0 to 2                                     |
|                   |               | $(1\ 2\ 1) \times \frac{1}{4}^{(1)}$                                            |       |           | $(1\ 1) \times \frac{1}{2}^{(1)}$                       |       |           |                                            |
| $\frac{1}{3}$     | 3             | 4                                                                               | 1     | 3         | 3                                                       | 0     | 2         | 2                                          |
|                   |               | $(1\ 2\ 2\ 2\ 1) \times \frac{1}{8}^{(1)}$                                      |       |           | $(1\ 1\ 1\ 1) \times \frac{1}{4}^{(1)}$                 |       |           |                                            |
| $\frac{1}{4}$     | 4             | 7                                                                               | 0     | 3         | 4                                                       | 1     | 3         | 2                                          |
|                   |               | $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1) \times \frac{1}{8}^{(1)}$                             |       |           | $(1\ 2\ 2\ 2\ 1) \times \frac{1}{8}^{(1)}$              |       |           |                                            |
| $\frac{1}{5}$     | 5             | 8                                                                               | 1     | 4         | 7                                                       | 0     | 3         | 2                                          |
|                   |               | $(1\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 1) \times \frac{1}{16}^{(1)}$                         |       |           | $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1) \times \frac{1}{8}^{(1)}$     |       |           |                                            |
| $\frac{1}{6}$     | 6             | 8                                                                               | 1     | 4         | 7                                                       | 0     | 3         | 3                                          |
|                   |               | $(1\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 1) \times \frac{1}{16}^{(1)}$                         |       |           | $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1) \times \frac{1}{8}^{(1)}$     |       |           |                                            |
| $\frac{1}{7}$     | 7             | 8                                                                               | 1     | 4         | 7                                                       | 0     | 3         | 3                                          |
|                   |               | $(1\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 1) \times \frac{1}{16}^{(1)}$                         |       |           | $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1) \times \frac{1}{8}^{(1)}$     |       |           |                                            |
| $\frac{1}{8}$     | 8             | 15                                                                              | 0     | 4         | 8                                                       | 1     | 4         | 3                                          |
|                   |               | $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1) \times \frac{1}{16}^{(1)}$    |       |           | $(1\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 1) \times \frac{1}{16}^{(1)}$ |       |           |                                            |
| $\frac{1}{9}$     | 9             | 15                                                                              | 0     | 4         | 8                                                       | 1     | 4         | 3                                          |
|                   |               | $(1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1) \times \frac{1}{16}^{(1)}$    |       |           | $(1\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 1) \times \frac{1}{16}^{(1)}$ |       |           |                                            |
| $\frac{1}{10}$    | 10            | 16                                                                              | 1     | 5         | 8                                                       | 1     | 4         | 3                                          |
|                   |               | $(1\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 1) \times \frac{1}{32}^{(1)}$ |       |           | $(1\ 2\ 2\ 2\ 2\ 2\ 2\ 2\ 1) \times \frac{1}{16}^{(1)}$ |       |           |                                            |
| $\frac{1}{13}$    | 13            | 16                                                                              | 1     | 5         | 16                                                      | 1     | 5         | 3                                          |
| $\frac{1}{15}$    | 15            | 31                                                                              | 0     | 5         | 16                                                      | 1     | 5         | 3                                          |
| $\frac{1}{16}$    | 16            | 32                                                                              | 1     | 6         | 16                                                      | 1     | 5         | 3                                          |
| $\frac{1}{19}$    | 19            | 32                                                                              | 1     | 6         | 32                                                      | 1     | 6         | 3                                          |
| $\frac{1}{31}$    | 31            | 32                                                                              | 1     | 6         | 32                                                      | 1     | 6         | 3                                          |
| $\frac{1}{32}$    | 32            | 63                                                                              | 1     | 7         | 32                                                      | 1     | 6         | 3                                          |
| $\frac{1}{35}$    | 35            | 63                                                                              | 1     | 7         | 63                                                      | 1     | 7         | 3                                          |

**Note**

1. Resulting FIR function.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.3.2.2 Horizontal fine scaling (variable phase delay filter; subaddresses A8H to AFH and D8H to DFH)

The horizontal fine scaling (VPD) should operate at scaling ratios between  $\frac{1}{2}$  and 2 (0.8 and 1.6), but can also be used for direct scaling in the range from  $\frac{1}{7.999}$  to (theoretical) zoom 3.5 (restriction due to the internal data path architecture), without prescaler.

In combination with the prescaler a compromise between sharpness impression and alias can be found. This is signal source and application dependent.

For the luminance channel a filter structure with 10 taps is implemented, and for the chrominance a filter with 4 taps.

Luminance and chrominance scale increments (XSCY[12:0] A9H[4:0] A8H[7:0] and XSCC[12:0] ADH[4:0] ACH[7:0]) are defined independently, but must be set in a 2 : 1 relationship in the actual data path implementation. The phase offsets XPHY[7:0] AAH[7:0] and XPHC[7:0] AEH[7:0] can be used to shift the sample phases slightly. XPHY[7:0] and XPHC[7:0] covers the phase offset range  $7.999T$  to  $\frac{1}{32}T$ . The phase offsets should also be programmed in a 2 : 1 ratio.

The underlying phase controlling DTO has a 13-bit resolution.

According to the equations

$$XSCY[12:0] = 1024 \times \frac{N_{pix\_in}}{X_{PSC}[5:0]} \times \frac{1}{N_{pix\_out}} \text{ and}$$

$$XSCC[12:0] = \frac{XSCY[12:0]}{2}$$

the VPD covers the scale range from 0.125 to zoom 3.5. VPD acts equivalent to a polyphase filter with 64 possible phases. In combination with the prescaler, it is possible to get very accurate samples from a highly anti-aliased integer downsampled input picture.

## 8.3.3 VERTICAL SCALING

The vertical scaler of the SAA7114 consists of a line FIFO buffer for line repetition and the vertical scaler block, which implements the vertical scaling on the input data stream in 2 different operational modes from theoretical zoom by 64 down to icon size  $\frac{1}{64}$ . The vertical scaler is located between the BCS and horizontal fine scaler, so that the BCS can be used to compensate the DC gain amplification of the ACM mode (see Section 8.3.3.2) as the internal RAMs are only 8-bit wide.

## 8.3.3.1 Line FIFO buffer (subaddresses 91H, B4H and C1H, E4H)

The line FIFO buffer is a dual ported RAM structure for 768 pixels, with asynchronous write and read access. The line buffer can be used for various functions, but not all functions may be available simultaneously.

The line buffer can buffer a complete unscaled active video line or more than one shorter lines (only for non-mirror mode), for selective repetition for vertical zoom-up.

For zooming up 240 lines to 288 lines e.g., every fourth line is requested (read) twice from the vertical scaling circuitry for calculation.

For conversion of a 4 : 2 : 0 or 4 : 1 : 0 input sampling scheme (MPEG, video phone, Indeo YUV-9) to ITU like sampling scheme 4 : 2 : 2, the chrominance line buffer is read twice or four times, before being refilled again by the source. It has to be preserved by means of the input acquisition window definition, so that the processing starts with a line containing luminance and chrominance information for 4 : 2 : 0 and 4 : 1 : 0 input. The bits FSC[2:1] 91H[2:1] define the distance between the Y/C lines. In the event of 4 : 2 : 2 and 4 : 1 : 1 FSC2 and FSC1 have to be set to '00'.

The line buffer can also be used for mirroring, i.e. for flipping the image left to right, for the vanity picture in video phone applications (bit YMIR[B4H[4]]). In mirror mode only one active prescaled line can be held in the FIFO at a time.

The line buffer can be utilized as an excessive pipeline buffer for discontinuous and variable rate transfer conditions at the expansion port or image port.

## PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

### 8.3.3.2 Vertical scaler (subaddresses B0H to BFH and E0H to EFH)

Vertical scaling of any ratio from 64 (theoretical zoom) to  $\frac{1}{63}$  (icon) can be applied.

The vertical scaling block consists of another line delay, and the vertical filter structure, that can operate in two different modes; Linear Phase Interpolation (LPI) and accumulation (ACM) mode. These are controlled by YMODE[B4H[0]]:

- **LPI mode:** In LPI mode (YMODE = 0) two neighbouring lines of the source video stream are added together, but weighted by factors corresponding to the vertical position (phase) of the target output line relative to the source lines. This linear interpolation has a 6-bit phase resolution, which equals 64 intra line phases. It interpolates between two consecutive input lines only. LPI mode should be applied for scaling ratios around 1 (down to  $\frac{1}{2}$ ), **it must be applied for vertical zooming.**
- **ACM mode:** The vertical Accumulation (ACM) mode (YMODE = 1) represents a vertical averaging window over multiple lines, sliding over the field. This mode also generates phase correct output lines. The averaging window length corresponds to the scaling ratio, resulting in an adaptive vertical low-pass effect, to greatly reduce aliasing artefacts. ACM can be applied for downscalers only from ratio 1 down to  $\frac{1}{64}$ . ACM results in a scale dependent **DC gain amplification**, which has to be precorrected by the BCS control of the scaler part.

The phase and scale controlling DTO calculates in 16-bit resolution, controlled by parameters YSCY[15:0] B1H[7:0] B0H[7:0] and YSCC[15:0] B3H[7:0] B2H[7:0], continuously over the entire field. A start offset can be applied to the phase processing by means of the parameters YPY3[7:0] to YPY0[7:0] in BFH[7:0] to BCH[7:0] and YPC3[7:0] to YPC0[7:0] in BBH[7:0] to B8H[7:0]. The start phase covers the range of  $\frac{255}{32}$  to  $\frac{1}{32}$  lines offset.

By programming appropriate, opposite, vertical start phase values (subaddresses B8H to BFH and E8H to EFH) depending on odd or even field ID of the source video stream and A or B page cycle, frame ID conversion and field rate conversion are supported (i.e. de-interlacing, re-interlacing).

Figures 29 and 30 and Tables 13 and 14 describe the use of the offsets.

**Remark: The vertical start phase, as well as scaling ratio are defined independently for the luminance and chrominance channel, but must be set to the same values in the actual implementation for accurate 4 : 2 : 2 output processing.**

The vertical processing communicates on its input side with the line FIFO buffer. The scale related equations are:

- Scaling increment calculation for ACM and LPI mode, downscale and zoom: YSCY[15:0] and YSCC[15:0]

$$= \text{lower integer of } \left( 1024 \times \frac{N_{\text{line\_in}}}{N_{\text{line\_out}}} \right)$$

- BCS value to compensate DC gain in ACM mode (contrast and saturation have to be set): CONT[7:0] A5H[7:0] respectively SATN[7:0] A6H[7:0]

$$= \text{lower integer of } \left( \frac{N_{\text{line\_out}}}{N_{\text{line\_in}}} \times 64 \right), \text{ or}$$

$$= \text{lower integer of } \left( \frac{1024}{YSCY[15:0]} \times 64 \right)$$

### 8.3.3.3 Use of the vertical phase offsets

As described in Section 8.3.1.3, the scaler processing may run randomly over the interlaced input sequence. Additionally the interpretation and timing between ITU 656 field ID and real-time detection by means of the state of H-sync at the falling edge of V-sync may result in different field ID interpretation.

A vertically scaled interlaced output also gets a larger vertical sampling phase error, if the interlaced input fields are processed, without regard to the actual scale at the starting point of operation (see Fig.29).

For correct interlaced processing the vertical scaler must be used with respect to the interlace properties of the input signal and, if required, for conversion of the field sequences.

Four events should be considered, they are illustrated in Fig.30.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

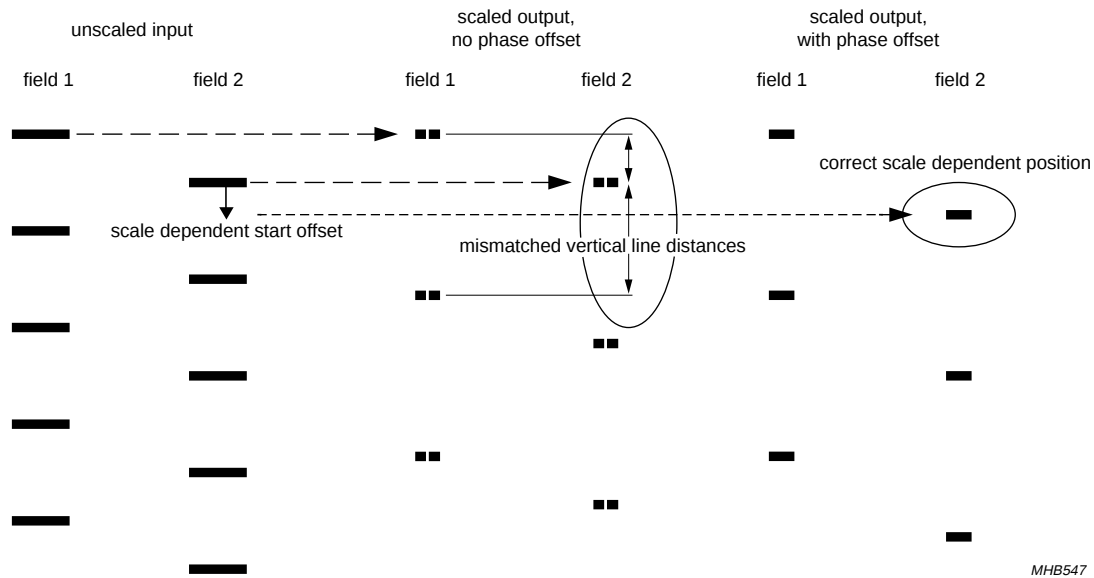
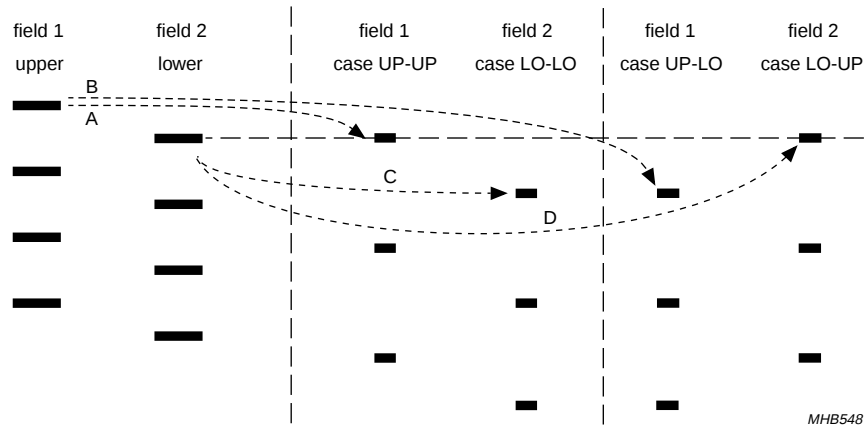


Fig.29 Basic problem of interlaced vertical scaling (example: downscale  $\frac{3}{5}$ ).



$$\text{Offset} = \frac{1024}{32} = 32 = 1 \text{ line shift}$$

$$A = \frac{1}{2} \text{ input line shift} = 16$$

$$B = \frac{1}{2} \text{ input line shift} + \frac{1}{2} \text{ scale increment} = \frac{\text{YSCY}[15:0]}{64} + 16$$

$$C = \frac{1}{2} \text{ scale increment} = \frac{\text{YSCY}[15:0]}{64}$$

$$D = \text{no offset} = 0$$

Fig.30 Derivation of the phase related equations (example: interlace vertical scaling down to  $\frac{3}{5}$ , with field conversion).

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

In Tables 13 and 14 PHO is a usable common phase offset.

It should be noted that the equations of Fig.30 produce an interpolated output, also for the unscaled case, as the geometrical reference position for all conversions is the position of the first line of the lower field; see Table 13.

If there is no need for UP-LO and LO-UP conversion and the input field ID is the reference for the back-end operation, then it is UP-LO = UP-UP and LO-UP = LO-LO and the  $\frac{1}{2}$  line phase shift (PHO + 16) that can be skipped. This case is listed in Table 14.

The SAA7114 supports 4 phase offset registers per task and component (luminance and chrominance). The value of 20H represents a phase shift of one line.

The registers are assigned to the following events; e.g. subaddresses B8H to BBH:

- B8H: 00 = input field ID 0, task status bit D0 (toggle status; see Section 8.3.1.3)
- B9H: 01 = input field ID 0, task status bit D1
- BAH: 10 = input field ID 1, task status bit D0
- BBH: 11 = input field ID 1, task status bit D1.

Depending on the input signal (interlaced or non-interlaced) and the task processing 50 Hz or field reduced processing with one or two tasks (see examples in Section 8.3.1.3), other combinations may also be possible, but the basic equations are the same.

Table 13 Examples for vertical phase offset usage: global equations

| INPUT FIELD UNDER PROCESSING | OUTPUT FIELD INTERPRETATION | USED ABBREVIATION | EQUATION FOR PHASE OFFSET CALCULATION (DECIMAL VALUES) |
|------------------------------|-----------------------------|-------------------|--------------------------------------------------------|
| Upper input lines            | upper output lines          | UP-UP             | PHO + 16                                               |
| Upper input lines            | lower output lines          | UP-LO             | $PHO + \frac{YSCY[15:0]}{64} + 16$                     |
| Lower input lines            | upper output lines          | LO-UP             | PHO                                                    |
| Lower input lines            | lower output lines          | LO-LO             | $PHO + \frac{YSCY[15:0]}{64}$                          |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 14** Vertical phase offset usage; assignment of the phase offsets

| DETECTED INPUT FIELD ID | TASK STATUS BIT | VERTICAL PHASE OFFSET   | CASE                  | EQUATION TO BE USED                                     |
|-------------------------|-----------------|-------------------------|-----------------------|---------------------------------------------------------|
| 0 = upper lines         | 0               | YPY0[7:0] and YPC0[7:0] | case 1 <sup>(1)</sup> | UP-UP (PHO)                                             |
|                         |                 |                         | case 2 <sup>(2)</sup> | UP-UP                                                   |
|                         |                 |                         | case 3 <sup>(3)</sup> | UP-LO                                                   |
| 0 = upper lines         | 1               | YPY1[7:0] and YPC1[7:0] | case 1                | UP-UP (PHO)                                             |
|                         |                 |                         | case 2                | UP-LO                                                   |
|                         |                 |                         | case 3                | UP-UP                                                   |
| 1 = lower lines         | 0               | YPY2[7:0] and YPC2[7:0] | case 1                | $LO-LO \left( PHO + \frac{YSCY[15:0]}{64} - 16 \right)$ |
|                         |                 |                         | case 2                | LO-UP                                                   |
|                         |                 |                         | case 3                | LO-LO                                                   |
| 1 = lower lines         | 1               | YPY3[7:0] and YPC3[7:0] | case 1                | $LO-LO \left( PHO + \frac{YSCY[15:0]}{64} - 16 \right)$ |
|                         |                 |                         | case 2                | LO-LO                                                   |
|                         |                 |                         | case 3                | LO-UP                                                   |

**Notes**

- Case 1: OFIDC[90H[6]] = 0; scaler input field ID as output ID; back-end interprets output field ID at logic 0 as upper output lines.
- Case 2: OFIDC[90H[6]] = 1; task status bit as output ID; back-end interprets output field ID at logic 0 as upper output lines.
- Case 3: OFIDC[90H[6]] = 1; task status bit as output ID; back-end interprets output field ID at logic 1 as upper output lines.

## 8.4 VBI data decoder and capture (subaddresses 40H to 7FH)

The SAA7114 contains a versatile VBI data decoder.

The implementation and programming model is in accordance with the VBI data slicer built into the multimedia video data acquisition circuit SAA5284.

The circuitry recovers the actual clock phase during the clock run-in period, slices the data bits with the selected data rate, and groups them into bytes. The result is buffered into a dedicated VBI data FIFO with a capacity of  $2 \times 56$  bytes ( $2 \times 14$  Dwords). The clock frequency, signal source, field frequency and accepted error count must be defined in subaddress 40H.

The supported VBI data standards are shown in Table 15.

For lines 2 to 24 of a field, per VBI line, 1 of 16 standards can be selected (LCR24\_[7:0] to LCR2\_[7:0] in 57H[7:0] to 41H[7:0]:  $23 \times 2 \times 4$  bit programming bits).

The definition for line 24 is valid for the rest of the corresponding field, normally no text data (video data) should be selected there (LCR24\_[7:0] = FFH) to stop the activity of the VBI data slicer during active video.

To adjust the slicers processing to the input signal source, there are offsets in the horizontal and vertical direction available: parameters HOFF[10:0] 5BH[2:0] 59H[7:0], VOFF[8:0] 5BH[4] 5AH[7:0] and FFFF[5BH[7]].

Contrary to the scalers counting, the slicers offsets define the position of the H and V trigger events related to the processed video field. The trigger events are the falling edge of HREF and the falling edge of V123 from the decoder processing part.

The relationship of these programming values to the input signal and the recommended values are given in Tables 5 to 8.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 15** Data types supported by the data slicer block

| DT[3:0]<br>62H[3:0] | STANDARD TYPE                                       | DATA RATE<br>(Mbits/s) | FRAMING CODE       | FC<br>WINDOW | HAM<br>CHECK |
|---------------------|-----------------------------------------------------|------------------------|--------------------|--------------|--------------|
| 0000                | teletext EuroWST, CCST                              | 6.9375                 | 27H                | WST625       | always       |
| 0001                | European closed caption                             | 0.500                  | 001                | CC625        |              |
| 0010                | VPS                                                 | 5                      | 9951H              | VPS          |              |
| 0011                | wide screen signalling bits                         | 5                      | 1E3C1FH            | WSS          |              |
| 0100                | US teletext (WST)                                   | 5.7272                 | 27H                | WST525       | always       |
| 0101                | US closed caption (line 21)                         | 0.503                  | 001                | CC525        |              |
| 0110                | (video data selected)                               | 5                      | none               | disable      |              |
| 0111                | (raw data selected)                                 | 5                      | none               | disable      |              |
| 1000                | teletext                                            | 6.9375                 | programmable       | general text | optional     |
| 1001                | VITC/EBU time codes (Europe)                        | 1.8125                 | programmable       | VITC625      |              |
| 1010                | VITC/SMPTE time codes (USA)                         | 1.7898                 | programmable       | VITC525      |              |
| 1011                | reserved                                            |                        |                    |              |              |
| 1100                | US NABTS                                            | 5.7272                 | programmable       | NABTS        | optional     |
| 1101                | MOJI (Japanese)                                     | 5.7272                 | programmable (A7H) | Japtext      |              |
| 1110                | Japanese format switch (L20/22)                     | 5                      | programmable       | open         |              |
| 1111                | no sliced data transmitted<br>(video data selected) | 5                      | none               | disable      |              |

## 8.5 Image port output formatter (subaddresses 84H to 87H)

The output interface consists of a FIFO for video and for sliced text data, an arbitration circuit, which controls the mixed transfer of video and sliced text data over the I port and a decoding and multiplexing unit, which generates the 8 or 16-bit wide output data stream and the accompanied reference and supporting information.

The clock for the output interface can be derived from an internal clock, decoder, expansion port, or an externally provided clock which is appropriate for e.g. VGA and frame buffer. The clock can be up to 33 MHz. The scaler provides the following video related timing reference events (signals), which are available on pins as defined by subaddresses 84H and 85H:

- Output field ID
- Start and end of vertical active video range
- Start and end of active video line
- Data qualifier or gated clock
- Actually activated programming page (if CONLH is used)
- Threshold controlled FIFO filling flags (empty, full, filled)
- Sliced data marker.

The discontinuous data stream at the scaler output is accompanied by a data valid flag (or data qualifier), or is transported via a gated clock. Clock cycles with invalid data on the I port data bus (including the HPD pins in 16-bit output mode) are marked with code 00H.

The output interface also arbitrates the transfer between scaled video data and sliced text data over the I port output.

The bits VITX1 and VITX0 (subaddress 86H) are used to control the arbitration.

As a further operation the serialization of the internal 32-bit Dwords to 8-bit or optional 16-bit output, as well as the insertion of the extended ITU 656 codes (SAV/EAV for video data, ANC or SAV/EAV codes for sliced text data) are done here.

For handshake with the VGA controller, or other memory or bus interface circuitry, programmable FIFO flags are provided; see Section 8.5.2.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.5.1 SCALER OUTPUT FORMATTER (SUBADDRESSES 93H AND C3H)

The output formatter organizes the packing into the output FIFO. The following formats are available:

Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 2, Y-C<sub>B</sub>-C<sub>R</sub> 4 : 1 : 1, Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 0, Y-C<sub>B</sub>-C<sub>R</sub> 4 : 1 : 0 and Y only (e.g. for raw samples). The formatting is controlled by FSI[2:0] 93H[2:0], FOI[1:0] 93H[4:3] and FYSK[93H[5]].

The data formats are defined on Dwords, or multiples, and are similar to the video formats as recommended for PCI multimedia applications (compares to SAA7146A), but planar formats are not supported.

FSI[2:0] defines the horizontal packing of the data, FOI[1:0] defines how many Y only lines are expected, before a Y/C line will be formatted. If FYSK is set to logic 0 preceding Y only lines will be skipped, and the output will always start with a Y/C line.

Additionally the output formatter limits the amplitude range of the video data (controlled by ILLV[85H[5]]); see Table 18.

**Table 16** Byte stream for different output formats

| OUTPUT FORMAT                              | BYTE SEQUENCE FOR 8-BIT OUTPUT MODES |    |                  |    |                  |    |                  |    |                  |    |                  |     |                  |     |
|--------------------------------------------|--------------------------------------|----|------------------|----|------------------|----|------------------|----|------------------|----|------------------|-----|------------------|-----|
| Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 | C <sub>B</sub> 0                     | Y0 | C <sub>R</sub> 0 | Y1 | C <sub>B</sub> 2 | Y2 | C <sub>R</sub> 2 | Y3 | C <sub>B</sub> 4 | Y4 | C <sub>R</sub> 4 | Y5  | C <sub>B</sub> 6 | Y6  |
| Y-C <sub>B</sub> -C <sub>R</sub> 4 : 1 : 1 | C <sub>B</sub> 0                     | Y0 | C <sub>R</sub> 0 | Y1 | C <sub>B</sub> 4 | Y2 | C <sub>R</sub> 4 | Y3 | Y4               | Y5 | Y6               | Y7  | C <sub>B</sub> 8 | Y8  |
| Y only                                     | Y0                                   | Y1 | Y2               | Y3 | Y4               | Y5 | Y6               | Y7 | Y8               | Y9 | Y10              | Y11 | Y12              | Y13 |

**Table 17** Explanation to Table 16

| NAME             | EXPLANATION                                                                         |
|------------------|-------------------------------------------------------------------------------------|
| C <sub>B</sub> n | C <sub>B</sub> (B – Y) colour difference component, pixel number n = 0, 2, 4 to 718 |
| Yn               | Y (luminance) component, pixel number n = 0, 1, 2, 3 to 719                         |
| C <sub>R</sub> n | C <sub>R</sub> (R – Y) colour difference component, pixel number n = 0, 2, 4 to 718 |

**Table 18** Limiting range on I port

| LIMIT STEP<br>ILLV[85H[5]] | VALID RANGE   |                   | SUPPRESSED CODES (HEXADECIMAL VALUE) |             |
|----------------------------|---------------|-------------------|--------------------------------------|-------------|
|                            | DECIMAL VALUE | HEXADECIMAL VALUE | LOWER RANGE                          | UPPER RANGE |
| 0                          | 1 to 254      | 01 to FE          | 00                                   | FF          |
| 1                          | 8 to 247      | 08 to F7          | 00 to 07                             | F8 to FF    |

## 8.5.2 VIDEO FIFO (SUBADDRESS 86H)

The video FIFO at the scaler output contains 32 Dwords. That corresponds to 64 pixels in 16-bit Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 2 format. But as the entire scaler can act as a pipeline buffer, the actual available buffer capacity for the image port is much higher, and can exceed beyond a video line.

The image port, and the video FIFO, can operate with the video source clock (synchronous mode) or with an externally provided clock (asynchronous and burst mode), as appropriate for the VGA controller or attached frame buffer.

The video FIFO provides 4 internal flags, reporting to what extent the FIFO is actually filled.

These are:

- The FIFO Almost Empty (FAE) flag
- The FIFO Combined Flag (FCF) or FIFO filled, which is set at almost full level and reset, with hysteresis, only after the level crosses below the almost empty mark
- The FIFO Almost Full (FAF) flag
- The FIFO Overflow (FOVL) flag.

The trigger levels for FAE and FAF are programmable by FFL[1:0] 86H[3:2] (16, 24, 28, full) and FEL[1:0] 86H[1:0] (16, 8, 4, empty).

The state of this flag can be seen on the pins IGP0 or IGP1. The pin mapping is defined by subaddresses 84H and 85H; see Section 9.5.

## PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

### 8.5.3 TEXT FIFO

The data of the internal VBI data slicer is collected in the text FIFO before the transmission over the I port is requested (normally before the video window starts). It is partitioned into two FIFO sections. A complete line is filled into the FIFO before a data transfer is requested. So normally, one line of text data is ready for transfer, while the next text line is collected. Thus sliced text data is delivered as a block of qualified data, without any qualification gaps in the byte stream of the I port.

The decoded VBI data is collected in the dedicated VBI data FIFO. After the capture of a line has been completed, the FIFO can be streamed through the image port, preceded by a header, giving line number and standard.

The VBI data period can be signalled via the sliced data flag on pin IGP0 or IGP1. The decoded VBI data is lead by the ITU ancillary data header (DID[5:0] 5DH[5:0] at value <3EH) or by SAV/EAV codes selectable by DID[5:0] at value 3EH or 3FH. Pin IGP0 or IGP1 is set if the first byte of the ANC header is valid on the I port bus. It is reset if an SAV occurs. So it may frame multiple lines of text data output, in the event that the video processing starts with a distance of several video lines to the region of text data. Valid sliced data from the text FIFO is available on the I port as long as the IGP0 or IGP1 flag is set and the data qualifier is active on pin IDQ.

The decoded VBI data is presented in two different data formats, controlled by bit RECODE.

- RECODE = 1: values 00H and FFH will be recoded to even parity values 03H and FCH
- RECODE = 0: values 00H and FFH may occur in the data stream as detected.

### 8.5.4 VIDEO AND TEXT ARBITRATION (SUBADDRESS 86H)

Sliced text data and scaled video data are transferred over the same bus, the I port. The mixed transfer is controlled by an arbitration circuit.

If the video data is transferred without any interrupt and the video FIFO does not need to buffer any output pixel, the text data is inserted after the end of a scaled video line, normally during the blanking interval of the video.

### 8.5.5 DATA STREAM CODING AND REFERENCE SIGNAL GENERATION (SUBADDRESSES 84H, 85H AND 93H)

As H and V reference signals are logic 1, active gate signals are generated, which frame the transfer of the valid output data. As an alternative to the gates, H and V trigger pulses are generated on the rising edges of the gates.

Due to the dynamic FIFO behaviour of the complete scaler path, the output signal timing has no fixed timing relationship to the real-time input video stream. So fixed propagation delays, in terms of clock cycles, related to the analog input cannot be defined.

The data stream is accompanied by a data qualifier. Additionally invalid data cycles are marked with code 00H.

If ITU 656 like codes are not required, they can be suppressed in the output stream.

As a further option, it is possible to provide the scaler with an external gating signal on pin ITRDY. Thereby making it possible to hold the data output for a certain time and to get valid output data in bursts of a guaranteed length.

The sketched reference signals and events can be mapped to the I port output pins IDQ, IGPH, IGPV, IGP0 and IGP1. For flexible use the polarities of all the outputs can be modified. The default polarity for the qualifier and reference signals is logic 1 (active).

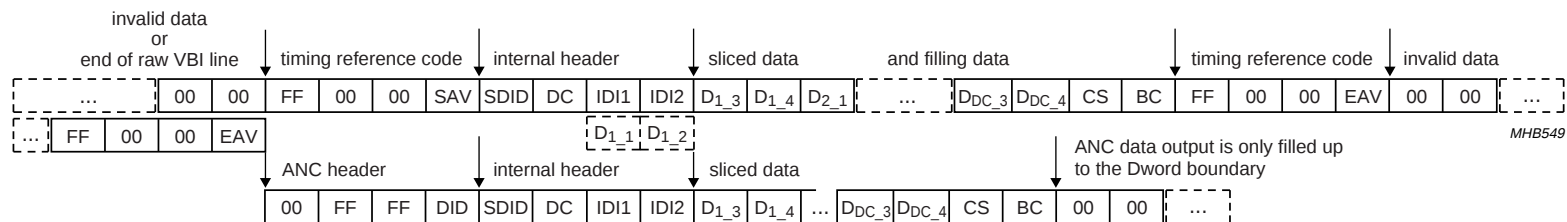
Table 19 shows the relevant and supported SAV and EAV coding.

**Table 19** SAV/EAV codes on I port

| EVENT DESCRIPTION                                                               | SAV/EAV CODES ON I PORT <sup>(1)</sup> (HEX) |              |                                        |              | COMMENT                             |
|---------------------------------------------------------------------------------|----------------------------------------------|--------------|----------------------------------------|--------------|-------------------------------------|
|                                                                                 | MSB <sup>(2)</sup> OF SAV/EAV BYTE = 0       |              | MSB <sup>(2)</sup> OF SAV/EAV BYTE = 1 |              |                                     |
|                                                                                 | FIELD ID = 0                                 | FIELD ID = 1 | FIELD ID = 0                           | FIELD ID = 1 |                                     |
| Next pixel is FIRST pixel of any active line                                    | 0E                                           | 49           | 80                                     | C7           | HREF = active;<br>VREF = active     |
| Previous pixel was LAST pixel of any active line, but not the last              | 13                                           | 54           | 9D                                     | DA           | HREF = inactive;<br>VREF = active   |
| Next pixel is FIRST pixel of any V-blanking line                                | 25                                           | 62           | AB                                     | EC           | HREF = active;<br>VREF = inactive   |
| Previous pixel was LAST pixel of the last active line or of any V-blanking line | 38                                           | 7F           | B6                                     | F1           | HREF = inactive;<br>VREF = inactive |
| No valid data, don't capture and don't increment pointer                        | 00                                           |              |                                        |              | IDQ pin inactive                    |

**Notes**

- The leading byte sequence is: FFH-00H-00H.
- The MSB of the SAV/EAV code byte is controlled by:
  - Scaler output data: task A  $\Rightarrow$  MSB =  $\overline{\text{CONLH}}[90\text{H}[7]]$ ; task B  $\Rightarrow$  MSB =  $\overline{\text{CONLH}}[C0\text{H}[7]]$ .
  - VBI data slicer output data: DID[5:0] 5DH[5:0] = 3EH  $\Rightarrow$  MSB = 1; DID[5:0] 5DH[5:0] = 3FH  $\Rightarrow$  MSB = 0.



ANC header active for DID (subaddress 5DH) < 3EH

Fig.31 Sliced data formats on the I port in 8-bit mode.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 20** Explanation to Fig.31

| NAME              | EXPLANATION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SAV               | start of active data; see Table 21                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| SDID              | sliced data identification: NEP <sup>(1)</sup> , EP <sup>(2)</sup> , SDID5 to SDID0, freely programmable via I <sup>2</sup> C-bus subaddress 5EH, D5 to D0, e. g. to be used as source identifier                                                                                                                                                                                                                                                                                                                                                                    |
| DC                | Dword count: NEP <sup>(1)</sup> , EP <sup>(2)</sup> , DC5 to DC0. DC describes the number of succeeding 32-bit words: <ul style="list-style-type: none"> <li>For SAV/EAV mode DC is fixed to 11 Dwords (byte value 4BH)</li> <li>For ANC mode it is: <math>DC = \frac{1}{4}(C + n)</math>, where <math>C = 2</math> (the two data identification bytes IDI1 and IDI2) and <math>n</math> = number of decoded bytes according to the chosen text standard.</li> </ul> It should be noted that the number of valid bytes inside the stream can be seen in the BC byte. |
| IDI1              | internal data identification 1: OP <sup>(3)</sup> , FID (field 1 = 0, field 2 = 1), LineNumber8 to LineNumber3 = Dword 1 byte 1; see Table 21                                                                                                                                                                                                                                                                                                                                                                                                                        |
| IDI2              | internal data identification 2: OP <sup>(3)</sup> , LineNumber2 to LineNumber0, DataType3 to DataType0 = Dword 1 byte 2; see Table 21                                                                                                                                                                                                                                                                                                                                                                                                                                |
| D <sub>n_m</sub>  | Dword number <b>n</b> , byte number <b>m</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| D <sub>DC_4</sub> | last Dword byte 4, note: for SAV/EAV framing DC is fixed to 0BH, missing data bytes are filled up; the fill value is A0H                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CS                | the check sum byte, the check sum is accumulated from the SAV (respectively DID) byte to the D <sub>DC_4</sub> byte                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| BC                | number of valid sliced bytes counted from the IDI1 byte                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| EAV               | end of active data; see Table 21                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Notes**

1. Inverted EP (bit D7); for EP see note 2.
2. Even parity (bit D6) of bits D5 to D0.
3. Odd parity (bit D7) of bits D6 to D0.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 21** Bytes stream of the data slicer

| NICK NAME           | COMMENT                            | D7                      | D6                  | D5                  | D4                  | D3                  | D2                  | D1                  | D0                  |
|---------------------|------------------------------------|-------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| DID,<br>SAV,<br>EAV | subaddress 5DH = 00H               | NEP <sup>(1)</sup>      | EP <sup>(2)</sup>   | 0                   | 1                   | 0                   | FID <sup>(3)</sup>  | I1 <sup>(4)</sup>   | I0 <sup>(4)</sup>   |
|                     | subaddress 5DH;<br>D5 = 1          | NEP <sup>(1)</sup>      | EP <sup>(2)</sup>   | 0                   | D4[5DH]             | D3[5DH]             | D2[5DH]             | D1[5DH]             | D0[5DH]             |
|                     | subaddress 5DH<br>D5 = 3EH; note 5 | 1                       | FID <sup>(3)</sup>  | V <sup>(6)</sup>    | H <sup>(7)</sup>    | P3                  | P2                  | P1                  | P0                  |
|                     | subaddress 5DH<br>D5 = 3FH; note 5 | 0                       | FID <sup>(3)</sup>  | V <sup>(6)</sup>    | H <sup>(7)</sup>    | P3                  | P2                  | P1                  | P0                  |
| SDID                | programmable via<br>subaddress 5EH | NEP <sup>(1)</sup>      | EP <sup>(2)</sup>   | D5[5EH]             | D4[5EH]             | D3[5EH]             | D2[5EH]             | D1[5EH]             | D0[5EH]             |
| DC <sup>(8)</sup>   |                                    | NEP <sup>(1)</sup>      | EP <sup>(2)</sup>   | DC5                 | DC4                 | DC3                 | DC2                 | DC1                 | DC0                 |
| IDI1                |                                    | OP <sup>(9)</sup>       | FID <sup>(3)</sup>  | LN8 <sup>(10)</sup> | LN7 <sup>(10)</sup> | LN6 <sup>(10)</sup> | LN5 <sup>(10)</sup> | LN4 <sup>(10)</sup> | LN3 <sup>(10)</sup> |
| IDI2                |                                    | OP <sup>(9)</sup>       | LN2 <sup>(10)</sup> | LN1 <sup>(10)</sup> | LN0 <sup>(10)</sup> | DT3 <sup>(11)</sup> | DT2 <sup>(11)</sup> | DT1 <sup>(11)</sup> | DT0 <sup>(11)</sup> |
| CS                  | check sum byte                     | $\overline{\text{CS6}}$ | CS6                 | CS5                 | CS4                 | CS3                 | CS2                 | CS1                 | CS0                 |
| BC                  | valid byte count                   | OP <sup>(9)</sup>       | 0                   | CNT5                | CNT4                | CNT3                | CNT2                | CNT1                | CNT0                |

**Notes**

1. NEP = inverted EP (see note 2).
2. EP = Even Parity of bits D5 to D0.
3. FID = 0: field 1; FID = 1: field 2.
4. I1 = 0 and I0 = 0: before line 1; I1 = 0 and I0 = 1: lines 1 to 23; I1 = 1 and I0 = 0: after line 23; I1 = 1 and I0 = 1: line 24 to end of field.
5. Subaddress 5DH at 3EH and 3FH are used for ITU 656 like SAV/EAV header generation; recommended value.
6. V = 0: active video; V = 1: blanking.
7. H = 0: start of line; H = 1: end of line.
8. DC = Data Count in Dwords according to the data type.
9. OP = Odd Parity of bits D6 to D0.
10. LN = Line Number.
11. DT = Data Type according to table.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.6 Audio clock generation (subaddresses 30H to 3FH)

The SAA7114 incorporates the generation of a field-locked audio clock as an auxiliary function for video capture. An audio sample clock, that is locked to the field frequency, ensures that there is always the same predefined number of audio samples associated with a field, or a set of fields. This ensures synchronous playback of audio and video after digital recording (e.g. capture to hard disk), MPEG or other compression, or non-linear editing.

**Remark:** For standard applications the synthesized audio clock AMCLK can be used directly as master clock and as input clock for port AMXCLK (short cut) to generate ASCLK and ALRCLK. For high-end applications it is recommended to use an external analog PLL circuit to enhance the performance of the generated audio clock.

### 8.6.1 MASTER AUDIO CLOCK

The audio clock is synthesized from the same crystal frequency as the line-locked video clock is generated. The master audio clock is defined by the parameters:

- Audio master Clocks Per Field, ACPF[17:0] 32H[1:0] 31H[7:0] 30H[7:0] according to the equation:

$$ACPF[17:0] = \text{round}\left(\frac{\text{audio frequency}}{\text{field frequency}}\right)$$

- Audio master Clocks Nominal Increment, ACNI[21:0] 36H[5:0] 35H[7:0] 34H[7:0] according to the equation:

$$ACNI[21:0] = \text{round}\left(\frac{\text{audio frequency}}{\text{crystal frequency}} \times 2^{23}\right)$$

See Table 22 for examples.

**Table 22** Programming examples for audio master clock generation

| XTALO<br>(MHz)                       | FIELD<br>(Hz) | ACPF    |       | ACNI    |         |
|--------------------------------------|---------------|---------|-------|---------|---------|
|                                      |               | DECIMAL | HEX   | DECIMAL | HEX     |
| AMCLK = 256 × 48 kHz (12.288 MHz)    |               |         |       |         |         |
| 32.11                                | 50            | 245760  | 3C000 | 3210190 | 30FBCE  |
|                                      | 59.94         | 205005  | 320CD | 3210190 | 30FBCE  |
| 24.576                               | 50            | —       | —     | —       | —       |
|                                      | 59.94         | —       | —     | —       | —       |
| AMCLK = 256 × 44.1 kHz (11.2896 MHz) |               |         |       |         |         |
| 32.11                                | 50            | 225792  | 37200 | 2949362 | 2D00F2  |
|                                      | 59.94         | 188348  | 2DFBC | 2949362 | 2D00F2  |
| 24.576                               | 50            | 225792  | 37200 | 3853517 | 3ACCCD  |
|                                      | 59.94         | 188348  | 2DFBC | 3853517 | 3ACCCD  |
| AMCLK = 256 × 32 kHz (8.192 MHz)     |               |         |       |         |         |
| 32.11                                | 50            | 163840  | 28000 | 2140127 | 20A7DF  |
|                                      | 59.94         | 136670  | 215DE | 2140127 | 20A7DF  |
| 24.576                               | 50            | 163840  | 28000 | 2796203 | 2AAAAAB |
|                                      | 59.94         | 136670  | 215DE | 2796203 | 2AAAAAB |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 8.6.2 SIGNALS ASCLK AND ALRCLK

Two binary divided signals ASCLK and ALRCLK are provided for slower serial digital audio signal transmission and for channel-select. The frequencies of these signals are defined by the following parameters:

- SDIV[5:0] 38H[5:0] according to the equation:

$$f_{ASCLK} = \frac{f_{AMXCLK}}{(SDIV + 1) \times 2} \Rightarrow SDIV[5:0] = \frac{f_{AMXCLK}}{2f_{ASCLK}} - 1$$

- LRDIV[5:0] 39H[5:0] according to the equation:  $f_{ALRCLK} = \frac{f_{ASCLK}}{LRDIV \times 2} \Rightarrow LRDIV[5:0] = \frac{f_{ASCLK}}{2f_{ALRCLK}}$

See Table 23 for examples.

**Table 23** Programming examples for ASCLK/ALRCLK clock generation

| AMXCLK<br>(MHz) | ASCLK<br>(kHz) | SDIV    |     | ALRCLK<br>(kHz) | LRDIV   |     |
|-----------------|----------------|---------|-----|-----------------|---------|-----|
|                 |                | DECIMAL | HEX |                 | DECIMAL | HEX |
| 12.288          | 1536           | 3       | 03  | 48              | 16      | 10  |
|                 | 768            | 7       | 07  |                 | 8       | 08  |
| 11.2896         | 1411.2         | 3       | 03  | 44.1            | 16      | 10  |
|                 | 2822.4         | 1       | 01  |                 | 32      | 10  |
| 8.192           | 1024           | 3       | 03  | 32              | 16      | 10  |
|                 | 2048           | 1       | 01  |                 | 32      | 10  |

## 8.6.3 OTHER CONTROL SIGNALS

Further control signals are available to define reference clock edges and vertical references; see Table 24.

**Table 24** Control signals for reference clock edges and vertical references

| SIGNAL       | DESCRIPTION                                                                                                                                                  |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| APLL[3AH[3]] | Audio PLL mode<br>0 = PLL closed<br>1 = PLL open                                                                                                             |
| AMVR[3AH[2]] | Audio Master clock Vertical Reference<br>0 = internal V<br>1 = external V                                                                                    |
| LRPH[3AH[1]] | ALRCLK phase<br>0 = invert ASCLK, ALRCLK edges triggered by falling edge of ASCLK<br>1 = don't invert ASCLK, ALRCLK edges triggered by rising edge of ASCLK  |
| SCPH[3AH[0]] | ASCLK phase<br>0 = invert AMXCLK, ASCLK edges triggered by falling edge of AMXCLK<br>1 = don't invert AMXCLK, ASCLK edges triggered by rising edge of AMXCLK |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 9 INPUT/OUTPUT INTERFACES AND PORTS

The SAA7114 has 5 different I/O interfaces:

- Analog video input interface, for analog CVBS and/or Y and C input signals
- Audio clock port
- Digital real-time signal port (RT port)
- Digital video expansion port (X port), for unscaled digital video input and output
- Digital image port (I port) for scaled video data output and programming
- Digital host port (H port) for extension of the image port or expansion port from 8 to 16-bit.

### 9.1 Analog terminals

The SAA7114 has 6 analog inputs AI21 to AI24, AI11 and AI12 for composite video CVBS or S-video Y/C signal pairs. Additionally, there are two differential reference inputs, which must be connected to ground via a capacitor equivalent to the decoupling capacitors at the 6 inputs. There are no peripheral components required other than these decoupling capacitors and 18  $\Omega$ /56  $\Omega$  termination resistors, one set per connected input signal; see application example in Fig.41. Two anti-alias filters are integrated, and self adjusting via the clock frequency.

Clamp and gain control for the two ADCs are also integrated. An analog video output (pin AOUT) is provided for testing purposes.

**Table 25** Analog pin description

| SYMBOL        | PIN <sup>(1)</sup>                     | I/O | DESCRIPTION                                                                                       | BIT             |
|---------------|----------------------------------------|-----|---------------------------------------------------------------------------------------------------|-----------------|
| AI24 to AI21  | P6, P7, P9 and P10 (10, 12, 14 and 16) | I   | analog video signal inputs, e.g. 2 CVBS signals and two Y/C pairs can be connected simultaneously | MODE3 to MODE0  |
| AI12 and AI11 | P11 and P13 (18 and 20)                |     |                                                                                                   |                 |
| AOUT          | M10 (22)                               | O   | analog video output, for test purposes                                                            | AOSL1 and AOSL0 |
| AI1D and AI2D | P12 and P8 (19 and 13)                 | I   | analog reference pins for differential ADC operation                                              | –               |

### Note

1. Pin numbers for LQFP100 in parenthesis.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 9.2 Audio clock signals

The SAA7114 also synchronizes the audio clock and sampling rate to the video frame rate, via a very slow PLL. This ensures that the multimedia capture and compression processes always gather the same predefined number of samples per video frame.

An audio master clock AMCLK and two divided clocks ASCLK and ALRCLK are generated:

- ASCLK: can be used as audio serial clock
- ALRCLK: audio left/right channel clock.

The ratios are programmable; see Section 8.6.

**Table 26** Audio clock pin description

| SYMBOL | PIN <sup>(1)</sup> | I/O | DESCRIPTION                                                                                                                           | BIT                                                                             |
|--------|--------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| AMCLK  | K12 (37)           | O   | audio master clock output                                                                                                             | ACPF[17:0] 32H[1:0] 31H[7:0] 30H[7:0] and ACNI[21:0] 36H[5:0] 35H[7:0] 34H[7:0] |
| AMXCLK | J12 (41)           | I   | external audio master clock input for the clock division circuit, can be directly connected to output AMCLK for standard applications | –                                                                               |
| ASCLK  | K14 (39)           | O   | serial audio clock output, can be synchronized to rising or falling edge of AMXCLK                                                    | SDIV[5:0] 38H[5:0] and SCPH[3AH[0]]                                             |
| ALRCLK | J13 (40)           | O   | audio channel (left/right) clock output, can be synchronized to rising or falling edge of ASCLK                                       | LRDIV[5:0] 39H[5:0] and LRPH[3AH[1]]                                            |

### Note

1. Pin numbers for LQFP100 in parenthesis.

## 9.3 Clock and real-time synchronization signals

For the generation of the line-locked video (pixel) clock LLC, and of the frame-locked audio serial bit clock, a crystal accurate frequency reference is required. An oscillator is built-in for fundamental or third harmonic crystals. The supported crystal frequencies are 32.11 or 24.576 MHz (defined during reset by strapping pin ALRCLK).

Alternatively pin XTALI can be driven from an external single-ended oscillator.

The crystal oscillation can be propagated as a clock to other ICs in the system via pin XTOUT.

The Line-Locked Clock (LLC) is the double pixel clock of nominal 27 MHz. It is locked to the selected video input, generating baseband video pixels according to *ITU recommendation 601*. In order to support interfacing circuits, a direct pixel clock (LLC2) is also provided.

The pins for line and field timing reference signals are RTCO, RTS1 and RTS0. Various real-time status information can be selected for the RTS pins. The signals are always available (output) and reflect the synchronization operation of the decoder part in the SAA7114. The function of the RTS1 and RTS0 pins can be defined by bits RTSE1[3:0] 12H[7:4] and RTSE0[3:0] 12H[3:0].

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 27** Clock and real-time synchronization signals

| SYMBOL                             | PIN <sup>(1)</sup> | I/O | DESCRIPTION                                                                                                                                                          | BIT                 |
|------------------------------------|--------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| <b>Crystal oscillator</b>          |                    |     |                                                                                                                                                                      |                     |
| XTALI                              | P2<br>(7)          | I   | input for crystal oscillator or reference clock                                                                                                                      | –                   |
| XTALO                              | P3<br>(6)          | O   | output of crystal oscillator                                                                                                                                         | –                   |
| XTOUT                              | P4<br>(4)          | O   | reference (crystal) clock output drive (optional)                                                                                                                    | XTOUTE[14H[3]]      |
| <b>Real-time signals (RT port)</b> |                    |     |                                                                                                                                                                      |                     |
| LLC                                | M14<br>(28)        | O   | line-locked clock, nominal 27 MHz, double pixel clock locked to the selected video input signal                                                                      | –                   |
| LLC2                               | L14<br>(29)        | O   | line-locked pixel clock, nominal 13.5 MHz                                                                                                                            | –                   |
| RTCO                               | L13<br>(36)        | O   | real-time control output, transfers real-time status information supporting RTC level 3.1 (see document “ <i>RTC Functional Description</i> ”, available on request) | –                   |
| RTS0                               | K13<br>(34)        | O   | real-time status information line 0, can be programmed to carry various real-time information; see Table 57                                                          | RTSE0[3:0] 12H[3:0] |
| RTS1                               | L10<br>(35)        | O   | real-time status information line 1, can be programmed to carry various real-time information; see Table 58                                                          | RTSE1[3:0] 12H[7:4] |

**Note**

- Pin numbers for LQFP100 in parenthesis.

**9.4 Video expansion port (X port)**

The expansion port is intended for transporting video streams image data from other digital video circuits such as MPEG encoder/decoder and video phone codec, to the image port (I port).

The expansion port consists of two groups of signals/pins:

- 8-bit data, I/O, regularly components video  $Y-C_B-C_R$  4 : 2 : 2, i.e.  $C_B-Y-C_R-Y$ , byte serial, exceptionally raw video samples (e.g. ADC test). In input mode the data bus can be extended to 16-bit by pins HPD7 to HPD0.
- Clock, synchronization and auxiliary signals, accompanying the data stream, I/O.

As output, these are direct copies of the decoder signals.

The data transfers through the expansion port represent a single D1 port, with half duplex mode. The SAV and EAV codes may be inserted optionally for data input (controlled by bit XCODE[92H[3]]). The input/output direction is switched for complete fields only.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 28** Signals dedicated to the expansion port

| SYMBOL       | PIN <sup>(1)</sup>                                            | I/O | DESCRIPTION                                                                                                                                                                                                                                    | BIT                                                                |
|--------------|---------------------------------------------------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|
| XPD7 to XPD0 | K2, K3, L1 to L3, M1, M2 and N1 (81, 82, 84 to 87, 89 and 90) | I/O | X port data: in output mode controlled by decoder section, data format see Table 29; in input mode Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 serial input data or luminance part of a 16-bit Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 input | OFTS[2:0]<br>13H[2:0],<br>91H[7:0] and<br>C1H[7:0]                 |
| XCLK         | M3 (94)                                                       | I/O | clock at expansion port: if output, then copy of LLC; as input normally a double pixel clock of up to 32 MHz or a gated clock (clock gated with a qualifier)                                                                                   | XCKS[92H[0]]                                                       |
| XDQ          | M4 (95)                                                       | I/O | data valid flag of the expansion port input (qualifier): if output, then decoder (HREF and VGATE) gate (see Fig.24)                                                                                                                            | —                                                                  |
| XRDY         | N3 (96)                                                       | O   | data request flag = ready to receive, to work with optional buffer in external device, to prevent internal buffer overflow;<br>second function: input related task flag A/B                                                                    | XRQT[83H[2]]                                                       |
| XRH          | N2 (92)                                                       | I/O | horizontal reference signal for the X port:<br>as output: HREF or HS from the decoder (see Fig.24);<br>as input: a reference edge for horizontal input timing and a polarity for input field ID detection can be defined                       | XRHS[13H[6]],<br>XFDH[92H[6]]<br>and<br>XDH[92H[2]]                |
| XRV          | L5 (91)                                                       | I/O | vertical reference signal for the X port:<br>as output: V123 or field ID from the decoder, see Figs 22 and 23;<br>as input: a reference edge for vertical input timing and for input field ID detection can be defined                         | XRVS[1:0]<br>13H[5:4],<br>XFDV[92H[7]]<br>and XDV[1:0]<br>92H[5:4] |
| XTRI         | K1 (80)                                                       | I   | port control: switches X port input 3-state                                                                                                                                                                                                    | XPE[1:0]<br>83H[1:0]                                               |

**Note**

1. Pin numbers for LQFP100 in parenthesis.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 9.4.1 X PORT CONFIGURED AS OUTPUT

If data output is enabled at the expansion port, then the data stream from the decoder is presented. The data format of the 8-bit data bus is dependent on the chosen data type, selectable by the line control registers LCR2 to LCR24; see Table 4. In contrast to the image port, the sliced data format is not available on the expansion port. Instead, raw CVBS samples are always transferred if any sliced data type is selected.

Some details of data types on the expansion port are as follows:

- **Active video** (data type 15): contains component  $Y-C_B-C_R$  4 : 2 : 2 signal, 720 active pixels per line. The amplitude and offsets are programmable via DBRI7 to DBRI0, DCON7 to DCON0, DSAT7 to DSAT0, OFFU1, OFFU0, OFFV1 and OFFV0. The nominal levels are illustrated in Fig.18.
- **Test line** (data type 6): is similar to the active video format, with some constraints within the data processing:
  - adaptive chrominance comb filter, vertical filter (chrominance comb filter for NTSC standards, PAL phase error correction) within the chrominance processing are disabled
  - adaptive luminance comb filter, peaking and chrominance trap are bypassed within the luminance processing.

This data type is defined for future enhancements. It could be activated for lines containing standard test signals within the vertical blanking period. Currently the most sources do not contain test lines. The nominal levels are illustrated in Fig.18.

- **Raw samples** (data types 0 to 5 and 7 to 14):  $C_B-C_R$  samples are similar to data type 6, but CVBS samples are transferred instead of processed luminance samples within the Y time slots.

The amplitude and offset of the CVBS signal is programmable via RAWG7 to RAWG0 and RAWO7 to RAWO0; see Chapter 15, Tables 64 and 65. The nominal levels are illustrated in Fig.19.

The relationship of LCR programming to line numbers is described in Section 8.2, Tables 5 to 8.

The data type selections by LCR are overruled by setting OFTS2 = 1 (subaddress 13H bit D2). This setting is mainly intended for device production test. The VPO-bus carries the upper or lower 8 bits of the two ADCs depending on the OFTS[1:0] 13H[1:0] settings; see Table 59. The input configuration is done via MODE[3:0] 02H[3:0] settings; see Table 41. If a Y/C mode is selected, the expansion port carries the multiplexed output signals of both ADCs, and in CVBS mode the output of only one ADC. No timing reference codes are generated in this mode.

**Remark:** The LSBs (bit D0) of the ADCs are also available on pin RTS0; see Table 57.

The SAV/EAV timing reference codes define the start and end of valid data regions. The ITU-blanking code sequence '- 80 - 10 - 80 - 10 - ...' is transmitted during the horizontal blanking period between EAV and SAV.

The position of the F-bit is constant in accordance with ITU 656; see Tables 31 and 32.

The V-bit can be generated in two different ways (see Tables 31 and 32) controlled via OFTS1 and OFTS0; see Table 59.

The F and V bits change synchronously with the EAV code.

**Table 29** Data format on the expansion port

| BLANKING PERIOD |    |    | TIMING REFERENCE CODE (HEX) <sup>(1)</sup> |    |    |     | 720 PIXELS Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 DATA <sup>(2)</sup> |    |                  |    |                  |    |     |                    |      |    | TIMING REFERENCE CODE (HEX) <sup>(1)</sup> |    |     |    | BLANKING PERIOD |     |  |
|-----------------|----|----|--------------------------------------------|----|----|-----|---------------------------------------------------------------------------|----|------------------|----|------------------|----|-----|--------------------|------|----|--------------------------------------------|----|-----|----|-----------------|-----|--|
| ...             | 80 | 10 | FF                                         | 00 | 00 | SAV | C <sub>B</sub> 0                                                          | Y0 | C <sub>R</sub> 0 | Y1 | C <sub>B</sub> 2 | Y2 | ... | C <sub>R</sub> 718 | Y719 | FF | 00                                         | 00 | EAV | 80 | 10              | ... |  |

### Notes

1. The generation of the timing reference codes can be suppressed by setting OFTS[2:0] to 010; see Table 59. In this event the code sequence is replaced by the standard '- 80 - 10 -' blanking values.
2. If raw samples or sliced data are selected by the line control registers (LCR2 to LCR24), the Y samples are replaced by CVBS samples.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 30** SAV/EAV format on expansion port XPD7 to XPD0

| BIT D7 | BIT D6<br>(F)                                     | BIT D5<br>(V)                                              | BIT D4<br>(H)                                        | BIT D3<br>(P3)                                                                    | BIT D2<br>(P2) | BIT D1<br>(P1) | BIT D0<br>(P0) |
|--------|---------------------------------------------------|------------------------------------------------------------|------------------------------------------------------|-----------------------------------------------------------------------------------|----------------|----------------|----------------|
| 1      | field bit<br>1st field: F = 0<br>2nd field: F = 1 | vertical blanking bit<br>VBI: V = 1<br>active video: V = 0 | format<br>H = 0 in SAV format<br>H = 1 in EAV format | reserved; evaluation not<br>recommended (protection bits<br>according to ITU 656) |                |                |                |
|        | for vertical timing see Tables 31 and 32          |                                                            |                                                      |                                                                                   |                |                |                |

**Table 31** 525 lines/60 Hz vertical timing

| LINE NUMBER | F (ITU 656) | V                         |                                                                                                                        |
|-------------|-------------|---------------------------|------------------------------------------------------------------------------------------------------------------------|
|             |             | OFTS[2:0] = 000 (ITU 656) | OFTS[2:0] = 001                                                                                                        |
| 1 to 3      | 1           | 1                         | according to selected VGATE<br>position type via VSTA and<br>VSTO<br>(subaddresses 15H to 17H);<br>see Tables 61 to 63 |
| 4 to 19     | 0           | 1                         |                                                                                                                        |
| 20          | 0           | 0                         |                                                                                                                        |
| 21          | 0           | 0                         |                                                                                                                        |
| 22 to 261   | 0           | 0                         |                                                                                                                        |
| 262         | 0           | 0                         |                                                                                                                        |
| 263         | 0           | 0                         |                                                                                                                        |
| 264 and 265 | 0           | 1                         |                                                                                                                        |
| 266 to 282  | 1           | 1                         |                                                                                                                        |
| 283         | 1           | 0                         |                                                                                                                        |
| 284         | 1           | 0                         |                                                                                                                        |
| 285 to 524  | 1           | 0                         |                                                                                                                        |
| 525         | 1           | 0                         |                                                                                                                        |

**Table 32** 625 lines/50 Hz vertical timing

| LINE NUMBER | F (ITU 656) | V                         |                                                                                                                        |
|-------------|-------------|---------------------------|------------------------------------------------------------------------------------------------------------------------|
|             |             | OFTS[2:0] = 000 (ITU 656) | OFTS[1:0] = 10                                                                                                         |
| 1 to 22     | 0           | 1                         | according to selected VGATE<br>position type via VSTA and<br>VSTO<br>(subaddresses 15H to 17H);<br>see Tables 61 to 63 |
| 23          | 0           | 0                         |                                                                                                                        |
| 24 to 309   | 0           | 0                         |                                                                                                                        |
| 310         | 0           | 0                         |                                                                                                                        |
| 311 and 312 | 0           | 1                         |                                                                                                                        |
| 313 to 335  | 1           | 1                         |                                                                                                                        |
| 336         | 1           | 0                         |                                                                                                                        |
| 337 to 622  | 1           | 0                         |                                                                                                                        |
| 623         | 1           | 0                         |                                                                                                                        |
| 624 and 625 | 1           | 1                         |                                                                                                                        |

## PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

### 9.4.2 X PORT CONFIGURED AS INPUT

If the data input mode is selected at the expansion port, then the scaler can select its input data stream from the on-chip video decoder, or from the expansion port (controlled by bit SCSRC[1:0] 91H[5:4]). Byte serial Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 2, or subsets for other sampling schemes, or raw samples from an external ADC may be input (see also bits FSC[2:0] 91H[2:0]). The input stream must be accompanied by an external clock (XCLK), qualifier XDQ and reference signals XRH and XRV. Instead of the reference signal, embedded SAV and EAV codes according to ITU 656 are also accepted. The protection bits are not evaluated.

XRH and XRV carry the horizontal and vertical synchronization signals for the digital video stream through the expansion port. The field ID of the input video stream is carried in the phase (edge) of XRV and state of XRH, or directly as FS (frame sync, odd/even signal) on the XRV pin (controlled by XFDV[92H[7]], XFDH[92H[6]] and XDV[1:0] 92H[5:4]).

The trigger events on XRH (rising/falling edge) and XRV (rising/falling/both edges) for the scalers acquisition window are defined by XDV[1:0] 92H[5:4] and XDH[92H[2]]. The signal polarity of the qualifier can also be defined (bit XDQ[92H[1]]). Alternatively to a qualifier, the input clock can be applied to a gated clock (clock gated with a data qualifier, controlled by bit XCKS[92H[0]]). In this event, all input data will be qualified.

### 9.5 Image port (I port)

The image port transfers data from the scaler as well as from the VBI data slicer, if selected (maximum 33 MHz). The reference clock is available at the ICLK pin, as an output, or as an input (maximum 33 MHz). As output, ICLK is derived from the line-locked decoder or expansion port input clock. The data stream from the scaler output is normally discontinuous. Therefore valid data during a clock cycle is accompanied by a data qualifying (data valid) flag on pin IDQ. For pin constrained applications the IDQ pin can be programmed to function as a gated clock output (bit ICKS2[80H[2]]).

The data formats at the image port are defined in Dwords of 32 bits (4 bytes), such as the related FIFO structures. However the physical data stream at the image port is only 16-bit or 8-bit wide; in 16-bit mode data pins HPD7 to HPD0 are used for chrominance data. The four bytes of the Dwords are serialized in words or bytes.

Available formats are as follows:

- Y-C<sub>B</sub>-C<sub>R</sub> 4 : 2 : 2
- Y-C<sub>B</sub>-C<sub>R</sub> 4 : 1 : 1
- Raw samples
- Decoded VBI data.

For handshake with the receiving VGA controller, or other memory or bus interface circuitry, F, H and V reference signals and programmable FIFO flags are provided. The information is provided on pins IGP0, IGP1, IGPH and IGPV. The functionality on these pins is controlled via subaddresses 84H and 85H.

VBI data is collected over an entire line in its own FIFO, and transferred as an uninterrupted block of bytes. Decoded VBI data can be signed by the VBI flag on pin IGP0 or IGP1.

As scaled video data and decoded VBI data may come from different and asynchronous sources, an arbitration scheme is needed. Normally the VBI data slicer has priority.

The image port consists of the pins and/or signals, as listed in Table 33.

For pin constrained applications, or interfaces, the relevant timing and data reference signals can also get encoded into the data stream. Therefore the corresponding pins do not need to be connected. The minimum image port configuration requires 9 pins only, i.e. 8 pins for data including codes, and 1 pin for clock or gated clock. The inserted codes are defined in close relationship to the ITU-R BT.656 (D1) recommendation, where possible.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

The following deviations from “ITU 656 recommendation” are implemented at the SAA7114 image port interface:

- SAV and EAV codes are only present in those lines, where data is to be transferred, i.e. active video lines, or VBI raw samples, no codes for empty lines
- There may be more or less than 720 pixels between SAV and EAV
- Data content and the number of clock cycles during horizontal and vertical blanking is undefined, and may not be constant
- Data stream may be interleaved with not-valid data codes, 00H, but SAV and EAV 4-byte codes are not interleaved with not-valid data codes
- There may be an irregular pattern of not-valid data, or IDQ, and as a result,  $C_B$ -Y- $C_R$ -Y is not in a fixed phase to a regular clock divider
- VBI raw sample streams are enveloped with SAV and EAV, like normal video
- Decoded VBI data is transported as Ancillary (ANC) data, two modes:
  - direct decoded VBI data bytes (8-bit) are directly placed in the ANC data field, 00H and FFH codes may appear in data block (violation to ITU-R BT.656)
  - recoded VBI data bytes (8-bit) directly placed in ANC data field, 00H and FFH codes will be recoded to even parity codes 03H and FCH to suppress invalid ITU-R BT.656 codes.

There are no empty cycles in the ancillary code and its data field. The data codes 00H and FFH are suppressed (changed to 01H or FEH respectively) in the active video stream, as well as in the VBI raw sample stream (VBI pass-through). Optionally, the number range can be further limited.

**Table 33** Signals dedicated to the image port

| SYMBOL       | PIN <sup>(1)</sup>                                                | I/O | DESCRIPTION                                                                                                                                 | BIT                                                                   |
|--------------|-------------------------------------------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------|
| IPD7 to IPD0 | E14, D14, C14, B14, E13, D13, C13 and B13 (54 to 57 and 59 to 62) | I/O | I port data                                                                                                                                 | ICODE[93H[7]], ISWP[1:0] 85H[7:6] and IPE[1:0] 87H[1:0]               |
| ICLK         | H12 (45)                                                          | I/O | continuous reference clock at image port, can be input or output, as output decoder LLC or XCLK from X port                                 | ICKS[1:0] 80H[1:0] and IPE[1:0] 87H[1:0]                              |
| IDQ          | H14 (46)                                                          | O   | data valid flag at image port, qualifier, with programmable polarity; secondary function: gated clock                                       | ICKS2[80H[2]], IDQP[85H[0]] and IPE[1:0] 87H[1:0]                     |
| IGPH         | G12 (53)                                                          | O   | horizontal reference output signal, copy of the H gate signal of the scaler, with programmable polarity; alternative function: HRESET pulse | IDH[1:0] 84H[1:0], IRHP[85H[1]] and IPE[1:0] 87H[1:0]                 |
| IGPV         | F13 (52)                                                          | O   | vertical reference output signal, copy of the V gate signal of the scaler, with programmable polarity; alternative function: VRESET pulse   | IDV[1:0] 84H[3:2], IRVP[85H[2]] and IPE[1:0] 87H[1:0]                 |
| IGP1         | G13 (49)                                                          | O   | general purpose output signal for I port                                                                                                    | IDG12[86H[4]], IDG1[1:0] 84H[5:4], IG1P[85H[3]] and IPE[1:0] 87H[1:0] |
| IGP0         | F14 (48)                                                          | O   | general purpose output signal for I port                                                                                                    | IDG02[86H[5]], IDG0[1:0] 84H[7:6], IG0P[85H[4]] and IPE[1:0] 87H[1:0] |
| ITRDY        | J14 (42)                                                          | I   | target ready input signals                                                                                                                  | –                                                                     |
| ITRI         | G14 (47)                                                          | I   | port control, switches I port into 3-state                                                                                                  | IPE[1:0] 87H[1:0]                                                     |

## Note

1. Pin numbers for LQFP100 in parenthesis.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

9.6 Host port for 16-bit extension of video data I/O (H port)

The H port pins HPD can be used for extension of the data I/O paths to 16-bit.

The I port has functional priority. If I8\_16[93H[6]] is set to logic 1 the output drivers of the H port are enabled depending on the I port enable control. For I8\_16 = 0, the HPD output is disabled.

Table 34 Signals dedicated to the host port

| SYMBOL       | PIN <sup>(1)</sup>                                                   | I/O | DESCRIPTION                                              | BIT                                               |
|--------------|----------------------------------------------------------------------|-----|----------------------------------------------------------|---------------------------------------------------|
| HPD7 to HPD0 | A13, D12, C12, B12, A12, C11, B11 and A11<br>(64 to 67 and 69 to 72) | I/O | 16-bit extension for digital I/O (chrominance component) | IPE[1:0] 87H[1:0], ITRI[8FH[6]] and I8_16[93H[6]] |

Note

1. Pin numbers for LQFP100 in parenthesis.

9.7 Basic input and output timing diagrams I port and X port

9.7.1 I PORT OUTPUT TIMING

The following diagrams illustrate the output timing via the I port. IGPH and IGPV are logic 1 active gate signals. If reference pulses are programmed, these pulses are generated on the rising edge of the logic 1 active gates. Valid data is accompanied by the output data qualifier on pin IDQ. In addition invalid cycles are marked with output code 00H.

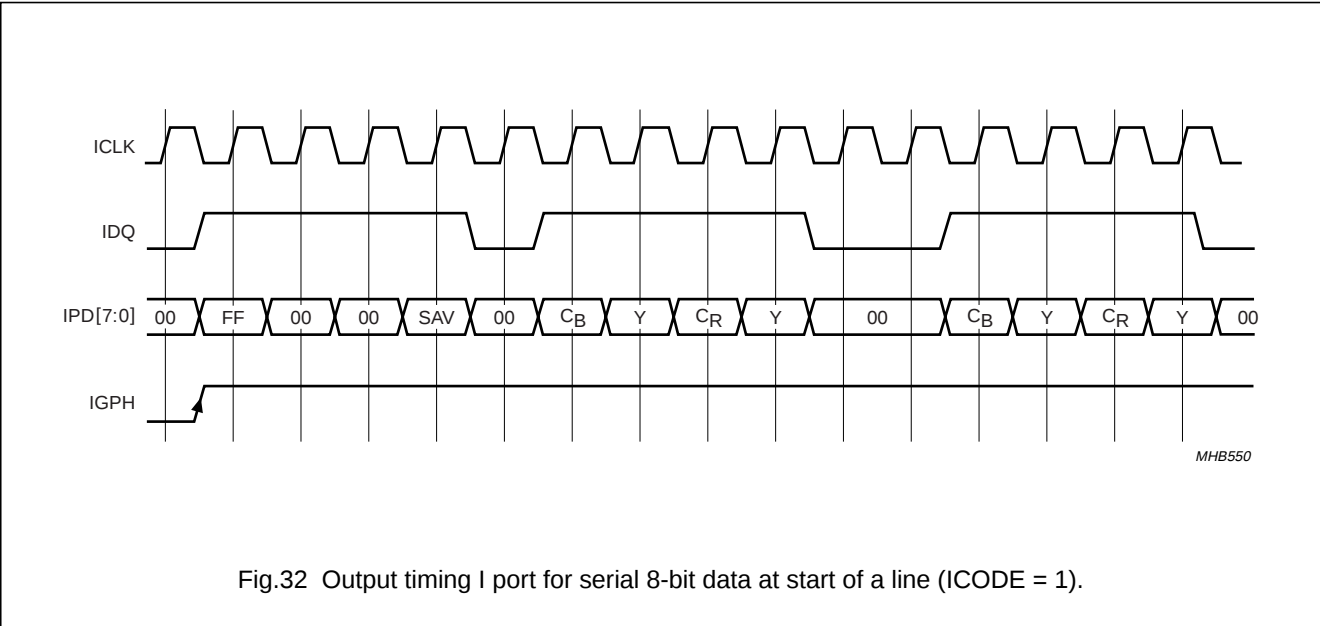
The IDQ output pin may be defined to be a gated clock output signal (ICLK AND internal IDQ).

9.7.2 X PORT INPUT TIMING

At the X port the input timing requirements are the same as those for the I port output. But different to those below:

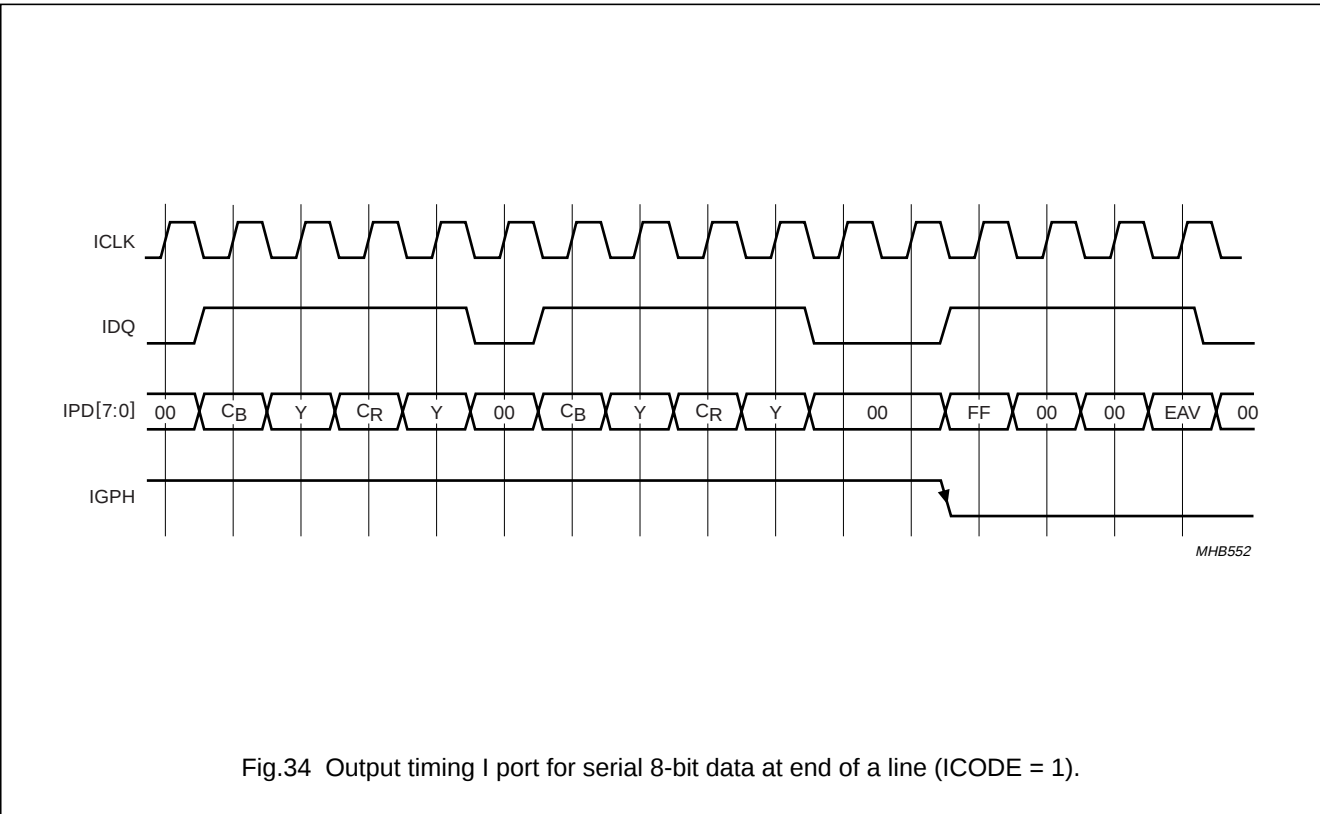
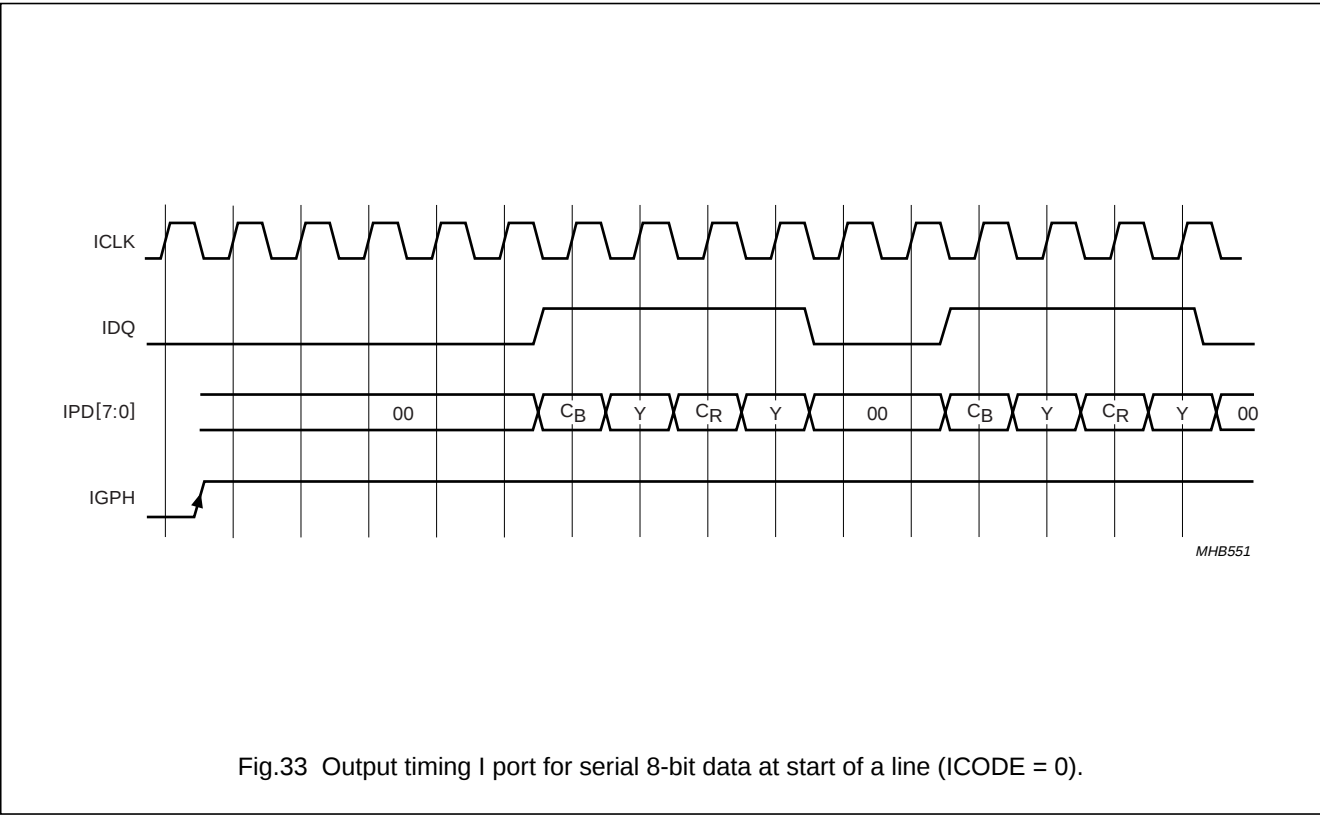
- It is not necessary to mark invalid cycles with a 00H code
- No constraints on the input qualifier (can be a random pattern)
- XCLK may be a gated clock (XCLK AND external XDQ).

**Remark:** All timings illustrated in Figs 32 to 38 are given for an uninterrupted output stream (no handshake with the external hardware).



PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

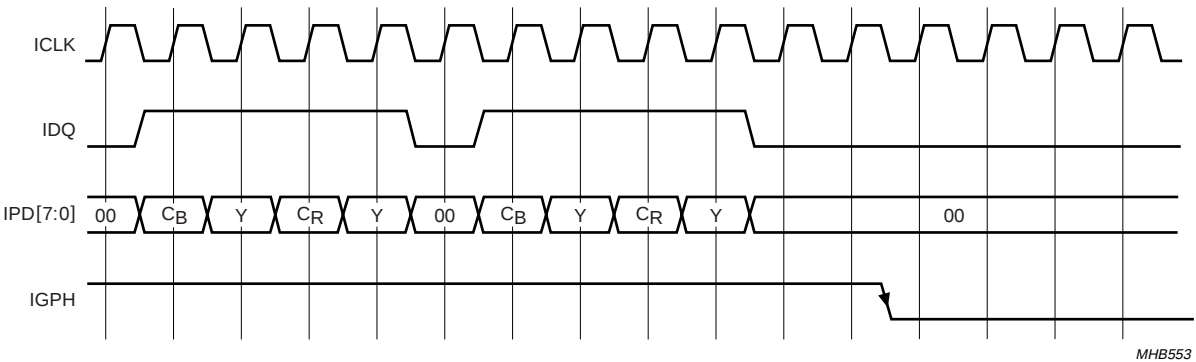


Fig.35 Output timing I port for serial 8-bit data at end of a line (ICODE = 0).

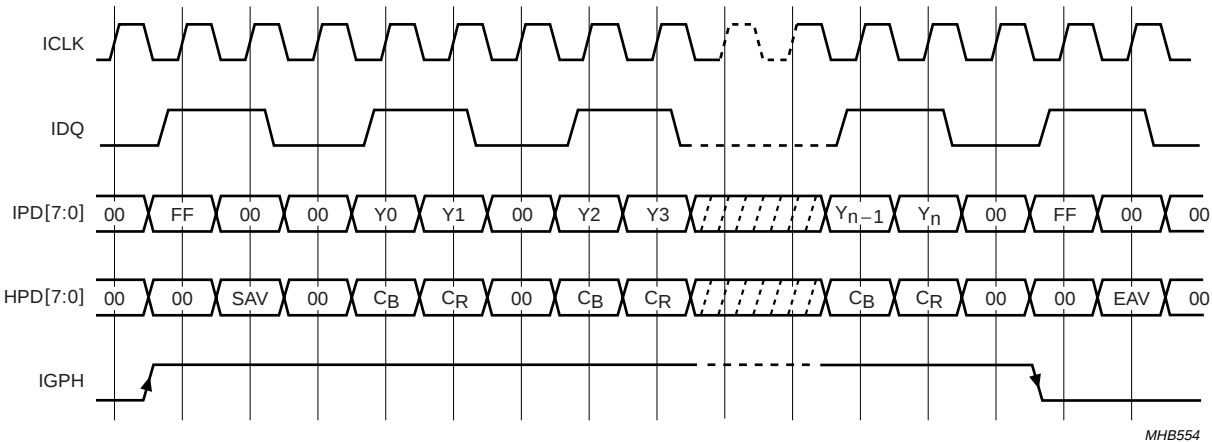


Fig.36 Output timing for 16-bit data output via I port and H port with codes (ICODE = 1), timing is like 8-bit output, but packages of 2 bytes per valid cycle.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

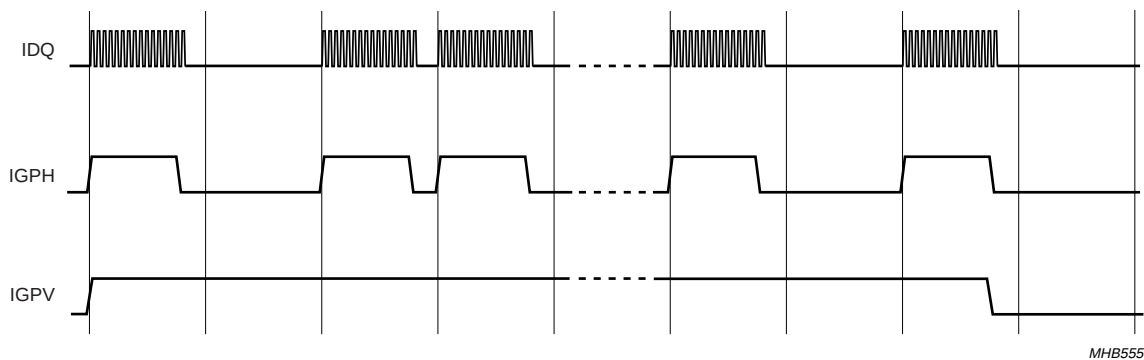


Fig.37 H gate and V gate output timing.

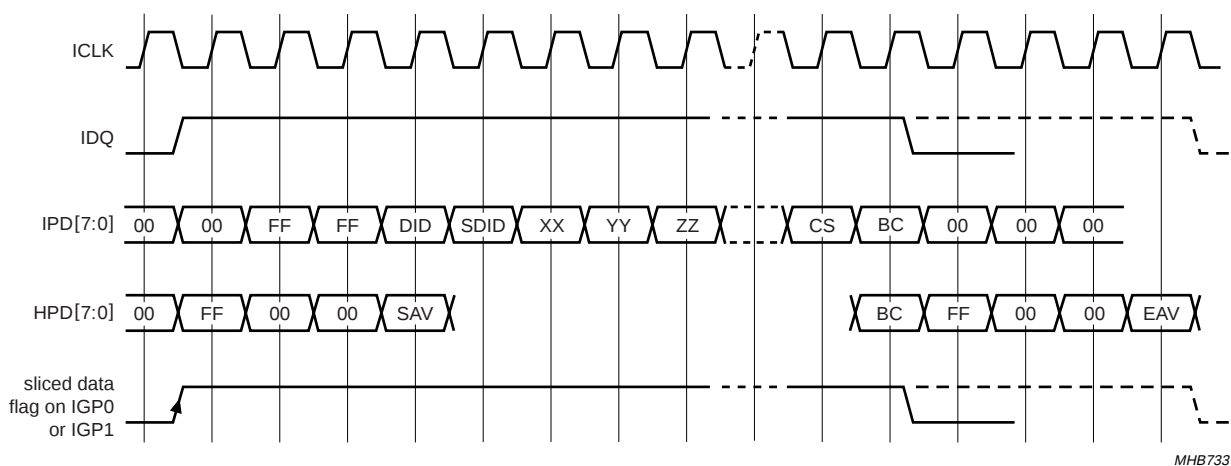


Fig.38 Output timing for sliced VBI data in 8-bit serial output mode (dotted graphs for SAV/EAV mode).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 10 BOUNDARY SCAN TEST

The SAA7114 has built-in logic and 5 dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAA7114 follows the “*IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture*” set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset ( $\overline{\text{TRST}}$ ), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, INTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 35. Details about the JTAG BST-TEST can be found in specification “*IEEE Std. 1149.1*”. A file containing the detailed Boundary Scan Description Language (BSDL) description of the SAA7114 is available on request.

**Table 35** BST instructions supported by the SAA7114

| INSTRUCTION | DESCRIPTION                                                                                                                                                                                                        |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BYPASS      | This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.                                                                  |
| EXTEST      | This mandatory instruction allows testing of off-chip circuitry and board level interconnections.                                                                                                                  |
| SAMPLE      | This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register. |
| CLAMP       | This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.                               |
| IDCODE      | This optional instruction will provide information on the components manufacturer, part number and version number.                                                                                                 |
| INTEST      | This optional instruction allows testing of the internal logic (no customer support available).                                                                                                                    |
| USER1       | This private instruction allows testing by the manufacturer (no customer support available).                                                                                                                       |

### 10.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST\_LOGIC\_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST\_LOGIC\_RESET state by setting the  $\overline{\text{TRST}}$  pin LOW.

### 10.2 Device identification codes

A device identification register is specified in “*IEEE Std. 1149.1b-1994*”. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between pins TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE\_DATA\_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit D31 is the most significant bit (nearest to TDI) and bit D0 is the least significant bit (nearest to TDO); see Fig.39.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

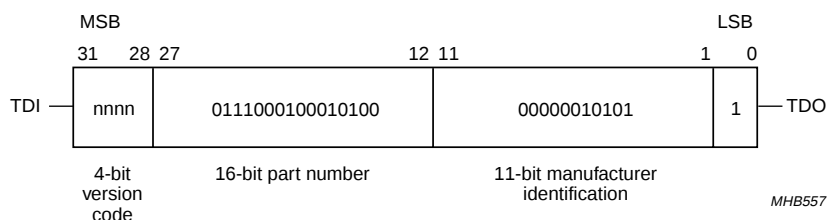


Fig.39 32 bits of identification code.

## 11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all ground pins connected together and grounded (0 V); all supply pins connected together.

| SYMBOL          | PARAMETER                                                | CONDITIONS                 | MIN. | MAX.           | UNIT |
|-----------------|----------------------------------------------------------|----------------------------|------|----------------|------|
| $V_{DD}$        | digital supply voltage                                   |                            | -0.5 | +4.6           | V    |
| $V_{DDA}$       | analog supply voltage                                    |                            | -0.5 | +4.6           | V    |
| $V_{i(A)}$      | input voltage at analog inputs                           |                            | -0.5 | +4.6           | V    |
| $V_{i(n)}$      | input voltage at pins XTALI, SDA and SCL                 |                            | -0.5 | $V_{DD} + 0.5$ | V    |
| $V_{i(D)}$      | input voltage at digital inputs or I/O pins              | outputs in 3-state         | -0.5 | +4.6           | V    |
|                 |                                                          | outputs in 3-state; note 1 | -0.5 | +5.5           | V    |
| $\Delta V_{SS}$ | voltage difference between $V_{SSA(n)}$ and $V_{SSD(n)}$ |                            | -    | 100            | mV   |
| $T_{stg}$       | storage temperature                                      |                            | -65  | +150           | °C   |
| $T_{amb}$       | ambient temperature                                      |                            | 0    | 70             | °C   |
| $V_{esd}$       | electrostatic discharge voltage                          | human body model; note 2   | -    | ±2000          | V    |
|                 |                                                          | machine model; note 3      | -    | ±150           | V    |

### Notes

- Condition for maximum voltage at digital inputs or I/O pins:  $3.0\text{ V} < V_{DD} < 3.6\text{ V}$ .
- Class 2 according to EIA/JESD22-114-B.
- Class A according to EIA/JESD22-115-A.

## 12 THERMAL CHARACTERISTICS

| SYMBOL        | PARAMETER                                   | CONDITIONS  | VALUE             | UNIT |
|---------------|---------------------------------------------|-------------|-------------------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air |                   |      |
|               | SAA7114E                                    |             | 38 <sup>(1)</sup> | K/W  |
|               | SAA7114H                                    |             | 38 <sup>(1)</sup> | K/W  |

### Note

- The overall  $R_{th(j-a)}$  value can vary depending on the board layout. To minimize the effective  $R_{th(j-a)}$  all power and ground pins must be connected to the power and ground layers directly. An ample copper area direct under the SAA7114 with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective  $R_{th(j-a)}$ . Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 13 CHARACTERISTICS

$V_{DDDD} = 3.0$  to  $3.6$  V;  $V_{DDA} = 3.1$  to  $3.5$  V;  $T_{amb} = 0$  to  $70$  °C (typical values excluded); timings and levels refer to drawings and conditions illustrated in Fig.40; unless otherwise specified.

| SYMBOL                                    | PARAMETER                                                          | CONDITIONS                                                                                                                    | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| <b>Supplies</b>                           |                                                                    |                                                                                                                               |      |      |      |      |
| $V_{DDDD}$                                | digital supply voltage                                             |                                                                                                                               | 3.0  | 3.3  | 3.6  | V    |
| $I_{DDDD}$                                | digital supply current                                             | X port 3-state; 8-bit I port                                                                                                  | –    | 90   | –    | mA   |
| $P_D$                                     | power dissipation digital part                                     |                                                                                                                               | –    | 300  | –    | mW   |
| $V_{DDA}$                                 | analog supply voltage                                              |                                                                                                                               | 3.1  | 3.3  | 3.5  | V    |
| $I_{DDA}$                                 | analog supply current                                              | AOSL1 and AOSL0 = 0<br>CVBS mode                                                                                              | –    | 47   | –    | mA   |
|                                           |                                                                    | Y/C mode                                                                                                                      | –    | 72   | –    | mA   |
| $P_A$                                     | power dissipation analog part                                      | CVBS mode                                                                                                                     | –    | 150  | –    | mW   |
|                                           |                                                                    | Y/C mode                                                                                                                      | –    | 240  | –    | mW   |
| $P_{tot(A+D)}$                            | total power dissipation analog and digital part                    | CVBS mode                                                                                                                     | –    | 450  | –    | mW   |
|                                           |                                                                    | Y/C mode                                                                                                                      | –    | 540  | –    | mW   |
| $P_{tot(A+D)(pd)}$                        | total power dissipation analog and digital part in power-down mode | CE pulled down to ground                                                                                                      | –    | 5    | –    | mW   |
| $P_{tot(A+D)(ps)}$                        | total power dissipation analog and digital part in power-save mode | I <sup>2</sup> C-bus controlled via subaddress 88H = 0FH                                                                      | –    | 75   | –    | mW   |
| <b>Analog part</b>                        |                                                                    |                                                                                                                               |      |      |      |      |
| $I_{clamp}$                               | clamping current                                                   | $V_i = 0.9$ V DC                                                                                                              | –    | ±8   | –    | µA   |
| $V_{i(p-p)}$                              | input voltage (peak-to-peak value)                                 | for normal video levels<br>1 V (p-p), –3 dB<br>termination 27/47 Ω and<br>AC coupling required;<br>coupling capacitor = 22 nF | –    | 0.7  | –    | V    |
| $ Z_i $                                   | input impedance                                                    | clamping current off                                                                                                          | 200  | –    | –    | kΩ   |
| $C_i$                                     | input capacitance                                                  |                                                                                                                               | –    | –    | 10   | pF   |
| $\alpha_{cs}$                             | channel crosstalk                                                  | $f_i < 5$ MHz                                                                                                                 | –    | –    | –50  | dB   |
| <b>9-bit analog-to-digital converters</b> |                                                                    |                                                                                                                               |      |      |      |      |
| B                                         | analog bandwidth                                                   | at –3 dB                                                                                                                      | –    | 7    | –    | MHz  |
| $\phi_{diff}$                             | differential phase                                                 | amplifier plus anti-alias filter bypassed                                                                                     | –    | 2    | –    | deg  |
| $G_{diff}$                                | differential gain                                                  | amplifier plus anti-alias filter bypassed                                                                                     | –    | 2    | –    | %    |
| $f_{clk(ADC)}$                            | ADC clock frequency                                                |                                                                                                                               | 12.8 | –    | 14.3 | MHz  |
| $LE_{dc(d)}$                              | DC differential linearity error                                    |                                                                                                                               | –    | 0.7  | –    | LSB  |
| $LE_{dc(i)}$                              | DC integral linearity error                                        |                                                                                                                               | –    | 1    | –    | LSB  |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| SYMBOL                                            | PARAMETER                                                    | CONDITIONS                          | MIN.                | TYP.  | MAX.                   | UNIT |
|---------------------------------------------------|--------------------------------------------------------------|-------------------------------------|---------------------|-------|------------------------|------|
| <b>Digital inputs</b>                             |                                                              |                                     |                     |       |                        |      |
| $V_{IL(SCL,SDA)}$                                 | LOW-level input voltage pins SDA and SCL                     |                                     | -0.5                | –     | +0.3V <sub>DDD</sub>   | V    |
| $V_{IH(SCL,SDA)}$                                 | HIGH-level input voltage pins SDA and SCL                    |                                     | 0.7V <sub>DDD</sub> | –     | V <sub>DDD</sub> + 0.5 | V    |
| $V_{IL(XTALI)}$                                   | LOW-level CMOS input voltage pin XTALI                       |                                     | -0.3                | –     | +0.8                   | V    |
| $V_{IH(XTALI)}$                                   | HIGH-level CMOS input voltage pin XTALI                      |                                     | 2.0                 | –     | V <sub>DDD</sub> + 0.3 | V    |
| $V_{IL(n)}$                                       | LOW-level input voltage all other inputs                     |                                     | -0.3                | –     | +0.8                   | V    |
| $V_{IH(n)}$                                       | HIGH-level input voltage all other inputs                    |                                     | 2.0                 | –     | 5.5                    | V    |
| $I_{LI}$                                          | input leakage current                                        |                                     | –                   | –     | 1                      | μA   |
| $I_{LI/O}$                                        | I/O leakage current                                          |                                     | –                   | –     | 10                     | μA   |
| $C_i$                                             | input capacitance                                            | I/O at high impedance               | –                   | –     | 8                      | pF   |
| <b>Digital outputs; note 1</b>                    |                                                              |                                     |                     |       |                        |      |
| $V_{OL(SDA)}$                                     | LOW-level output voltage pin SDA                             | SDA at 3 mA sink current            | –                   | –     | 0.4                    | V    |
| $V_{OL(clk)}$                                     | LOW-level output voltage for clocks                          |                                     | -0.5                | –     | +0.6                   | V    |
| $V_{OH(clk)}$                                     | HIGH-level output voltage for clocks                         |                                     | 2.4                 | –     | V <sub>DDD</sub> + 0.5 | V    |
| $V_{OL(n)}$                                       | LOW-level output voltage all other digital outputs           |                                     | 0                   | –     | 0.4                    | V    |
| $V_{OH(n)}$                                       | HIGH-level output voltage all other digital outputs          |                                     | 2.4                 | –     | V <sub>DDD</sub> + 0.5 | V    |
| <b>Clock output timing (LLC and LLC2); note 2</b> |                                                              |                                     |                     |       |                        |      |
| $C_L$                                             | output load capacitance                                      |                                     | 15                  | –     | 50                     | pF   |
| $T_{cy}$                                          | cycle time                                                   | pin LLC                             | 35                  | –     | 39                     | ns   |
|                                                   |                                                              | pin LLC2                            | 70                  | –     | 78                     | ns   |
| $\delta$                                          | duty factors for $t_{LLCH}/t_{LLC}$ and $t_{LLC2H}/t_{LLC2}$ | $C_L = 40$ pF                       | 40                  | –     | 60                     | %    |
| $t_r$                                             | rise time LLC and LLC2                                       | 0.2 V to V <sub>DDD</sub> – 0.2 V   | –                   | –     | 5                      | ns   |
| $t_f$                                             | fall time LLC and LLC2                                       | V <sub>DDD</sub> – 0.2 V to 0.2 V   | –                   | –     | 5                      | ns   |
| $t_d(LLC-LLC2)$                                   | delay time between LLC and LLC2 output                       | measured at 1.5 V;<br>$C_L = 25$ pF | -4                  | –     | +8                     | ns   |
| <b>Horizontal PLL</b>                             |                                                              |                                     |                     |       |                        |      |
| $f_{hor(nom)}$                                    | nominal line frequency                                       | 50 Hz field                         | –                   | 15625 | –                      | Hz   |
|                                                   |                                                              | 60 Hz field                         | –                   | 15734 | –                      | Hz   |
| $\Delta f_{hor}/f_{hor(nom)}$                     | permissible static deviation                                 |                                     | –                   | –     | 5.7                    | %    |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| SYMBOL                                                                    | PARAMETER                                                | CONDITIONS | MIN.      | TYP.           | MAX.                    | UNIT     |
|---------------------------------------------------------------------------|----------------------------------------------------------|------------|-----------|----------------|-------------------------|----------|
| <b>Subcarrier PLL</b>                                                     |                                                          |            |           |                |                         |          |
| $f_{sc(nom)}$                                                             | nominal subcarrier frequency                             | PAL BGHI   | –         | 4433619        | –                       | Hz       |
|                                                                           |                                                          | NTSC M     | –         | 3579545        | –                       | Hz       |
|                                                                           |                                                          | PAL M      | –         | 3575612        | –                       | Hz       |
|                                                                           |                                                          | PAL N      | –         | 3582056        | –                       | Hz       |
| $\Delta f_{sc}$                                                           | lock-in range                                            |            | $\pm 400$ | –              | –                       | Hz       |
| <b>Crystal oscillator for 32.11 MHz; note 3</b>                           |                                                          |            |           |                |                         |          |
| $f_{xtal(nom)}$                                                           | nominal frequency                                        |            | –         | 32.11          | –                       | MHz      |
| $\Delta f_{xtal(nom)}$                                                    | permissible nominal frequency deviation                  |            | –         | –              | $\pm 70 \times 10^{-6}$ |          |
| $\Delta f_{xtal(nom)(T)}$                                                 | permissible nominal frequency deviation with temperature |            | –         | –              | $\pm 30 \times 10^{-6}$ |          |
| <b>CRYSTAL SPECIFICATION (X1)</b>                                         |                                                          |            |           |                |                         |          |
| $T_{amb(X1)}$                                                             | operating ambient temperature                            |            | 0         | –              | 70                      | °C       |
| $C_L$                                                                     | load capacitance                                         |            | 8         | –              | –                       | pF       |
| $R_s$                                                                     | series resonance resistor                                |            | –         | 40             | 80                      | $\Omega$ |
| $C_1$                                                                     | motional capacitance                                     |            | –         | $1.5 \pm 20\%$ | –                       | fF       |
| $C_0$                                                                     | parallel capacitance                                     |            | –         | $4.3 \pm 20\%$ | –                       | pF       |
| <b>Crystal oscillator for 24.576 MHz; note 3</b>                          |                                                          |            |           |                |                         |          |
| $f_{xtal(nom)}$                                                           | nominal frequency                                        |            | –         | 24.576         | –                       | MHz      |
| $\Delta f_{xtal(nom)}$                                                    | permissible nominal frequency deviation                  |            | –         | –              | $\pm 50 \times 10^{-6}$ |          |
| $\Delta f_{xtal(nom)(T)}$                                                 | permissible nominal frequency deviation with temperature |            | –         | –              | $\pm 20 \times 10^{-6}$ |          |
| <b>CRYSTAL SPECIFICATION (X1)</b>                                         |                                                          |            |           |                |                         |          |
| $T_{amb(X1)}$                                                             | ambient temperature                                      |            | 0         | –              | 70                      | °C       |
| $C_L$                                                                     | load capacitance                                         |            | 8         | –              | –                       | pF       |
| $R_s$                                                                     | series resonance resistor                                |            | –         | 40             | 80                      | $\Omega$ |
| $C_1$                                                                     | motional capacitance                                     |            | –         | $1.5 \pm 20\%$ | –                       | fF       |
| $C_0$                                                                     | parallel capacitance                                     |            | –         | $3.5 \pm 20\%$ | –                       | pF       |
| <b>Clock input timing (XCLK)</b>                                          |                                                          |            |           |                |                         |          |
| $T_{cy}$                                                                  | cycle time                                               |            | 31        | –              | 45                      | ns       |
| $\delta$                                                                  | duty factors for $t_{LLCH}/t_{LLC}$                      |            | 40        | 50             | 60                      | %        |
| $t_r$                                                                     | rise time                                                |            | –         | –              | 5                       | ns       |
| $t_f$                                                                     | fall time                                                |            | –         | –              | 5                       | ns       |
| <b>Data and control signal input timing X port, related to XCLK input</b> |                                                          |            |           |                |                         |          |
| $t_{SU;DAT}$                                                              | input data set-up time                                   |            | –         | 10             | –                       | ns       |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| SYMBOL                                                                                                                      | PARAMETER                                           | CONDITIONS    | MIN. | TYP. | MAX. | UNIT |
|-----------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|---------------|------|------|------|------|
| $t_{HD;DAT}$                                                                                                                | input data hold time                                |               | –    | 3    | –    | ns   |
| <b>Clock output timing</b>                                                                                                  |                                                     |               |      |      |      |      |
| $C_L$                                                                                                                       | output load capacitance                             |               | 15   | –    | 50   | pF   |
| $T_{cy}$                                                                                                                    | cycle time                                          |               | 35   | –    | 39   | ns   |
| $\delta$                                                                                                                    | duty factors for $t_{XCLKH}/t_{XCLKL}$              |               | 35   | –    | 65   | %    |
| $t_r$                                                                                                                       | rise time                                           | 0.6 to 2.6 V  | –    | –    | 5    | ns   |
| $t_f$                                                                                                                       | fall time                                           | 2.6 to 0.6 V  | –    | –    | 5    | ns   |
| <b>Data and control signal output timing X port, related to XCLK output (for XPCK[1:0]83H[5:4] = 00 is default); note 2</b> |                                                     |               |      |      |      |      |
| $C_L$                                                                                                                       | output load capacitance                             |               | 15   | –    | 50   | pF   |
| $t_{OHD;DAT}$                                                                                                               | output data hold time                               | $C_L = 15$ pF | –    | 14   | –    | ns   |
| $t_{PD}$                                                                                                                    | propagation delay from positive edge of XCLK output | $C_L = 15$ pF | –    | 24   | –    | ns   |
| <b>Control signal output timing RT port, related to LLC output</b>                                                          |                                                     |               |      |      |      |      |
| $C_L$                                                                                                                       | output load capacitance                             |               | 15   | –    | 50   | pF   |
| $t_{OHD;DAT}$                                                                                                               | output hold time                                    | $C_L = 15$ pF | –    | 14   | –    | ns   |
| $t_{PD}$                                                                                                                    | propagation delay from positive edge of LLC output  | $C_L = 15$ pF | –    | 24   | –    | ns   |
| <b>ICLK output timing</b>                                                                                                   |                                                     |               |      |      |      |      |
| $C_L$                                                                                                                       | output load capacitance                             |               | 15   | –    | 50   | pF   |
| $T_{cy}$                                                                                                                    | cycle time                                          |               | 31   | –    | 45   | ns   |
| $\delta$                                                                                                                    | duty factors for $t_{ICLKH}/t_{ICCLKL}$             |               | 35   | –    | 65   | %    |
| $t_r$                                                                                                                       | rise time                                           | 0.6 to 2.6 V  | –    | –    | 5    | ns   |
| $t_f$                                                                                                                       | fall time                                           | 2.6 to 0.6 V  | –    | –    | 5    | ns   |
| <b>Data and control signal output timing I port, related to ICLK output (for IPCK[1:0]87H[5:4] = 00 is default)</b>         |                                                     |               |      |      |      |      |
| $C_L$                                                                                                                       | output load capacitance at all outputs              |               | 15   | –    | 50   | pF   |
| $t_{OHD;DAT}$                                                                                                               | output data hold time                               | $C_L = 15$ pF | –    | 12   | –    | ns   |
| $t_{o(d)}$                                                                                                                  | output delay time                                   | $C_L = 15$ pF | –    | 22   | –    | ns   |
| <b>ICLK input timing</b>                                                                                                    |                                                     |               |      |      |      |      |
| $T_{cy}$                                                                                                                    | cycle time                                          |               | 31   | –    | 100  | ns   |

## Notes

1. The levels must be measured with load circuits; 1.2 k $\Omega$  at 3 V (TTL load);  $C_L = 50$  pF.
2. The effects of rise and fall times are included in the calculation of  $t_{OHD;DAT}$  and  $t_{PD}$ . Timings and levels refer to drawings and conditions illustrated in Fig.40.
3. The crystal oscillator drive level is typical 0.28 mW.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

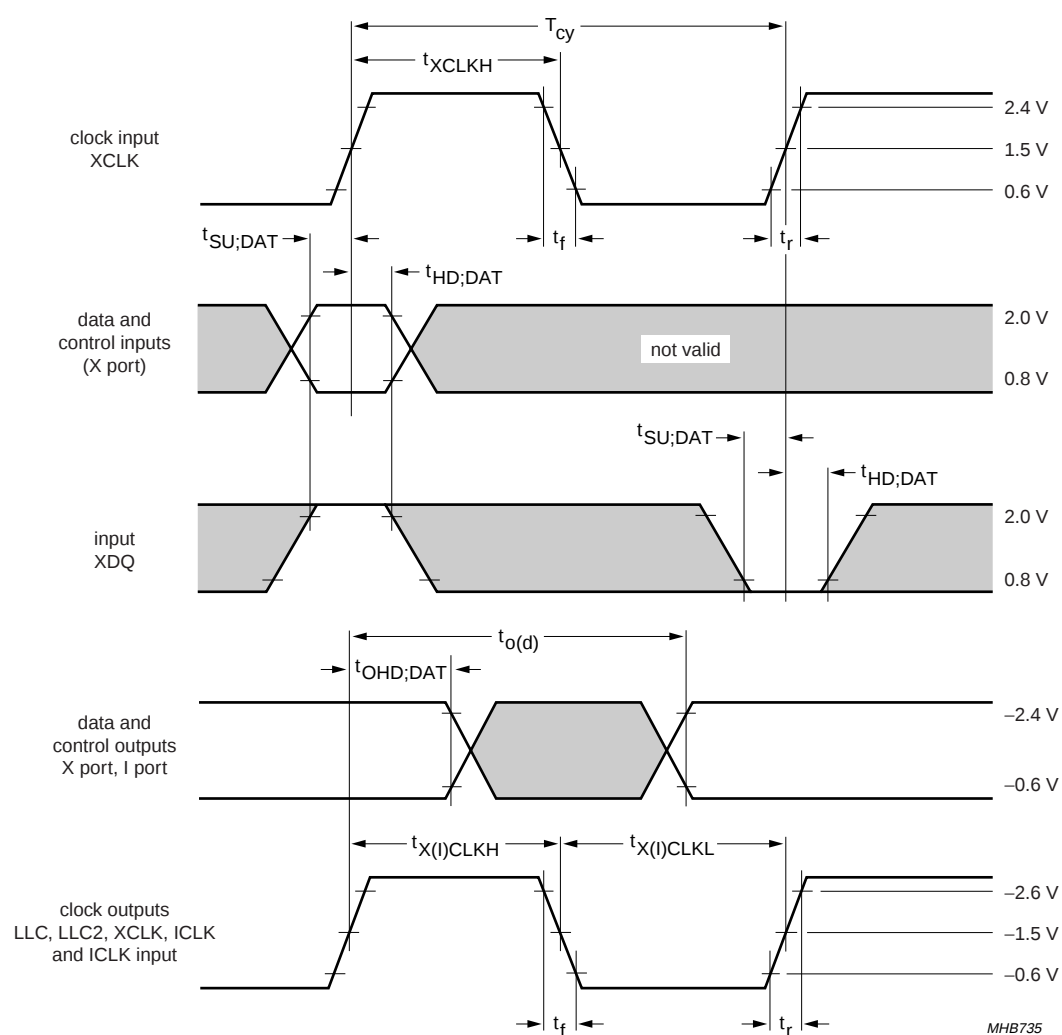


Fig.40 Data input/output timing diagram (X port, RT port and I port).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 14 APPLICATION INFORMATION

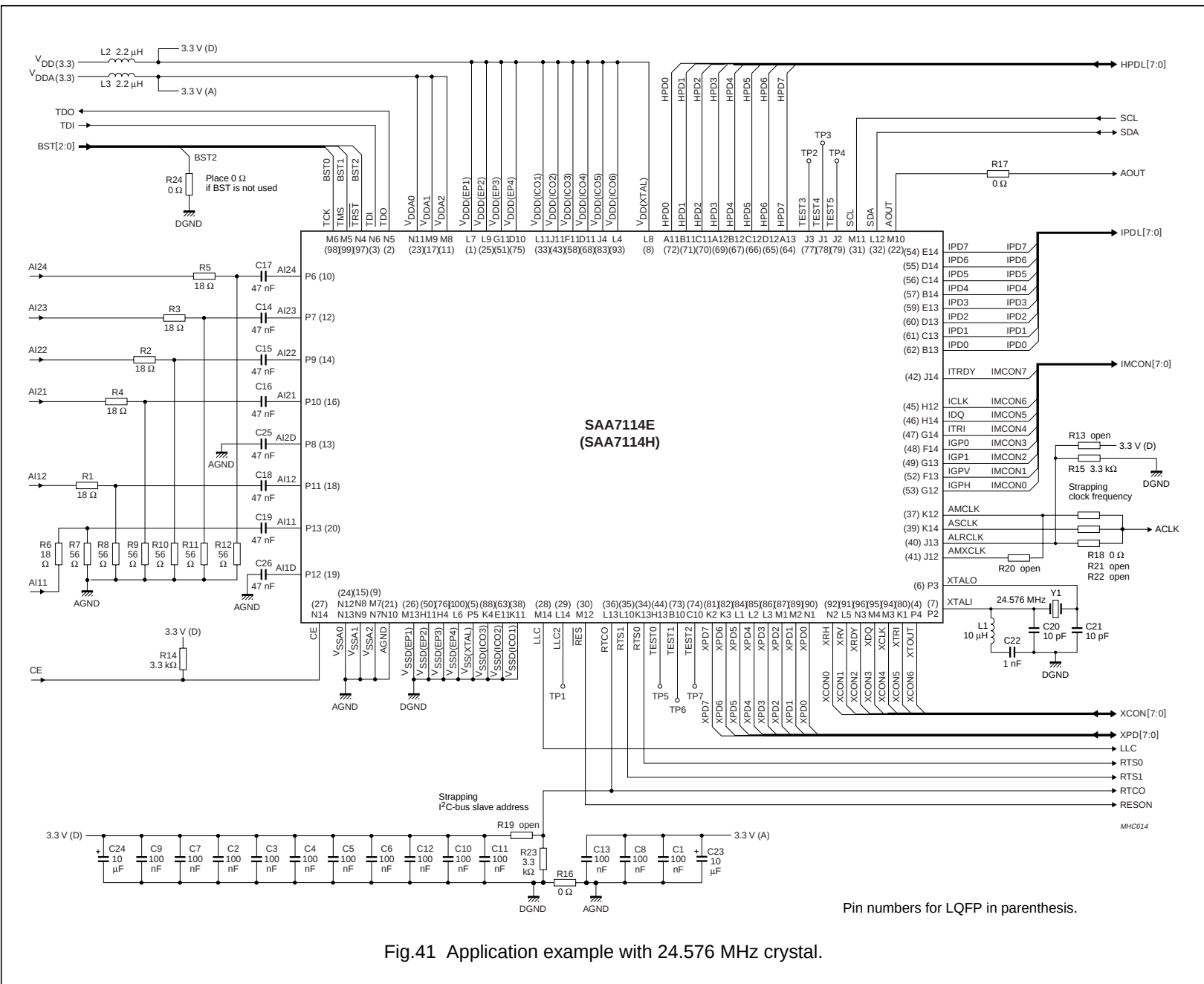
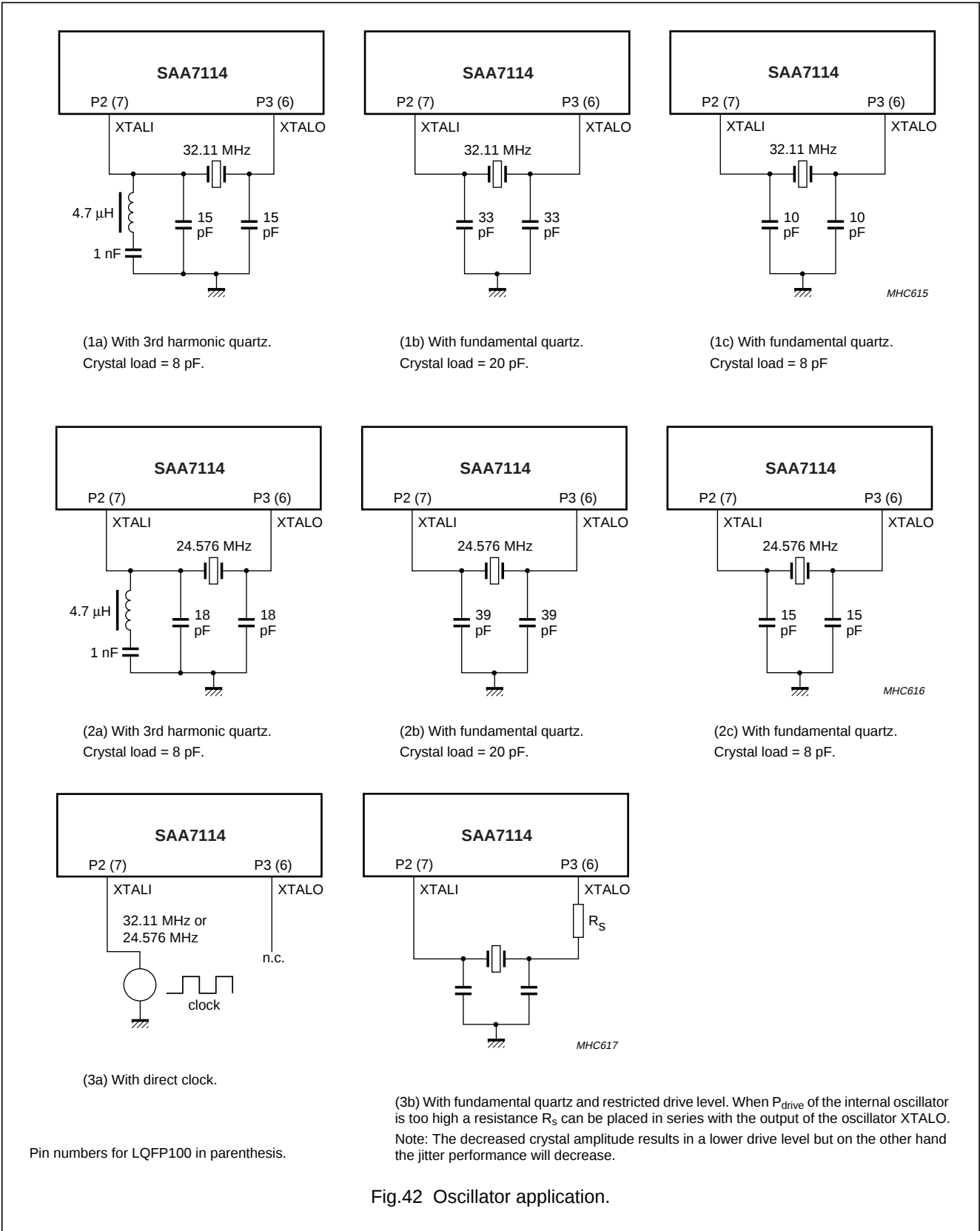


Fig.41 Application example with 24.576 MHz crystal.

Pin numbers for LQFP in parenthesis.

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

15 I<sup>2</sup>C-BUS DESCRIPTION

The SAA7114 supports the ‘fast mode’ I<sup>2</sup>C-bus specification extension (data rate up to 400 kbits/s).

15.1 I<sup>2</sup>C-bus format

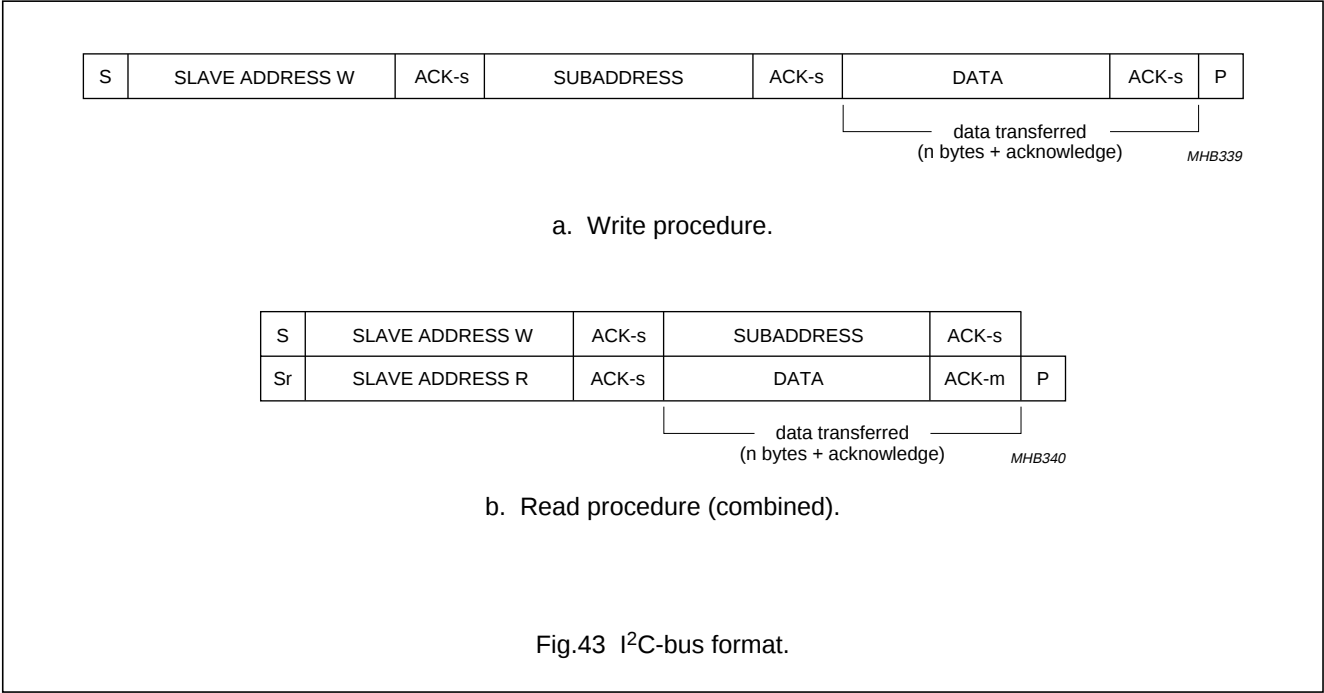


Table 36 Description of I<sup>2</sup>C-bus format

| CODE            | DESCRIPTION                                                                                                                                                |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S               | START condition                                                                                                                                            |
| Sr              | repeated START condition                                                                                                                                   |
| SLAVE ADDRESS W | ‘0100 0010’ (42H, default) or ‘0100 0000’ (40H; note 1)                                                                                                    |
| SLAVE ADDRESS R | ‘0100 0011’ (43H, default) or ‘0100 0001’ (41H; note 1)                                                                                                    |
| ACK-s           | acknowledge generated by the slave                                                                                                                         |
| ACK-m           | acknowledge generated by the master                                                                                                                        |
| SUBADDRESS      | subaddress byte; see Tables 37 and 38                                                                                                                      |
| DATA            | data byte; see Table 38; if more than one byte DATA is transmitted the subaddress pointer is automatically incremented                                     |
| P               | STOP condition                                                                                                                                             |
| X               | read/write control bit (LSB slave address); X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter) |

Note

1. If pin RTCO strapped to supply voltage via a 3.3 kΩ resistor.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 37** Subaddress description and access

| SUBADDRESS                                         | DESCRIPTION                      | ACCESS (READ/WRITE) |
|----------------------------------------------------|----------------------------------|---------------------|
| 00H                                                | chip version                     | read only           |
| F0H to FFH                                         | reserved                         | –                   |
| <b>Video decoder: 01H to 2FH</b>                   |                                  |                     |
| 01H to 05H                                         | front-end part                   | read and write      |
| 06H to 19H                                         | decoder part                     | read and write      |
| 1AH to 1EH                                         | reserved                         | –                   |
| 1FH                                                | video decoder status byte        | read only           |
| 20H to 2FH                                         | reserved                         | –                   |
| <b>Audio clock generation: 30H to 3FH</b>          |                                  |                     |
| 30H to 3AH                                         | audio clock generator            | read and write      |
| 3BH to 3FH                                         | reserved                         | –                   |
| <b>General purpose VBI data slicer: 40H to 7FH</b> |                                  |                     |
| 40H to 5EH                                         | VBI data slicer                  | read and write      |
| 5FH                                                | reserved                         | –                   |
| 60H to 62H                                         | VBI data slicer status           | read only           |
| 63H to 7FH                                         | reserved                         | –                   |
| <b>X port, I port and the scaler: 80H to EFH</b>   |                                  |                     |
| 80H to 8FH                                         | task independent global settings | read and write      |
| 90H to BFH                                         | task A definition                | read and write      |
| C0H to EFH                                         | task B definition                | read and write      |

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 38** I<sup>2</sup>C-bus receiver/transmitter overview

| REGISTER FUNCTION                          | SUB<br>ADDR.<br>(HEX) | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|--------------------------------------------|-----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| <b>Chip version: register 00H</b>          |                       |        |        |        |        |        |        |        |        |
| Chip version (read only)                   | 00                    | ID7    | ID6    | ID5    | ID4    | –      | –      | –      | –      |
| <b>Video decoder: registers 01H to 2FH</b> |                       |        |        |        |        |        |        |        |        |
| FRONT-END PART: REGISTERS 01H TO 05H       |                       |        |        |        |        |        |        |        |        |
| Increment delay                            | 01                    | (1)    | (1)    | (1)    | (1)    | IDEL3  | IDEL2  | IDEL1  | IDEL0  |
| Analog input control 1                     | 02                    | FUSE1  | FUSE0  | GUDL1  | GUDL0  | MODE3  | MODE2  | MODE1  | MODE0  |
| Analog input control 2                     | 03                    | (1)    | HLNRS  | VBSL   | WPOFF  | HOLDG  | GAFIX  | GAI28  | GAI18  |
| Analog input control 3                     | 04                    | GAI17  | GAI16  | GAI15  | GAI14  | GAI13  | GAI12  | GAI11  | GAI10  |
| Analog input control 4                     | 05                    | GAI27  | GAI26  | GAI25  | GAI24  | GAI23  | GAI22  | GAI21  | GAI20  |
| DECODER PART: REGISTERS 06H TO 2FH         |                       |        |        |        |        |        |        |        |        |
| Horizontal sync start                      | 06                    | HSB7   | HSB6   | HSB5   | HSB4   | HSB3   | HSB2   | HSB1   | HSB0   |
| Horizontal sync stop                       | 07                    | HSS7   | HSS6   | HSS5   | HSS4   | HSS3   | HSS2   | HSS1   | HSS0   |
| Sync control                               | 08                    | AUFD   | FSEL   | FOET   | HTC1   | HTC0   | HPLL   | VNOI1  | VNOI0  |
| Luminance control                          | 09                    | BYP5   | YCOMB  | LDEL   | LUBW   | LUF13  | LUF12  | LUF11  | LUF10  |
| Luminance brightness control               | 0A                    | DBRI7  | DBRI6  | DBRI5  | DBRI4  | DBRI3  | DBRI2  | DBRI1  | DBRI0  |
| Luminance contrast control                 | 0B                    | DCON7  | DCON6  | DCON5  | DCON4  | DCON3  | DCON2  | DCON1  | DCON0  |
| Chrominance saturation control             | 0C                    | DSAT7  | DSAT6  | DSAT5  | DSAT4  | DSAT3  | DSAT2  | DSAT1  | DSAT0  |
| Chrominance hue control                    | 0D                    | HUEC7  | HUEC6  | HUEC5  | HUEC4  | HUEC3  | HUEC2  | HUEC1  | HUEC0  |
| Chrominance control 1                      | 0E                    | CDTO   | CSTD2  | CSTD1  | CSTD0  | DCVF   | FCTC   | (1)    | CCOMB  |
| Chrominance gain control                   | 0F                    | ACGC   | CGAIN6 | CGAIN5 | CGAIN4 | CGAIN3 | CGAIN2 | CGAIN1 | CGAIN0 |
| Chrominance control 2                      | 10                    | OFFU1  | OFFU0  | OFFV1  | OFFV0  | CHBW   | LCBW2  | LCBW1  | LCBW0  |
| Mode/delay control                         | 11                    | COLO   | RTP1   | HDEL1  | HDEL0  | RTP0   | YDEL2  | YDEL1  | YDEL0  |
| RT signal control                          | 12                    | RTSE13 | RTSE12 | RTSE11 | RTSE10 | RTSE03 | RTSE02 | RTSE01 | RTSE00 |
| RT/X port output control                   | 13                    | RTCE   | XRHS   | XRVS1  | XRVS0  | HLSEL  | OFTS2  | OFTS1  | OFTS0  |
| Analog/ADC/compatibility control           | 14                    | CM99   | UPTCV  | AOSL1  | AOSL0  | XTOUTE | OLDSB  | APCK1  | APCK0  |
| VGATE start, FID change                    | 15                    | VSTA7  | VSTA6  | VSTA5  | VSTA4  | VSTA3  | VSTA2  | VSTA1  | VSTA0  |
| VGATE stop                                 | 16                    | VSTO7  | VSTO6  | VSTO5  | VSTO4  | VSTO3  | VSTO2  | VSTO1  | VSTO0  |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| REGISTER FUNCTION                                                 | SUB<br>ADDR.<br>(HEX) | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
|-------------------------------------------------------------------|-----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Miscellaneous,<br>VGATE configuration and MSBs                    | 17                    | LLCE   | LLC2E  | (1)    | (1)    | (1)    | VGPS   | VSTO8  | VSTA8  |
| Raw data gain control                                             | 18                    | RAWG7  | RAWG6  | RAWG5  | RAWG4  | RAWG3  | RAWG2  | RAWG1  | RAWG0  |
| Raw data offset control                                           | 19                    | RAWO7  | RAWO6  | RAWO5  | RAWO4  | RAWO3  | RAWO2  | RAWO1  | RAWO0  |
| Reserved                                                          | 1A to 1E              | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    |
| Status byte video decoder<br>(read only, OLDSB = 0)               | 1F                    | INTL   | HLVLN  | FIDT   | GLIMT  | GLIMB  | WIPA   | COPRO  | RDCAP  |
| Status byte video decoder<br>(read only, OLDSB = 1)               | 1F                    | INTL   | HLCK   | FIDT   | GLIMT  | GLIMB  | WIPA   | SLTCA  | CODE   |
| Reserved                                                          | 20 to 2F              | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    |
| <b>Audio clock generator part: registers 30H to 3FH</b>           |                       |        |        |        |        |        |        |        |        |
| Audio master clock cycles per<br>field                            | 30                    | ACPF7  | ACPF6  | ACPF5  | ACPF4  | ACPF3  | ACPF2  | ACPF1  | ACPF0  |
|                                                                   | 31                    | ACPF15 | ACPF14 | ACPF13 | ACPF12 | ACPF11 | ACPF10 | ACPF9  | ACPF8  |
|                                                                   | 32                    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | ACPF17 | ACPF16 |
| Reserved                                                          | 33                    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    |
| Audio master clock nominal<br>increment                           | 34                    | ACNI7  | ACNI6  | ACNI5  | ACNI4  | ACNI3  | ACNI2  | ACNI1  | ACNI0  |
|                                                                   | 35                    | ACNI15 | ACNI14 | ACNI13 | ACNI12 | ACNI11 | ACNI10 | ACNI9  | ACNI8  |
|                                                                   | 36                    | (1)    | (1)    | ACNI21 | ACNI20 | ACNI19 | ACNI18 | ACNI17 | ACNI16 |
| Reserved                                                          | 37                    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    |
| Clock ratio AMXCLK to ASCLK                                       | 38                    | (1)    | (1)    | SDIV5  | SDIV4  | SDIV3  | SDIV2  | SDIV1  | SDIV0  |
| Clock ratio ASCLK to ALRCLK                                       | 39                    | (1)    | (1)    | LRDIV5 | LRDIV4 | LRDIV3 | LRDIV2 | LRDIV1 | LRDIV0 |
| Audio clock generator basic<br>set-up                             | 3A                    | (1)    | (1)    | (1)    | (1)    | APLL   | AMVR   | LRPH   | SCPH   |
| Reserved                                                          | 3B to 3F              | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    |
| <b>General purpose VBI data slicer part: registers 40H to 7FH</b> |                       |        |        |        |        |        |        |        |        |
| Slicer control 1                                                  | 40                    | (1)    | HAM_N  | FCE    | HUNT_N | (1)    | (1)    | (1)    | (1)    |
| LCR2 to LCR24 (n = 2 to 24)                                       | 41 to 57              | LCRn_7 | LCRn_6 | LCRn_5 | LCRn_4 | LCRn_3 | LCRn_2 | LCRn_1 | LCRn_0 |
| Programmable framing code                                         | 58                    | FC7    | FC6    | FC5    | FC4    | FC3    | FC2    | FC1    | FC0    |
| Horizontal offset for slicer                                      | 59                    | HOFF7  | HOFF6  | HOFF5  | HOFF4  | HOFF3  | HOFF2  | HOFF1  | HOFF0  |
| Vertical offset for slicer                                        | 5A                    | VOFF7  | VOFF6  | VOFF5  | VOFF4  | VOFF3  | VOFF2  | VOFF1  | VOFF0  |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| REGISTER FUNCTION                                               | SUB<br>ADDR.<br>(HEX) | D7    | D6     | D5    | D4    | D3    | D2     | D1     | D0     |
|-----------------------------------------------------------------|-----------------------|-------|--------|-------|-------|-------|--------|--------|--------|
| Field offset and MSBs for horizontal and vertical offset        | 5B                    | FOFF  | RECODE | (1)   | VOFF8 | (1)   | HOFF10 | HOFF9  | HOFF8  |
| Reserved (for testing)                                          | 5C                    | (1)   | (1)    | (1)   | (1)   | (1)   | (1)    | (1)    | (1)    |
| Header and data identification (DID) code control               | 5D                    | FVREF | (1)    | DID5  | DID4  | DID3  | DID2   | DID1   | DID0   |
| Sliced data identification (SDID) code                          | 5E                    | (1)   | (1)    | SDID5 | SDID4 | SDID3 | SDID2  | SDID1  | SDID0  |
| Reserved                                                        | 5F                    | (1)   | (1)    | (1)   | (1)   | (1)   | (1)    | (1)    | (1)    |
| Slicer status byte 0 (read only)                                | 60                    | –     | FC8V   | FC7V  | VPSV  | PPV   | CCV    | –      | –      |
| Slicer status byte 1 (read only)                                | 61                    | –     | –      | F21_N | LN8   | LN7   | LN6    | LN5    | LN4    |
| Slicer status byte 2 (read only)                                | 62                    | LN3   | LN2    | LN1   | LN0   | DT3   | DT2    | DT1    | DT0    |
| Reserved                                                        | 63 to 7F              | (1)   | (1)    | (1)   | (1)   | (1)   | (1)    | (1)    | (1)    |
| <b>X port, I port and the scaler part: registers 80H to EFH</b> |                       |       |        |       |       |       |        |        |        |
| TASK INDEPENDENT GLOBAL SETTINGS: 80H to 8FH                    |                       |       |        |       |       |       |        |        |        |
| Global control 1                                                | 80                    | (1)   | SMOD   | TEB   | TEA   | ICKS3 | ICKS2  | ICKS1  | ICKS0  |
| Reserved                                                        | 81 and 82             | (1)   | (1)    | (1)   | (1)   | (1)   | (1)    | (1)    | (1)    |
| X port I/O enable and output clock phase control                | 83                    | (1)   | (1)    | XPCK1 | XPCK0 | (1)   | XRQT   | XPE1   | XPE0   |
| I port signal definitions                                       | 84                    | IDG01 | IDG00  | IDG11 | IDG10 | IDV1  | IDV0   | IDH1   | IDH0   |
| I port signal polarities                                        | 85                    | ISWP1 | ISWP0  | ILLV  | IG0P  | IG1P  | IRVP   | IRHP   | IDQP   |
| I port FIFO flag control and arbitration                        | 86                    | VITX1 | VITX0  | IDG02 | IDG12 | FFL1  | FFL0   | FEL1   | FEL0   |
| I port I/O enable, output clock and gated clock phase control   | 87                    | IPCK3 | IPCK2  | IPCK1 | IPCK0 | (1)   | (1)    | IPE1   | IPE0   |
| Power save control                                              | 88                    | CH4EN | CH2EN  | SWRST | DPROG | SLM3  | (1)    | SLM1   | SLM0   |
| Reserved                                                        | 89 to 8E              | (1)   | (1)    | (1)   | (1)   | (1)   | (1)    | (1)    | (1)    |
| Status information scaler part                                  | 8F                    | XTRI  | ITRI   | FFIL  | FFOV  | PRDON | ERROF  | FIDSCI | FIDSCO |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

**SAA7114**

| REGISTER FUNCTION                                       | SUB<br>ADDR.<br>(HEX) | D7    | D6    | D5     | D4     | D3    | D2    | D1    | D0    |
|---------------------------------------------------------|-----------------------|-------|-------|--------|--------|-------|-------|-------|-------|
| TASK A DEFINITION: REGISTERS 90H TO BFH                 |                       |       |       |        |        |       |       |       |       |
| <i>Basic settings and acquisition window definition</i> |                       |       |       |        |        |       |       |       |       |
| Task handling control                                   | 90                    | CONLH | OFIDC | FSKP2  | FSKP1  | FSKP0 | RPTSK | STRC1 | STRC0 |
| X port formats and configuration                        | 91                    | CONLV | HLDFV | SCSRC1 | SCSRC0 | SCRQE | FSC2  | FSC1  | FSC0  |
| X port input reference signal definitions               | 92                    | XFDV  | XFDH  | XDV1   | XDV0   | XCODE | XDH   | XDQ   | XCKS  |
| I port output formats and configuration                 | 93                    | ICODE | I8_16 | FYSK   | FOI1   | FOI0  | FSI2  | FSI1  | FSI0  |
| Horizontal input window start                           | 94                    | XO7   | XO6   | XO5    | XO4    | XO3   | XO2   | XO1   | XO0   |
|                                                         | 95                    | (1)   | (1)   | (1)    | (1)    | XO11  | XO10  | XO9   | XO8   |
| Horizontal input window length                          | 96                    | XS7   | XS6   | XS5    | XS4    | XS3   | XS2   | XS1   | XS0   |
|                                                         | 97                    | (1)   | (1)   | (1)    | (1)    | XS11  | XS10  | XS9   | XS8   |
| Vertical input window start                             | 98                    | YO7   | YO6   | YO5    | YO4    | YO3   | YO2   | YO1   | YO0   |
|                                                         | 99                    | (1)   | (1)   | (1)    | (1)    | YO11  | YO10  | YO9   | YO8   |
| Vertical input window length                            | 9A                    | YS7   | YS6   | YS5    | YS4    | YS3   | YS2   | YS1   | YS0   |
|                                                         | 9B                    | (1)   | (1)   | (1)    | (1)    | YS11  | YS10  | YS9   | YS8   |
| Horizontal output window length                         | 9C                    | XD7   | XD6   | XD5    | XD4    | XD3   | XD2   | XD1   | XD0   |
|                                                         | 9D                    | (1)   | (1)   | (1)    | (1)    | XD11  | XD10  | XD9   | XD8   |
| Vertical output window length                           | 9E                    | YD7   | YD6   | YD5    | YD4    | YD3   | YD2   | YD1   | YD0   |
|                                                         | 9F                    | (1)   | (1)   | (1)    | (1)    | YD11  | YD10  | YD9   | YD8   |
| <i>FIR filtering and prescaling</i>                     |                       |       |       |        |        |       |       |       |       |
| Horizontal prescaling                                   | A0                    | (1)   | (1)   | XPSC5  | XPSC4  | XPSC3 | XPSC2 | XPSC1 | XPSC0 |
| Accumulation length                                     | A1                    | (1)   | (1)   | XACL5  | XACL4  | XACL3 | XACL2 | XACL1 | XACL0 |
| Prescaler DC gain and FIR prefilter control             | A2                    | PFUV1 | PFUV0 | PFY1   | PFY0   | XC2_1 | XDCG2 | XDCG1 | XDCG0 |
| Reserved                                                | A3                    | (1)   | (1)   | (1)    | (1)    | (1)   | (1)   | (1)   | (1)   |
| Luminance brightness control                            | A4                    | BRIG7 | BRIG6 | BRIG5  | BRIG4  | BRIG3 | BRIG2 | BRIG1 | BRIG0 |
| Luminance contrast control                              | A5                    | CONT7 | CONT6 | CONT5  | CONT4  | CONT3 | CONT2 | CONT1 | CONT0 |
| Chrominance saturation control                          | A6                    | SATN7 | SATN6 | SATN5  | SATN4  | SATN3 | SATN2 | SATN1 | SATN0 |
| Reserved                                                | A7                    | (1)   | (1)   | (1)    | (1)    | (1)   | (1)   | (1)   | (1)   |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

**SAA7114**

| REGISTER FUNCTION                           | SUB<br>ADDR.<br>(HEX) | D7     | D6     | D5     | D4     | D3     | D2     | D1    | D0    |
|---------------------------------------------|-----------------------|--------|--------|--------|--------|--------|--------|-------|-------|
| <i>Horizontal phase scaling</i>             |                       |        |        |        |        |        |        |       |       |
| Horizontal luminance scaling<br>increment   | A8                    | XSCY7  | XSCY6  | XSCY5  | XSCY4  | XSCY3  | XSCY2  | XSCY1 | XSCY0 |
|                                             | A9                    | (1)    | (1)    | (1)    | XSCY12 | XSCY11 | XSCY10 | XSCY9 | XSCY8 |
| Horizontal luminance phase<br>offset        | AA                    | XPHY7  | XPHY6  | XPHY5  | XPHY4  | XPHY3  | XPHY2  | XPHY1 | XPHY0 |
| Reserved                                    | AB                    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)   | (1)   |
| Horizontal chrominance scaling<br>increment | AC                    | XSCC7  | XSCC6  | XSCC5  | XSCC4  | XSCC3  | XSCC2  | XSCC1 | XSCC0 |
|                                             | AD                    | (1)    | (1)    | (1)    | XSCC12 | XSCC11 | XSCC10 | XSCC9 | XSCC8 |
| Horizontal chrominance phase<br>offset      | AE                    | XPHC7  | XPHC6  | XPHC5  | XPHC4  | XPHC3  | XPHC2  | XPHC1 | XPHC0 |
| Reserved                                    | AF                    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)   | (1)   |
| <i>Vertical scaling</i>                     |                       |        |        |        |        |        |        |       |       |
| Vertical luminance scaling<br>increment     | B0                    | YSCY7  | YSCY6  | YSCY5  | YSCY4  | YSCY3  | YSCY2  | YSCY1 | YSCY0 |
|                                             | B1                    | YSCY15 | YSCY14 | YSCY13 | YSCY12 | YSCY11 | YSCY10 | YSCY9 | YSCY8 |
| Vertical chrominance scaling<br>increment   | B2                    | YSCC7  | YSCC6  | YSCC5  | YSCC4  | YSCC3  | YSCC2  | YSCC1 | YSCC0 |
|                                             | B3                    | YSCC15 | YSCC14 | YSCC13 | YSCC12 | YSCC11 | YSCC10 | YSCC9 | YSCC8 |
| Vertical scaling mode control               | B4                    | (1)    | (1)    | (1)    | YMIR   | (1)    | (1)    | (1)   | YMODE |
| Reserved                                    | B5 to B7              | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)   | (1)   |
| Vertical chrominance phase<br>offset '00'   | B8                    | YPC07  | YPC06  | YPC05  | YPC04  | YPC03  | YPC02  | YPC01 | YPC00 |
| Vertical chrominance phase<br>offset '01'   | B9                    | YPC17  | YPC16  | YPC15  | YPC14  | YPC13  | YPC12  | YPC11 | YPC10 |
| Vertical chrominance phase<br>offset '10'   | BA                    | YPC27  | YPC26  | YPC25  | YPC24  | YPC23  | YPC22  | YPC21 | YPC20 |
| Vertical chrominance phase<br>offset '11'   | BB                    | YPC37  | YPC36  | YPC35  | YPC34  | YPC33  | YPC32  | YPC31 | YPC30 |
| Vertical luminance phase<br>offset '00'     | BC                    | YPY07  | YPY06  | YPY05  | YPY04  | YPY03  | YPY02  | YPY01 | YPY00 |
| Vertical luminance phase<br>offset '01'     | BD                    | YPY17  | YPY16  | YPY15  | YPY14  | YPY13  | YPY12  | YPY11 | YPY10 |
| Vertical luminance phase<br>offset '10'     | BE                    | YPY27  | YPY26  | YPY25  | YPY24  | YPY23  | YPY22  | YPY21 | YPY20 |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

**SAA7114**

| REGISTER FUNCTION                                       | SUB<br>ADDR.<br>(HEX) | D7    | D6    | D5     | D4     | D3    | D2    | D1    | D0    |
|---------------------------------------------------------|-----------------------|-------|-------|--------|--------|-------|-------|-------|-------|
| Vertical luminance phase offset '11'                    | BF                    | YPY37 | YPY36 | YPY35  | YPY34  | YPY33 | YPY32 | YPY31 | YPY30 |
| TASK B DEFINITION REGISTERS C0H TO EFH                  |                       |       |       |        |        |       |       |       |       |
| <i>Basic settings and acquisition window definition</i> |                       |       |       |        |        |       |       |       |       |
| Task handling control                                   | C0                    | CONLH | OFIDC | FSKP2  | FSKP1  | FSKP0 | RPTSK | STRC1 | STRC0 |
| X port formats and configuration                        | C1                    | CONLV | HLDFV | SCSRC1 | SCSRC0 | SCRQE | FSC2  | FSC1  | FSC0  |
| Input reference signal definition                       | C2                    | XFDV  | XFDH  | XDV1   | XDV0   | XCODE | XDH   | XDQ   | XCKS  |
| I port formats and configuration                        | C3                    | ICODE | I8_16 | FYSK   | FOI1   | FOI0  | FSI2  | FSI1  | FSI0  |
| Horizontal input window start                           | C4                    | XO7   | XO6   | XO5    | XO4    | XO3   | XO2   | XO1   | XO0   |
|                                                         | C5                    | (1)   | (1)   | (1)    | (1)    | XO11  | XO10  | XO9   | XO8   |
| Horizontal input window length                          | C6                    | XS7   | XS6   | XS5    | XS4    | XS3   | XS2   | XS1   | XS0   |
|                                                         | C7                    | (1)   | (1)   | (1)    | (1)    | XS11  | XS10  | XS9   | XS8   |
| Vertical input window start                             | C8                    | YO7   | YO6   | YO5    | YO4    | YO3   | YO2   | YO1   | YO0   |
|                                                         | C9                    | (1)   | (1)   | (1)    | (1)    | YO11  | YO10  | YO9   | YO8   |
| Vertical input window length                            | CA                    | YS7   | YS6   | YS5    | YS4    | YS3   | YS2   | YS1   | YS0   |
|                                                         | CB                    | (1)   | (1)   | (1)    | (1)    | YS11  | YS10  | YS9   | YS8   |
| Horizontal output window length                         | CC                    | XD7   | XD6   | XD5    | XD4    | XD3   | XD2   | XD1   | XD0   |
|                                                         | CD                    | (1)   | (1)   | (1)    | (1)    | XD11  | XD10  | XD9   | XD8   |
| Vertical output window length                           | CE                    | YD7   | YD6   | YD5    | YD4    | YD3   | YD2   | YD1   | YD0   |
|                                                         | CF                    | (1)   | (1)   | (1)    | (1)    | YD11  | YD10  | YD9   | YD8   |
| <i>FIR filtering and prescaling</i>                     |                       |       |       |        |        |       |       |       |       |
| Horizontal prescaling                                   | D0                    | (1)   | (1)   | XPSC5  | XPSC4  | XPSC3 | XPSC2 | XPSC1 | XPSC0 |
| Accumulation length                                     | D1                    | (1)   | (1)   | XACL5  | XACL4  | XACL3 | XACL2 | XACL1 | XACL0 |
| Prescaler DC gain and FIR prefilter control             | D2                    | PFUV1 | PFUV0 | PFY1   | PFY0   | XC2_1 | XDCG2 | XDCG1 | XDCG0 |
| Reserved                                                | D3                    | (1)   | (1)   | (1)    | (1)    | (1)   | (1)   | (1)   | (1)   |
| Luminance brightness control                            | D4                    | BRIG7 | BRIG6 | BRIG5  | BRIG4  | BRIG3 | BRIG2 | BRIG1 | BRIG0 |
| Luminance contrast control                              | D5                    | CONT7 | CONT6 | CONT5  | CONT4  | CONT3 | CONT2 | CONT1 | CONT0 |
| Chrominance saturation control                          | D6                    | SATN7 | SATN6 | SATN5  | SATN4  | SATN3 | SATN2 | SATN1 | SATN0 |
| Reserved                                                | D7                    | (1)   | (1)   | (1)    | (1)    | (1)   | (1)   | (1)   | (1)   |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| REGISTER FUNCTION                           | SUB<br>ADDR.<br>(HEX) | D7     | D6     | D5     | D4     | D3     | D2     | D1    | D0    |
|---------------------------------------------|-----------------------|--------|--------|--------|--------|--------|--------|-------|-------|
| <i>Horizontal phase scaling</i>             |                       |        |        |        |        |        |        |       |       |
| Horizontal luminance scaling<br>increment   | D8                    | XSCY7  | XSCY6  | XSCY5  | XSCY4  | XSCY3  | XSCY2  | XSCY1 | XSCY0 |
|                                             | D9                    | (1)    | (1)    | (1)    | XSCY12 | XSCY11 | XSCY10 | XSCY9 | XSCY8 |
| Horizontal luminance phase<br>offset        | DA                    | XPHY7  | XPHY6  | XPHY5  | XPHY4  | XPHY3  | XPHY2  | XPHY1 | XPHY0 |
| Reserved                                    | DB                    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)   | (1)   |
| Horizontal chrominance scaling<br>increment | DC                    | XSCC7  | XSCC6  | XSCC5  | XSCC4  | XSCC3  | XSCC2  | XSCC1 | XSCC0 |
|                                             | DD                    | (1)    | (1)    | (1)    | XSCC12 | XSCC11 | XSCC10 | XSCC9 | XSCC8 |
| Horizontal chrominance phase<br>offset      | DE                    | XPHC7  | XPHC6  | XPHC5  | XPHC4  | XPHC3  | XPHC2  | XPHC1 | XPHC0 |
| Reserved                                    | DF                    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)   | (1)   |
| <i>Vertical scaling</i>                     |                       |        |        |        |        |        |        |       |       |
| Vertical luminance scaling<br>increment     | E0                    | YSCY7  | YSCY6  | YSCY5  | YSCY4  | YSCY3  | YSCY2  | YSCY1 | YSCY0 |
|                                             | E1                    | YSCY15 | YSCY14 | YSCY13 | YSCY12 | YSCY11 | YSCY10 | YSCY9 | YSCY8 |
| Vertical chrominance scaling<br>increment   | E2                    | YSCC7  | YSCC6  | YSCC5  | YSCC4  | YSCC3  | YSCC2  | YSCC1 | YSCC0 |
|                                             | E3                    | YSCC15 | YSCC14 | YSCC13 | YSCC12 | YSCC11 | YSCC10 | YSCC9 | YSCC8 |
| Vertical scaling mode control               | E4                    | (1)    | (1)    | (1)    | YMIR   | (1)    | (1)    | (1)   | YMODE |
| Reserved                                    | E5 to E7              | (1)    | (1)    | (1)    | (1)    | (1)    | (1)    | (1)   | (1)   |
| Vertical chrominance phase<br>offset '00'   | E8                    | YPC07  | YPC06  | YPC05  | YPC04  | YPC03  | YPC02  | YPC01 | YPC00 |
| Vertical chrominance phase<br>offset '01'   | E9                    | YPC17  | YPC16  | YPC15  | YPC14  | YPC13  | YPC12  | YPC11 | YPC10 |
| Vertical chrominance phase<br>offset '10'   | EA                    | YPC27  | YPC26  | YPC25  | YPC24  | YPC23  | YPC22  | YPC21 | YPC20 |
| Vertical chrominance phase<br>offset '11'   | EB                    | YPC37  | YPC36  | YPC35  | YPC34  | YPC33  | YPC32  | YPC31 | YPC30 |
| Vertical luminance phase<br>offset '00'     | EC                    | YPY07  | YPY06  | YPY05  | YPY04  | YPY03  | YPY02  | YPY01 | YPY00 |

**PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler**

**SAA7114**

| REGISTER FUNCTION                       | SUB<br>ADDR.<br>(HEX) | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-----------------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Vertical luminance phase<br>offset '01' | ED                    | YPY17 | YPY16 | YPY15 | YPY14 | YPY13 | YPY12 | YPY11 | YPY10 |
| Vertical luminance phase<br>offset '10' | EE                    | YPY27 | YPY26 | YPY25 | YPY24 | YPY23 | YPY22 | YPY21 | YPY20 |
| Vertical luminance phase<br>offset '11' | EF                    | YPY37 | YPY36 | YPY35 | YPY34 | YPY33 | YPY32 | YPY31 | YPY30 |

**Note**

1. All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2 I<sup>2</sup>C-bus details

### 15.2.1 SUBADDRESS 00H

**Table 39** Chip Version (CV) identification; 00H[7:4]; read only register

| FUNCTION          | LOGIC LEVELS |     |     |     |
|-------------------|--------------|-----|-----|-----|
|                   | ID7          | ID6 | ID5 | ID4 |
| Chip Version (CV) | CV3          | CV2 | CV1 | CV0 |

### 15.2.2 SUBADDRESS 01H

The programming of the horizontal increment delay is used to match internal processing delays to the delay of the ADC. Use recommended position only.

**Table 40** Horizontal increment delay; 01H[3:0]

| FUNCTION                    | IDEL3    | IDEL2    | IDEL1    | IDEL0    |
|-----------------------------|----------|----------|----------|----------|
| No update                   | 1        | 1        | 1        | 1        |
| Minimum delay               | 1        | 1        | 1        | 0        |
| <b>Recommended position</b> | <b>1</b> | <b>0</b> | <b>0</b> | <b>0</b> |
| Maximum delay               | 0        | 0        | 0        | 0        |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.3 SUBADDRESS 02H

**Table 41** Analog input control 1 (AICO1); 02H[7:0]

| BIT    | DESCRIPTION                                    | SYMBOL    | VALUE        | FUNCTION                                                                                                           |
|--------|------------------------------------------------|-----------|--------------|--------------------------------------------------------------------------------------------------------------------|
| D[7:6] | analog function select;<br>see Fig.7           | FUSE[1:0] | 00           | amplifier plus anti-alias filter bypassed                                                                          |
|        |                                                |           | 01           |                                                                                                                    |
|        |                                                |           | 10           | amplifier active                                                                                                   |
|        |                                                |           | 11           | amplifier plus anti-alias filter active                                                                            |
| D[5:4] | update hysteresis for<br>9-bit gain; see Fig.8 | GUDL[1:0] | 00           | off                                                                                                                |
|        |                                                |           | 01           | ±1 LSB                                                                                                             |
|        |                                                |           | 10           | ±2 LSB                                                                                                             |
|        |                                                |           | 11           | ±3 LSB                                                                                                             |
| D[3:0] | mode selection                                 | MODE[3:0] | 0000         | <b>Mode 0:</b> CVBS (automatic gain) from AI11; see Fig.44                                                         |
|        |                                                |           | 0001         | <b>Mode 1:</b> CVBS (automatic gain) from AI12; see Fig.45                                                         |
|        |                                                |           | 0010         | <b>Mode 2:</b> CVBS (automatic gain) from AI21; see Fig.46                                                         |
|        |                                                |           | 0011         | <b>Mode 3:</b> CVBS (automatic gain) from AI22; see Fig.47                                                         |
|        |                                                |           | 0100         | <b>Mode 4:</b> CVBS (automatic gain) from AI23; see Fig.48                                                         |
|        |                                                |           | 0101         | <b>Mode 5:</b> CVBS (automatic gain) from AI24; see Fig.49                                                         |
|        |                                                |           | 0110         | <b>Mode 6:</b> Y (automatic gain) from AI11 + C (gain adjustable via GAI28 to GAI20) from AI21; note 1; see Fig.50 |
|        |                                                |           | 0111         | <b>Mode 7:</b> Y (automatic gain) from AI12 + C (gain adjustable via GAI28 to GAI20) from AI22; note 1; see Fig.51 |
|        |                                                |           | 1000         | <b>Mode 8:</b> Y (automatic gain) from AI11 + C (gain adapted to Y gain) from AI21; note 1; see Fig.52             |
|        |                                                |           | 1001         | <b>Mode 9:</b> Y (automatic gain) from AI12 + C (gain adapted to Y gain) from AI22; note 1; see Fig.53             |
|        |                                                |           | 1010 to 1111 | <b>Modes 10 to 15:</b> reserved                                                                                    |

**Note**

1. To take full advantage of the Y/C modes 6 to 9 the I<sup>2</sup>C-bus bit BYPS (subaddress 09H, bit D7) should be set to logic 1 (full luminance bandwidth).

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

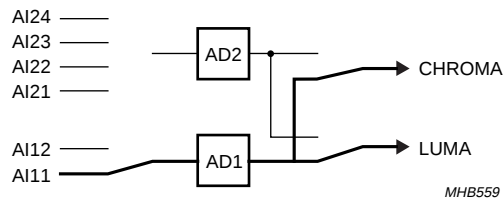


Fig.44 **Mode 0** CVBS (automatic gain)

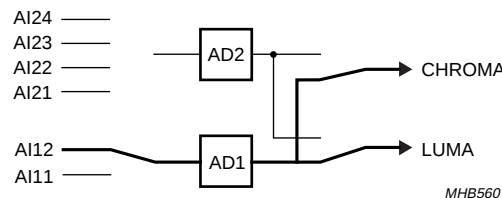


Fig.45 **Mode 1** CVBS (automatic gain).

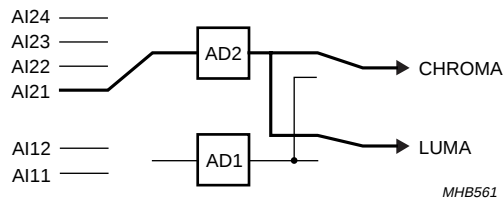


Fig.46 **Mode 2** CVBS (automatic gain).

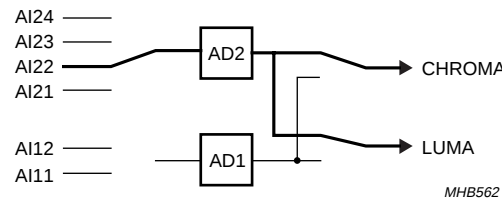


Fig.47 **Mode 3** CVBS (automatic gain).

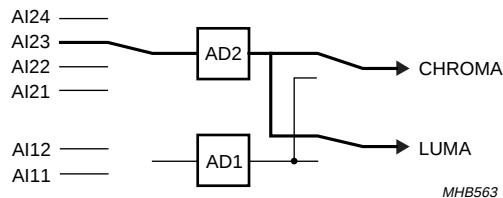


Fig.48 **Mode 4** CVBS (automatic gain).

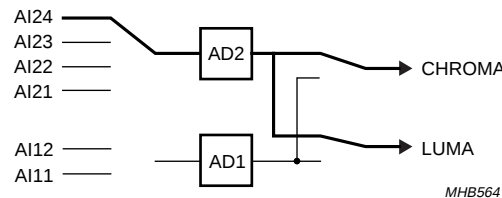
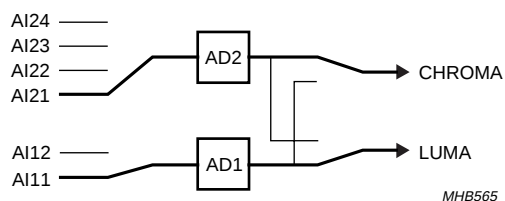


Fig.49 **Mode 5** CVBS (automatic gain).

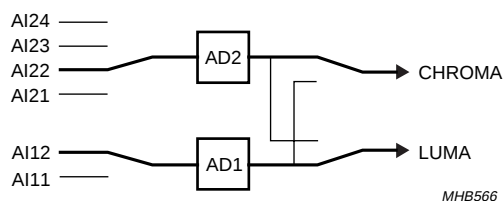
# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114



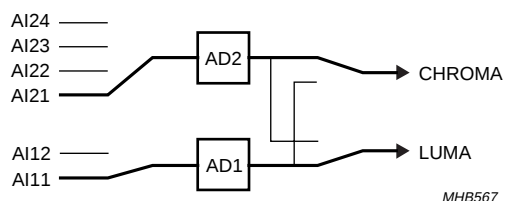
I<sup>2</sup>C-bus bit BYPS (subaddress 09H, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig.50 **Mode 6** Y + C (gain channel 2 adjusted via GAI2).



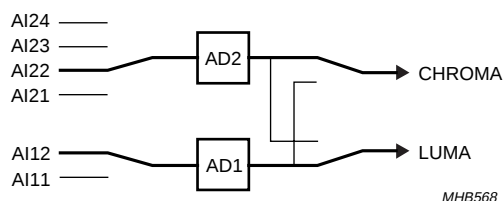
I<sup>2</sup>C-bus bit BYPS (subaddress 09H, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig.51 **Mode 7** Y + C (gain channel 2 adjusted via GAI2).



I<sup>2</sup>C-bus bit BYPS (subaddress 09H, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig.52 **Mode 8** Y + C (gain channel 2 adapted to Y gain).



I<sup>2</sup>C-bus bit BYPS (subaddress 09H, bit D7) should be set to logic 1 (full luminance bandwidth).

Fig.53 **Mode 9** Y + C (gain channel 2 adapted to Y gain).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.4 SUBADDRESS 03H

**Table 42** Analog input control 2 (AICO2); 03H[6:0]

| BIT | DESCRIPTION                              | SYMBOL | VALUE            | FUNCTION                                                                                                                                       |
|-----|------------------------------------------|--------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| D6  | HL not reference select                  | HLNRS  | 0                | normal clamping if decoder is in unlocked state                                                                                                |
|     |                                          |        | 1 <sup>(1)</sup> | reference select if decoder is in unlocked state                                                                                               |
| D5  | AGC hold during vertical blanking period | VBSL   | 0                | short vertical blanking (AGC disabled during equalization and serration pulses)                                                                |
|     |                                          |        | 1                | long vertical blanking (AGC disabled from start of pre-equalization pulses until start of active video (line 22 for 60 Hz, line 24 for 50 Hz)) |
| D4  | white peak control off                   | WPOFF  | 0 <sup>(1)</sup> | white peak control active                                                                                                                      |
|     |                                          |        | 1                | white peak control off                                                                                                                         |
| D3  | automatic gain control integration       | HOLDG  | 0                | AGC active                                                                                                                                     |
|     |                                          |        | 1                | AGC integration hold (freeze)                                                                                                                  |
| D2  | gain control fix                         | GAFIX  | 0                | automatic gain controlled by MODE3 to MODE0                                                                                                    |
|     |                                          |        | 1                | gain is user programmable via GAI[17:10] and GAI[27:20]                                                                                        |
| D1  | static gain control channel 2 sign bit   | GAI28  | see Table 44     |                                                                                                                                                |
| D0  | static gain control channel 1 sign bit   | GAI18  | see Table 43     |                                                                                                                                                |

**Note**

1. HLNRS = 1 should not be used in combination with WPOFF = 0.

## 15.2.5 SUBADDRESS 04H

**Table 43** Analog input control 3 (AICO3): static gain control channel 1; 03H[0] and 04H[7:0]

| DECIMAL VALUE | GAIN (dB) | SIGN BIT 03H[0] | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|---------------|-----------|-----------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|               |           | GAI18           | GAI17                 | GAI16 | GAI15 | GAI14 | GAI13 | GAI12 | GAI11 | GAI10 |
| 0...          | −3        | 0               | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| ...144        | 0         | 0               | 1                     | 0     | 0     | 1     | 0     | 0     | 0     | 0     |
| 145...        | 0         | 0               | 1                     | 0     | 0     | 1     | 0     | 0     | 0     | 1     |
| ...511        | +6        | 1               | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

## 15.2.6 SUBADDRESS 05H

**Table 44** Analog input control 4 (AICO4); static gain control channel 2; 03H[1] and 05H[7:0]

| DECIMAL VALUE | GAIN (dB) | SIGN BIT 03H[1] | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|---------------|-----------|-----------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|               |           | GAI28           | GAI27                 | GAI26 | GAI25 | GAI24 | GAI23 | GAI22 | GAI21 | GAI20 |
| 0...          | −3        | 0               | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| ...144        | 0         | 0               | 1                     | 0     | 0     | 1     | 0     | 0     | 0     | 0     |
| 145...        | 0         | 0               | 1                     | 0     | 0     | 1     | 0     | 0     | 0     | 1     |
| ...511        | +6        | 1               | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.7 SUBADDRESS 06H

**Table 45** Horizontal sync start; 06H[7:0]

| DELAY TIME<br>(STEP SIZE = 8/LLC) | CONTROL BITS D7 TO D0                               |      |      |      |      |      |      |      |
|-----------------------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
|                                   | HSB7                                                | HSB6 | HSB5 | HSB4 | HSB3 | HSB2 | HSB1 | HSB0 |
| –128...–109 (50 Hz)               | forbidden (outside available central counter range) |      |      |      |      |      |      |      |
| –128...–108 (60 Hz)               |                                                     |      |      |      |      |      |      |      |
| –108 (50 Hz)...                   | 1                                                   | 0    | 0    | 1    | 0    | 1    | 0    | 0    |
| –107 (60 Hz)...                   | 1                                                   | 0    | 0    | 1    | 0    | 1    | 0    | 1    |
| ...108 (50 Hz)                    | 0                                                   | 1    | 1    | 0    | 1    | 1    | 0    | 0    |
| ...107 (60 Hz)                    | 0                                                   | 1    | 1    | 0    | 1    | 0    | 1    | 1    |
| 109...127 (50 Hz)                 | forbidden (outside available central counter range) |      |      |      |      |      |      |      |
| 108...127 (60 Hz)                 |                                                     |      |      |      |      |      |      |      |

## 15.2.8 SUBADDRESS 07H

**Table 46** Horizontal sync stop; 07H[7:0]

| DELAY TIME<br>(STEP SIZE = 8/LLC) | CONTROL BITS D7 TO D0                               |      |      |      |      |      |      |      |
|-----------------------------------|-----------------------------------------------------|------|------|------|------|------|------|------|
|                                   | HSS7                                                | HSS6 | HSS5 | HSS4 | HSS3 | HSS2 | HSS1 | HSS0 |
| –128...–109 (50 Hz)               | forbidden (outside available central counter range) |      |      |      |      |      |      |      |
| –128...–108 (60 Hz)               |                                                     |      |      |      |      |      |      |      |
| –108 (50 Hz)...                   | 1                                                   | 0    | 0    | 1    | 0    | 1    | 0    | 0    |
| –107 (60 Hz)...                   | 1                                                   | 0    | 0    | 1    | 0    | 1    | 0    | 1    |
| ...108 (50 Hz)                    | 0                                                   | 1    | 1    | 0    | 1    | 1    | 0    | 0    |
| ...107 (60 Hz)                    | 0                                                   | 1    | 1    | 0    | 1    | 0    | 1    | 1    |
| 109...127 (50 Hz)                 | forbidden (outside available central counter range) |      |      |      |      |      |      |      |
| 108...127 (60 Hz)                 |                                                     |      |      |      |      |      |      |      |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.9 SUBADDRESS 08H

**Table 47** Sync control; 08H[7:0]

| BIT    | DESCRIPTION                         | SYMBOL    | VALUE | FUNCTION                                                                                                |
|--------|-------------------------------------|-----------|-------|---------------------------------------------------------------------------------------------------------|
| D7     | automatic field detection           | AUFD      | 0     | field state directly controlled via FSEL                                                                |
|        |                                     |           | 1     | automatic field detection; <b>recommended setting</b>                                                   |
| D6     | field selection; active if AUFD = 0 | FSEL      | 0     | 50 Hz, 625 lines                                                                                        |
|        |                                     |           | 1     | 60 Hz, 525 lines                                                                                        |
| D5     | forced ODD/EVEN toggle              | FOET      | 0     | ODD/EVEN signal toggles only with interlaced source                                                     |
|        |                                     |           | 1     | ODD/EVEN signal toggles fieldwise even if source is non-interlaced                                      |
| D[4:3] | horizontal time constant selection  | HTC[1:0]  | 00    | TV mode, recommended for poor quality TV signals only; do not use for new applications                  |
|        |                                     |           | 01    | VTR mode, recommended if a deflection control circuit is directly connected to the SAA7114              |
|        |                                     |           | 10    | reserved                                                                                                |
|        |                                     |           | 11    | fast locking mode; <b>recommended setting</b>                                                           |
| D2     | horizontal PLL                      | HPLL      | 0     | PLL closed                                                                                              |
|        |                                     |           | 1     | PLL open; horizontal frequency fixed                                                                    |
| D[1:0] | vertical noise reduction            | VNOI[1:0] | 00    | normal mode; <b>recommended setting</b>                                                                 |
|        |                                     |           | 01    | fast mode, applicable for stable sources only; automatic field detection (AUFD) <b>must</b> be disabled |
|        |                                     |           | 10    | free running mode                                                                                       |
|        |                                     |           | 11    | vertical noise reduction bypassed                                                                       |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.10 SUBADDRESS 09H

**Table 48** Luminance control; 09H[7:0]

| BIT    | DESCRIPTION                                                    | SYMBOL   | VALUE | FUNCTION                                                                                    |
|--------|----------------------------------------------------------------|----------|-------|---------------------------------------------------------------------------------------------|
| D7     | chrominance trap/comb filter bypass                            | BYPS     | 0     | chrominance trap or luminance comb filter active; default for CVBS mode                     |
|        |                                                                |          | 1     | chrominance trap or luminance comb filter bypassed; default for S-video mode                |
| D6     | adaptive luminance comb filter                                 | YCOMB    | 0     | disabled (= chrominance trap enabled, if BYPS = 0)                                          |
|        |                                                                |          | 1     | active, if BYPS = 0                                                                         |
| D5     | processing delay in non comb filter mode                       | LDEL     | 0     | processing delay is equal to internal pipelining delay                                      |
|        |                                                                |          | 1     | one (NTSC standards) or two (PAL standards) video lines additional processing delay         |
| D4     | remodulation bandwidth for luminance; see Figs 13 to 16        | LUBW     | 0     | small remodulation bandwidth (narrow chroma notch $\Rightarrow$ higher luminance bandwidth) |
|        |                                                                |          | 1     | large remodulation bandwidth (wider chroma notch $\Rightarrow$ smaller luminance bandwidth) |
| D[3:0] | sharpness control, luminance filter characteristic; see Fig.17 | LUF[3:0] | 0001  | resolution enhancement filter 8.0 dB at 4.1 MHz                                             |
|        |                                                                |          | 0010  | resolution enhancement filter 6.8 dB at 4.1 MHz                                             |
|        |                                                                |          | 0011  | resolution enhancement filter 5.1 dB at 4.1 MHz                                             |
|        |                                                                |          | 0100  | resolution enhancement filter 4.1 dB at 4.1 MHz                                             |
|        |                                                                |          | 0101  | resolution enhancement filter 3.0 dB at 4.1 MHz                                             |
|        |                                                                |          | 0110  | resolution enhancement filter 2.3 dB at 4.1 MHz                                             |
|        |                                                                |          | 0111  | resolution enhancement filter 1.6 dB at 4.1 MHz                                             |
|        |                                                                |          | 0000  | plain                                                                                       |
|        |                                                                |          | 1000  | low-pass filter 2 dB at 4.1 MHz                                                             |
|        |                                                                |          | 1001  | low-pass filter 3 dB at 4.1 MHz                                                             |
|        |                                                                |          | 1010  | low-pass filter 3 dB at 3.3 MHz; 4 dB at 4.1 MHz                                            |
|        |                                                                |          | 1011  | low-pass filter 3 dB at 2.6 MHz; 8 dB at 4.1 MHz                                            |
|        |                                                                |          | 1100  | low-pass filter 3 dB at 2.4 MHz; 14 dB at 4.1 MHz                                           |
|        |                                                                |          | 1101  | low-pass filter 3 dB at 2.2 MHz; notch at 3.4 MHz                                           |
|        |                                                                |          | 1110  | low-pass filter 3 dB at 1.9 MHz; notch at 3.0 MHz                                           |
|        |                                                                |          | 1111  | low-pass filter 3 dB at 1.7 MHz; notch at 2.5 MHz                                           |

## 15.2.11 SUBADDRESS 0AH

**Table 49** Luminance brightness control: decoder part; 0AH[7:0]

| OFFSET          | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|-----------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                 | DBRI7                 | DBRI6 | DBRI5 | DBRI4 | DBRI3 | DBRI2 | DBRI1 | DBRI0 |
| 255 (bright)    | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| 128 (ITU level) | 1                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 0 (dark)        | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.12 SUBADDRESS 0BH

**Table 50** Luminance contrast control: decoder part; 0BH[7:0]

| GAIN                   | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                        | DCON7                 | DCON6 | DCON5 | DCON4 | DCON3 | DCON2 | DCON1 | DCON0 |
| 1.984 (maximum)        | 0                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| 1.063 (ITU level)      | 0                     | 1     | 0     | 0     | 0     | 1     | 0     | 0     |
| 1.0                    | 0                     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| 0 (luminance off)      | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| −1 (inverse luminance) | 1                     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| −2 (inverse luminance) | 1                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

## 15.2.13 SUBADDRESS 0CH

**Table 51** Chrominance saturation control: decoder part; 0CH[7:0]

| GAIN                     | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|--------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                          | DSAT7                 | DSAT6 | DSAT5 | DSAT4 | DSAT3 | DSAT2 | DSAT1 | DSAT0 |
| 1.984 (maximum)          | 0                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| 1.0 (ITU level)          | 0                     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| 0 (colour off)           | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| −1 (inverse chrominance) | 1                     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| −2 (inverse chrominance) | 1                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

## 15.2.14 SUBADDRESS 0DH

**Table 52** Chrominance hue control; 0DH[7:0]

| HUE PHASE (DEG) | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|-----------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                 | HUEC7                 | HUEC6 | HUEC5 | HUEC4 | HUEC3 | HUEC2 | HUEC1 | HUEC0 |
| +178.6...       | 0                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| ...0...         | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| ...−180         | 1                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.15 SUBADDRESS 0EH

**Table 53** Chrominance control 1; 0EH[7:0]

| BIT    | DESCRIPTION                                                        | SYMBOL    | VALUE | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                |                       |
|--------|--------------------------------------------------------------------|-----------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
|        |                                                                    |           |       | 50 Hz/625 LINES                                                                                                                                                                                                                                                                                                                                                                                                                         | 60 Hz/525 LINES       |
| D7     | clear DTO                                                          | CDTO      | 0     | disabled                                                                                                                                                                                                                                                                                                                                                                                                                                |                       |
|        |                                                                    |           | 1     | Every time CDTO is set, the internal subcarrier DTO phase is reset to 0° and the RTCO output generates a logic 0 at time slot 68 (see document “ <i>RTC Functional Description</i> ”, available on request). So an identical subcarrier phase can be generated by an external device (e.g. an encoder); if a DTO reset is programmed via CDTO it has always to be executed in the following way:<br>1. Set CDTO = 0<br>2. Set CDTO = 1. |                       |
| D[6:4] | colour standard selection                                          | CSTD[2:0] | 000   | PAL BGDHI (4.43 MHz)                                                                                                                                                                                                                                                                                                                                                                                                                    | NTSC M (3.58 MHz)     |
|        |                                                                    |           | 001   | NTSC 4.43 (50 Hz)                                                                                                                                                                                                                                                                                                                                                                                                                       | PAL 4.43 (60 Hz)      |
|        |                                                                    |           | 010   | Combination-PAL N (3.58 MHz)                                                                                                                                                                                                                                                                                                                                                                                                            | NTSC 4.43 (60 Hz)     |
|        |                                                                    |           | 011   | NTSC N (3.58 MHz)                                                                                                                                                                                                                                                                                                                                                                                                                       | PAL M (3.58 MHz)      |
|        |                                                                    |           | 100   | reserved                                                                                                                                                                                                                                                                                                                                                                                                                                | NTSC-Japan (3.58 MHz) |
|        |                                                                    |           | 101   | SECAM                                                                                                                                                                                                                                                                                                                                                                                                                                   | reserved              |
|        |                                                                    |           | 110   | reserved; <b>do not use</b>                                                                                                                                                                                                                                                                                                                                                                                                             |                       |
|        |                                                                    |           | 111   | reserved; <b>do not use</b>                                                                                                                                                                                                                                                                                                                                                                                                             |                       |
| D3     | disable chrominance vertical filter and PAL phase error correction | DCVF      | 0     | chrominance vertical filter and PAL phase error correction on (during active video lines)                                                                                                                                                                                                                                                                                                                                               |                       |
|        |                                                                    |           | 1     | chrominance vertical filter and PAL phase error correction permanently off                                                                                                                                                                                                                                                                                                                                                              |                       |
| D2     | fast colour time constant                                          | FCTC      | 0     | nominal time constant                                                                                                                                                                                                                                                                                                                                                                                                                   |                       |
|        |                                                                    |           | 1     | fast time constant for special applications (high quality input source, fast chroma lock required, automatic standard detection off)                                                                                                                                                                                                                                                                                                    |                       |
| D0     | adaptive chrominance comb filter                                   | CCOMB     | 0     | disabled                                                                                                                                                                                                                                                                                                                                                                                                                                |                       |
|        |                                                                    |           | 1     | active                                                                                                                                                                                                                                                                                                                                                                                                                                  |                       |

## 15.2.16 SUBADDRESS 0FH

**Table 54** Chrominance gain control; 0FH[7:0]

| BIT    | DESCRIPTION                                        | SYMBOL     | VALUE    | FUNCTION                                                                  |
|--------|----------------------------------------------------|------------|----------|---------------------------------------------------------------------------|
| D7     | automatic chrominance gain control                 | ACGC       | 0        | on                                                                        |
|        |                                                    |            | 1        | programmable gain via CGAIN6 to CGAIN0; need to be set for SECAM standard |
| D[6:0] | chrominance gain value (if ACGC is set to logic 1) | CGAIN[6:0] | 000 0000 | minimum gain (0.5)                                                        |
|        |                                                    |            | 010 0100 | nominal gain (1.125)                                                      |
|        |                                                    |            | 111 1111 | maximum gain (7.5)                                                        |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.17 SUBADDRESS 10H

**Table 55** Chrominance control 2; 10H[7:0]

| BIT    | DESCRIPTION                                                            | SYMBOL    | VALUE | FUNCTION                                                   |
|--------|------------------------------------------------------------------------|-----------|-------|------------------------------------------------------------|
| D[7:6] | fine offset adjustment B – Y component                                 | OFFU[1:0] | 00    | 0 LSB                                                      |
|        |                                                                        |           | 01    | $\frac{1}{4}$ LSB                                          |
|        |                                                                        |           | 10    | $\frac{1}{2}$ LSB                                          |
|        |                                                                        |           | 11    | $\frac{3}{4}$ LSB                                          |
| D[5:4] | fine offset adjustment R – Y component                                 | OFFV[1:0] | 00    | 0 LSB                                                      |
|        |                                                                        |           | 01    | $\frac{1}{4}$ LSB                                          |
|        |                                                                        |           | 10    | $\frac{1}{2}$ LSB                                          |
|        |                                                                        |           | 11    | $\frac{3}{4}$ LSB                                          |
| D3     | chrominance bandwidth; see Figs 11 and 12                              | CHBW      | 0     | small                                                      |
|        |                                                                        |           | 1     | wide                                                       |
| D[2:0] | combined luminance/chrominance bandwidth adjustment; see Figs 11 to 17 | LCBW[2:0] | 000   | smallest chrominance bandwidth/largest luminance bandwidth |
|        |                                                                        |           | ...   | ... to ...                                                 |
|        |                                                                        |           | 111   | largest chrominance bandwidth/smallest luminance bandwidth |

## 15.2.18 SUBADDRESS 11H

**Table 56** Mode/delay control; 11H[7:0]

| BIT    | DESCRIPTION                                   | SYMBOL    | VALUE | FUNCTION                        |
|--------|-----------------------------------------------|-----------|-------|---------------------------------|
| D7     | colour on                                     | COLO      | 0     | automatic colour killer enabled |
|        |                                               |           | 1     | colour forced on                |
| D6     | polarity of RTS1 output signal                | RTP1      | 0     | non-inverted                    |
|        |                                               |           | 1     | inverted                        |
| D[5:4] | fine position of HS (steps in 2/LLC)          | HDEL[1:0] | 00    | 0                               |
|        |                                               |           | 01    | 1                               |
|        |                                               |           | 10    | 2                               |
|        |                                               |           | 11    | 3                               |
| D3     | polarity of RTS0 output signal                | RTP0      | 0     | non-inverted                    |
|        |                                               |           | 1     | inverted                        |
| D[2:0] | luminance delay compensation (steps in 2/LLC) | YDEL[2:0] | 100   | –4...                           |
|        |                                               |           | 000   | ...0...                         |
|        |                                               |           | 011   | ...3                            |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.19 SUBADDRESS 12H

**Table 57** RT signal control: RTS0 output; 12H[3:0]

The polarity of any signal on RTS0 can be inverted via RTP0[11H[3]].

| RTS0 OUTPUT                                                                                                                                                                                                                       | RTSE03 | RTSE02 | RTSE01 | RTSE00 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| 3-state                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
| Constant LOW                                                                                                                                                                                                                      | 0      | 0      | 0      | 1      |
| CREF (13.5 MHz toggling pulse; see Fig.24)                                                                                                                                                                                        | 0      | 0      | 1      | 0      |
| CREF2 (6.75 MHz toggling pulse; see Fig.24)                                                                                                                                                                                       | 0      | 0      | 1      | 1      |
| HL; horizontal lock indicator (note 1):<br>HL = 0: unlocked<br>HL = 1: locked                                                                                                                                                     | 0      | 1      | 0      | 0      |
| VL; vertical and horizontal lock:<br>VL = 0: unlocked<br>VL = 1: locked                                                                                                                                                           | 0      | 1      | 0      | 1      |
| DL; vertical and horizontal lock and colour detected:<br>DL = 0: unlocked<br>DL = 1: locked                                                                                                                                       | 0      | 1      | 1      | 0      |
| Reserved                                                                                                                                                                                                                          | 0      | 1      | 1      | 1      |
| HREF, horizontal reference signal; indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval (see Fig.24). | 1      | 0      | 0      | 0      |
| HS:<br>programmable width in LLC8 steps via HSB[7:0] 06H[7:0] and HSS[7:0] 07H[7:0]<br>fine position adjustment in LLC2 steps via HDEL[1:0] 11H[5:4]<br>(see Fig.24)                                                              | 1      | 0      | 0      | 1      |
| HQ; HREF gated with VGATE                                                                                                                                                                                                         | 1      | 0      | 1      | 0      |
| Reserved                                                                                                                                                                                                                          | 1      | 0      | 1      | 1      |
| V123; vertical sync (see vertical timing diagrams Figs 22 and 23)                                                                                                                                                                 | 1      | 1      | 0      | 0      |
| VGATE; programmable via VSTA[8:0] 17H[0] 15H[7:0], VSTO[8:0] 17H[1] 16H[7:0] and VGPS[17H[2]]                                                                                                                                     | 1      | 1      | 0      | 1      |
| LSBs of the 9-bit ADC's                                                                                                                                                                                                           | 1      | 1      | 1      | 0      |
| FID; position programmable via VSTA[8:0] 17H[0] 15H[7:0]; see vertical timing diagrams Figs 22 and 23                                                                                                                             | 1      | 1      | 1      | 1      |

### Note

1. Function of HL is selectable via HLSEL[13H[3]]:
  - a) HLSEL = 0: HL is standard horizontal lock indicator.
  - b) HLSEL = 1: HL is fast horizontal lock indicator (use is not recommended for sources with unstable timebase e.g. VCRs).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 58** RT signal control: RTS1 output; 12H[7:4]

The polarity of any signal on RTS1 can be inverted via RTP1[11H[6]].

| RTS1 OUTPUT                                                                                                                                                                                                                       | RTSE13 | RTSE12 | RTSE11 | RTSE10 |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|
| 3-state                                                                                                                                                                                                                           | 0      | 0      | 0      | 0      |
| Constant LOW                                                                                                                                                                                                                      | 0      | 0      | 0      | 1      |
| CREF (13.5 MHz toggling pulse; see Fig.24)                                                                                                                                                                                        | 0      | 0      | 1      | 0      |
| CREF2 (6.75 MHz toggling pulse; see Fig.24)                                                                                                                                                                                       | 0      | 0      | 1      | 1      |
| HL; horizontal lock indicator (note 1):<br>HL = 0: unlocked<br>HL = 1: locked                                                                                                                                                     | 0      | 1      | 0      | 0      |
| VL; vertical and horizontal lock:<br>VL = 0: unlocked<br>VL = 1: locked                                                                                                                                                           | 0      | 1      | 0      | 1      |
| DL; vertical and horizontal lock and colour detected:<br>DL = 0: unlocked<br>DL = 1: locked                                                                                                                                       | 0      | 1      | 1      | 0      |
| Reserved                                                                                                                                                                                                                          | 0      | 1      | 1      | 1      |
| HREF, horizontal reference signal; indicates 720 pixels valid data on the expansion port. The positive slope marks the beginning of a new active line. HREF is also generated during the vertical blanking interval (see Fig.24). | 1      | 0      | 0      | 0      |
| HS:<br>programmable width in LLC8 steps via HSB[7:0] 06H[7:0] and HSS[7:0] 07H[7:0]<br>fine position adjustment in LLC2 steps via HDEL[1:0] 11H[5:4]<br>(see Fig.24)                                                              | 1      | 0      | 0      | 1      |
| HQ; HREF gated with VGATE                                                                                                                                                                                                         | 1      | 0      | 1      | 0      |
| Reserved                                                                                                                                                                                                                          | 1      | 0      | 1      | 1      |
| V123; vertical sync (see vertical timing diagrams Figs 22 and 23)                                                                                                                                                                 | 1      | 1      | 0      | 0      |
| VGATE; programmable via VSTA[8:0] 17H[0] 15H[7:0], VSTO[8:0] 17H[1] 16H[7:0] and VGPS[17H[2]]                                                                                                                                     | 1      | 1      | 0      | 1      |
| Reserved                                                                                                                                                                                                                          | 1      | 1      | 1      | 0      |
| FID; position programmable via VSTA[8:0] 17H[0] 15H[7:0]; see vertical timing diagrams Figs 22 and 23                                                                                                                             | 1      | 1      | 1      | 1      |

**Note**

1. Function of HL is selectable via HLSEL[13H[3]]:
  - a) HLSEL = 0: HL is standard horizontal lock indicator.
  - b) HLSEL = 1: HL is fast horizontal lock indicator (use is not recommended for sources with unstable timebase e.g. VCRs).

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.20 SUBADDRESS 13H

**Table 59** RT/X port output control; 13H[7:0]

| BIT    | DESCRIPTION                                                  | SYMBOL    | VALUE | FUNCTION                                                                                                                                                                            |
|--------|--------------------------------------------------------------|-----------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D7     | RTCO output enable                                           | RTCE      | 0     | 3-state                                                                                                                                                                             |
|        |                                                              |           | 1     | enabled                                                                                                                                                                             |
| D6     | X port XRH output selection                                  | XRHS      | 0     | HREF (see Fig.24)                                                                                                                                                                   |
|        |                                                              |           | 1     | HS:<br>programmable width in LLC8 steps via HSB[7:0] 06H[7:0] and HSS[7:0] 07H[7:0]<br>fine position adjustment in LLC2 steps via HDEL[1:0] 11H[5:4] (see Fig.24)                   |
| D[5:4] | X port XRV output selection                                  | XRVS[1:0] | 00    | V123 (see Figs 22 and 23)                                                                                                                                                           |
|        |                                                              |           | 01    | ITU 656 related field ID (see Figs 22 and 23)                                                                                                                                       |
|        |                                                              |           | 10    | inverted V123                                                                                                                                                                       |
|        |                                                              |           | 11    | inverted ITU 656 related field ID                                                                                                                                                   |
| D3     | horizontal lock indicator selection                          | HLSEL     | 0     | copy of inverted HLCK status bit (default)                                                                                                                                          |
|        |                                                              |           | 1     | fast horizontal lock indicator (for special applications only)                                                                                                                      |
| D[2:0] | XPD7 to XPD0 (port output format selection); see Section 9.4 | OFTS[2:0] | 000   | ITU 656                                                                                                                                                                             |
|        |                                                              |           | 001   | ITU 656 like format with modified field blanking according to VGATE position (programmable via VSTA[8:0] 17H[0] 15H[7:0], VSTO[8:0] 17H[1] 16H[7:0] and VGPS[17H[2]])               |
|        |                                                              |           | 010   | Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 8-bit format (no SAV/EAV codes inserted)                                                                                                 |
|        |                                                              |           | 011   | reserved                                                                                                                                                                            |
|        |                                                              |           | 100   | multiplexed AD2/AD1 bypass (bits D8 to D1) dependent on mode settings (see Section 15.2.3); if both ADCs are selected AD2 is output at CREF = 1 and AD1 is output at CREF = 0       |
|        |                                                              |           | 101   | multiplexed AD2/AD1 bypass (bits D7 to D0) dependent on mode settings (see Section 15.2.3); if both ADCs are selected AD2 is output at CREF = 1 and AD1 is output at CREF = 0       |
|        |                                                              |           | 110   | reserved                                                                                                                                                                            |
|        |                                                              |           | 111   | multiplexed ADC MSB/LSB bypass dependent on mode settings; only one ADC should be selected at a time; ADx8 to ADx1 are outputs at CREF = 1 and ADx7 to ADx0 are outputs at CREF = 0 |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.21 SUBADDRESS 14H

**Table 60** Analog/ADC/compatibility control; 14H[7:0]

| BIT    | DESCRIPTION                                 | SYMBOL    | VALUE | FUNCTION                                                                                              |
|--------|---------------------------------------------|-----------|-------|-------------------------------------------------------------------------------------------------------|
| D7     | compatibility bit for SAA7199               | CM99      | 0     | off (default)                                                                                         |
|        |                                             |           | 1     | on (to be set <b>only</b> if SAA7199 is used for re-encoding <b>in conjunction with RTCO active</b> ) |
| D6     | update time interval for AGC value          | UPTCV     | 0     | horizontal update (once per line)                                                                     |
|        |                                             |           | 1     | vertical update (once per field)                                                                      |
| D[5:4] | analog test select                          | AOSL[1:0] | 00    | AOUT connected to internal test point 1                                                               |
|        |                                             |           | 01    | AOUT connected to input AD1                                                                           |
|        |                                             |           | 10    | AOUT connected to input AD2                                                                           |
|        |                                             |           | 11    | AOUT connected to internal test point 2                                                               |
| D3     | XTOUT output enable                         | XTOUTE    | 0     | XTOUT 3-stated                                                                                        |
|        |                                             |           | 1     | XTOUT enabled                                                                                         |
| D2     | decoder status byte selection; see Table 66 | OLDSB     | 0     | standard                                                                                              |
|        |                                             |           | 1     | backward compatibility to SAA7112                                                                     |
| D[1:0] | ADC sample clock phase delay                | APCK[1:0] | 00    | application dependent                                                                                 |
|        |                                             |           | 01    |                                                                                                       |
|        |                                             |           | 10    |                                                                                                       |
|        |                                             |           | 11    |                                                                                                       |

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SAA7114

15.2.22 SUBADDRESS 15H

**Table 61** VGATE start; FID polarity change; 17H[0] and 15H[7:0]  
Start of VGATE pulse (LOW-to-HIGH transition) and polarity change of FID pulse, VGPS = 0; see Figs 22 and 23.

| FIELD |     | FRAME LINE<br>COUNTING | DECIMAL<br>VALUE | MSB<br>17H[0] | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|-------|-----|------------------------|------------------|---------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|       |     |                        |                  | VSTA8         | VSTA7                 | VSTA6 | VSTA5 | VSTA4 | VSTA3 | VSTA2 | VSTA1 | VSTA0 |
| 50 Hz | 1st | 1                      | 312              | 1             | 0                     | 0     | 1     | 1     | 1     | 0     | 0     | 0     |
|       | 2nd | 314                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 2                      | 0...             | 0             | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|       | 2nd | 315                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 312                    | ...310           | 1             | 0                     | 0     | 1     | 1     | 0     | 1     | 1     | 1     |
|       | 2nd | 625                    |                  |               |                       |       |       |       |       |       |       |       |
| 60 Hz | 1st | 4                      | 262              | 1             | 0                     | 0     | 0     | 0     | 0     | 1     | 1     | 0     |
|       | 2nd | 267                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 5                      | 0...             | 0             | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|       | 2nd | 268                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 265                    | ...260           | 1             | 0                     | 0     | 0     | 0     | 0     | 1     | 0     | 1     |
|       | 2nd | 3                      |                  |               |                       |       |       |       |       |       |       |       |

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

SA7114

15.2.23 SUBADDRESS 16H

**Table 62** VGATE stop; 17H[1] and 16H[7:0]  
Stop of VGATE pulse (HIGH-to-LOW transition), VGPS = 0; see Figs 22 and 23.

| FIELD |     | FRAME LINE<br>COUNTING | DECIMAL<br>VALUE | MSB<br>17H[1] | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|-------|-----|------------------------|------------------|---------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|       |     |                        |                  | VSTO8         | VSTO7                 | VSTO6 | VSTO5 | VSTO4 | VSTO3 | VSTO2 | VSTO1 | VSTO0 |
| 50 Hz | 1st | 1                      | 312              | 1             | 0                     | 0     | 1     | 1     | 1     | 0     | 0     | 0     |
|       | 2nd | 314                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 2                      | 0...             | 0             | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|       | 2nd | 315                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 312                    | ...310           | 1             | 0                     | 0     | 1     | 1     | 0     | 1     | 1     | 1     |
|       | 2nd | 625                    |                  |               |                       |       |       |       |       |       |       |       |
| 60 Hz | 1st | 4                      | 262              | 1             | 0                     | 0     | 0     | 0     | 0     | 1     | 1     | 0     |
|       | 2nd | 267                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 5                      | 0...             | 0             | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|       | 2nd | 268                    |                  |               |                       |       |       |       |       |       |       |       |
|       | 1st | 265                    | ...260           | 1             | 0                     | 0     | 0     | 0     | 0     | 1     | 0     | 1     |
|       | 2nd | 3                      |                  |               |                       |       |       |       |       |       |       |       |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.2.24 SUBADDRESS 17H

**Table 63** Miscellaneous/VGATE MSBs; 17H[7:6] and 17H[2:0]

| BIT | DESCRIPTION                | SYMBOL | VALUE        | FUNCTION                                     |
|-----|----------------------------|--------|--------------|----------------------------------------------|
| D7  | LLC output enable          | LLCE   | 0            | enable                                       |
|     |                            |        | 1            | 3-state                                      |
| D6  | LLC2 output enable         | LLC2E  | 0            | enable                                       |
|     |                            |        | 1            | 3-state                                      |
| D2  | alternative VGATE position | VGPS   | 0            | VGATE position according to Tables 61 and 62 |
|     |                            |        | 1            | VGATE occurs one line earlier during field 2 |
| D1  | MSB VGATE stop             | VSTO8  | see Table 62 |                                              |
| D0  | MSB VGATE start            | VSTA8  | see Table 61 |                                              |

## 15.2.25 SUBADDRESS 18H

**Table 64** Raw data gain control; RAWG[7:0]18H[7:0]; see Fig.19

| GAIN                   | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                        | RAWG7                 | RAWG6 | RAWG5 | RAWG4 | RAWG3 | RAWG2 | RAWG1 | RAWG0 |
| 255 (double amplitude) | 0                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| 128 (nominal level)    | 0                     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| 0 (off)                | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

## 15.2.26 SUBADDRESS 19H

**Table 65** Raw data offset control; RAWO[7:0] 19H[7:0]; see Fig.19

| OFFSET   | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|----------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|          | RAWO7                 | RAWO6 | RAWO5 | RAWO4 | RAWO3 | RAWO2 | RAWO1 | RAWO0 |
| -128 LSB | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 0 LSB    | 1                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| +128 LSB | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

## 15.2.27 SUBADDRESS 1FH

**Table 66** Status byte video decoder; 1FH[7:0]; read only register

| BIT | DESCRIPTION                                     | I <sup>2</sup> C-BUS CONTROL BIT | OLDSB 14H[2] | VALUE | FUNCTION          |
|-----|-------------------------------------------------|----------------------------------|--------------|-------|-------------------|
| D7  | status bit for interlace detection              | INTL                             | –            | 0     | non-interlaced    |
|     |                                                 |                                  |              | 1     | interlaced        |
| D6  | status bit for horizontal and vertical loop     | HLVLN                            | 0            | 0     | both loops locked |
|     |                                                 |                                  |              | 1     | unlocked          |
|     | status bit for locked horizontal frequency      | HLCK                             | 1            | 0     | locked            |
|     |                                                 |                                  |              | 1     | unlocked          |
| D5  | identification bit for detected field frequency | FIDT                             | –            | 0     | 50 Hz             |
|     |                                                 |                                  |              | 1     | 60 Hz             |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| BIT | DESCRIPTION                                                                   | I <sup>2</sup> C-BUS<br>CONTROL<br>BIT | OLDSB<br>14H[2] | VALUE | FUNCTION   |
|-----|-------------------------------------------------------------------------------|----------------------------------------|-----------------|-------|------------|
| D4  | gain value for active luminance channel is limited;<br>maximum (top)          | GLIMT                                  | –               | 0     | not active |
|     |                                                                               |                                        |                 | 1     | active     |
| D3  | gain value for active luminance channel is limited;<br>minimum (bottom)       | GLIMB                                  | –               | 0     | not active |
|     |                                                                               |                                        |                 | 1     | active     |
| D2  | white peak loop is activated                                                  | WIPA                                   | –               | 0     | not active |
|     |                                                                               |                                        |                 | 1     | active     |
| D1  | copy protected source detected according to<br>Macrovision version up to 7.01 | COPRO                                  | 0               | 0     | not active |
|     |                                                                               |                                        |                 | 1     | active     |
|     | slow time constant active in WIPA mode                                        | SLTCA                                  | 1               | 0     | not active |
|     |                                                                               |                                        |                 | 1     | active     |
| D0  | ready for capture (all internal loops locked)                                 | RDCAP                                  | 0               | 0     | not active |
|     |                                                                               |                                        |                 | 1     | active     |
|     | colour signal in accordance with selected standard<br>has been detected       | CODE                                   | 1               | 0     | not active |
|     |                                                                               |                                        |                 | 1     | active     |

## 15.3 Programming register audio clock generation

See equations in Section 8.6 and examples in Tables 22 and 23.

### 15.3.1 SUBADDRESSES 30H TO 32H

**Table 67** Audio master clock (AMCLK) cycles per field

| SUBADDRESS | CONTROL BITS D7 TO D0 |        |        |        |        |        |        |        |
|------------|-----------------------|--------|--------|--------|--------|--------|--------|--------|
| 30H        | ACPF7                 | ACPF6  | ACPF5  | ACPF4  | ACPF3  | ACPF2  | ACPF1  | ACPF0  |
| 31H        | ACPF15                | ACPF14 | ACPF13 | ACPF12 | ACPF11 | ACPF10 | ACPF9  | ACPF8  |
| 32H        | –                     | –      | –      | –      | –      | –      | ACPF17 | ACPF16 |

### 15.3.2 SUBADDRESSES 34H TO 36H

**Table 68** Audio master clock (AMCLK) nominal increment

| SUBADDRESS | CONTROL BITS D7 TO D0 |        |        |        |        |        |        |        |
|------------|-----------------------|--------|--------|--------|--------|--------|--------|--------|
| 34H        | ACNI7                 | ACNI6  | ACNI5  | ACNI4  | ACNI3  | ACNI2  | ACNI1  | ACNI0  |
| 35H        | ACNI15                | ACNI14 | ACNI13 | ACNI12 | ACNI11 | ACNI10 | ACNI9  | ACNI8  |
| 36H        | –                     | –      | ACNI21 | ACNI20 | ACNI19 | ACNI18 | ACNI17 | ACNI16 |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.3.3 SUBADDRESS 38H

**Table 69** Clock ratio audio master clock (AMCLK) to serial bit clock (ASCLK)

| SUBADDRESS | CONTROL BITS D7 TO D0 |   |       |       |       |       |       |       |
|------------|-----------------------|---|-------|-------|-------|-------|-------|-------|
| 38H        | –                     | – | SDIV5 | SDIV4 | SDIV3 | SDIV2 | SDIV1 | SDIV0 |

## 15.3.4 SUBADDRESS 39H

**Table 70** Clock ratio serial bit clock (ASCLK) to channel select clock (ALRCLK)

| SUBADDRESS | CONTROL BITS D7 TO D0 |   |        |        |        |        |        |        |
|------------|-----------------------|---|--------|--------|--------|--------|--------|--------|
| 39H        | –                     | – | LRDIV5 | LRDIV4 | LRDIV3 | LRDIV2 | LRDIV1 | LRDIV0 |

## 15.3.5 SUBADDRESS 3AH

**Table 71** Audio clock control; 3AH[3:0]

| BIT | DESCRIPTION                              | SYMBOL | VALUE | FUNCTION                                                    |
|-----|------------------------------------------|--------|-------|-------------------------------------------------------------|
| D3  | audio PLL modes                          | APLL   | 0     | PLL active, AMCLK is field-locked                           |
|     |                                          |        | 1     | PLL open, AMCLK is free-running                             |
| D2  | audio master clock<br>vertical reference | AMVR   | 0     | vertical reference pulse is taken from internal decoder     |
|     |                                          |        | 1     | vertical reference is taken from XRV input (expansion port) |
| D1  | ALRCLK phase                             | LRPH   | 0     | ALRCLK edges triggered by falling edges of ASCLK            |
|     |                                          |        | 1     | ALRCLK edges triggered by rising edges of ASCLK             |
| D0  | ASCLK phase                              | SCPH   | 0     | ASCLK edges triggered by falling edges of AMCLK             |
|     |                                          |        | 1     | ASCLK edges triggered by rising edges of AMCLK              |

## 15.4 Programming register VBI data slicer

### 15.4.1 SUBADDRESS 40H

**Table 72** Slicer control 1; 40H[6:4]

| BIT | DESCRIPTION         | SYMBOL | VALUE | FUNCTION                                                                              |
|-----|---------------------|--------|-------|---------------------------------------------------------------------------------------|
| D6  | Hamming check       | HAM_N  | 0     | <b>Hamming check for 2 bytes after framing code, dependent on data type (default)</b> |
|     |                     |        | 1     | no Hamming check                                                                      |
| D5  | framing code error  | FCE    | 0     | one framing code error allowed                                                        |
|     |                     |        | 1     | no framing code errors allowed                                                        |
| D4  | amplitude searching | HUNT_N | 0     | <b>amplitude searching active (default)</b>                                           |
|     |                     |        | 1     | amplitude searching stopped                                                           |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.4.2 SUBADDRESSES 41H TO 57H

**Table 73** Line control register; LCR2 to LCR24 (41H to 57H)

See Sections 8.2 and 8.4.

| NAME         | DESCRIPTION                                                  | FRAMING CODE       | D[7:4]<br>(41H TO 57H)        | D[3:0]<br>(41H TO 57H)        |
|--------------|--------------------------------------------------------------|--------------------|-------------------------------|-------------------------------|
|              |                                                              |                    | DT[3:0] 62H[3:0]<br>(FIELD 1) | DT[3:0] 62H[3:0]<br>(FIELD 2) |
| WST625       | teletext EuroWST, CCST                                       | 27H                | 0000                          | 0000                          |
| CC625        | European closed caption                                      | 001                | 0001                          | 0001                          |
| VPS          | video programming service                                    | 9951H              | 0010                          | 0010                          |
| WSS          | wide screen signalling bits                                  | 1E3C1FH            | 0011                          | 0011                          |
| WST525       | US teletext (WST)                                            | 27H                | 0100                          | 0100                          |
| CC525        | US closed caption (line 21)                                  | 001                | 0101                          | 0101                          |
| Test line    | video component signal, VBI region                           | –                  | 0110                          | 0110                          |
| Intercast    | raw data                                                     | –                  | 0111                          | 0111                          |
| General text | teletext                                                     | programmable       | 1000                          | 1000                          |
| VITC625      | VITC/EBU time codes (Europe)                                 | programmable       | 1001                          | 1001                          |
| VITC525      | VITC/SMPTE time codes (USA)                                  | programmable       | 1010                          | 1010                          |
| Reserved     | reserved                                                     | –                  | 1011                          | 1011                          |
| NABTS        | US NABTS                                                     | –                  | 1100                          | 1100                          |
| Japtext      | MOJI (Japanese)                                              | programmable (A7H) | 1101                          | 1101                          |
| JFS          | Japanese format switch (L20/22)                              | programmable       | 1110                          | 1110                          |
| Active video | <b>video component signal, active video region (default)</b> | –                  | 1111                          | 1111                          |

## 15.4.3 SUBADDRESS 58H

**Table 74** Programmable framing code; slicer set 58H[7:0]

According to Tables 15 and 73.

| FRAMING CODE FOR PROGRAMMABLE DATA TYPES | CONTROL BITS D7 TO D0 |
|------------------------------------------|-----------------------|
| Default value                            | FC[7:0] = 40H         |

## 15.4.4 SUBADDRESS 59H

**Table 75** Horizontal offset for slicer; slicer set 59H and 5BH

| HORIZONTAL OFFSET | CONTROL BITS 5BH[2:0] | CONTROL BITS 59H[7:0] |
|-------------------|-----------------------|-----------------------|
| Recommended value | HOFF[10:8] = 3H       | HOFF[7:0] = 47H       |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.4.5 SUBADDRESS 5AH

**Table 76** Vertical offset for slicer; slicer set 5AH and 5BH

| VERTICAL OFFSET                 | CONTROL BIT 5BH[4] | CONTROL BITS 5AH[7:0] |
|---------------------------------|--------------------|-----------------------|
|                                 | VOFF8              | VOFF[7:0]             |
| Minimum value 0                 | 0                  | 00H                   |
| Maximum value 312               | 1                  | 38H                   |
| Value for 50 Hz 625 lines input | 0                  | 03H                   |
| Value for 60 Hz 525 lines input | 0                  | 06H                   |

## 15.4.6 SUBADDRESS 5BH

**Table 77** Field offset, and MSBs for horizontal and vertical offsets; slicer set 5BH[7:6]

See Sections 15.4.4 and 15.4.5 for HOFF[10:8] 5BH[2:0] and VOFF8[5BH[4]].

| BIT | DESCRIPTION  | SYMBOL | VALUE | FUNCTION                                                                                |
|-----|--------------|--------|-------|-----------------------------------------------------------------------------------------|
| D7  | field offset | FOFF   | 0     | no modification of internal field indicator (default for 50 Hz 625 lines input sources) |
|     |              |        | 1     | invert field indicator (default for 60 Hz 525 lines input sources)                      |
| D6  | recode       | RECODE | 0     | <b>leave data unchanged (default)</b>                                                   |
|     |              |        | 1     | convert 00H and FFH data bytes into 03H and FCH                                         |

## 15.4.7 SUBADDRESS 5DH

**Table 78** Header and data identification (DID; ITU 656) code control; slicer set 5DH[7:0]

| BIT    | DESCRIPTION                                                                  | SYMBOL   | VALUE   | FUNCTION                                                                      |
|--------|------------------------------------------------------------------------------|----------|---------|-------------------------------------------------------------------------------|
| D7     | field ID and V-blank selection for text output (F and V reference selection) | FVREF    | 0       | F and V output of slicer is LCR table dependent                               |
|        |                                                                              |          | 1       | F and V output is taken from decoder real-time signals EVEN_ITU and VBLNK_ITU |
| D[5:0] | default; DID[5:0] = 00H                                                      | DID[5:0] | 00 0000 | ANC header framing; see Fig.31 and Table 21                                   |
|        | special cases of DID programming                                             |          | 11 1110 | DID[5:0] = 3EH SAV/EAV framing, with FVREF = 1                                |
|        |                                                                              |          | 11 1111 | DID[5:0] = 3FH SAV/EAV framing, with FVREF = 0                                |

## 15.4.8 SUBADDRESS 5EH

**Table 79** Sliced data identification (SDID) code; slicer set 5EH[5:0]

| BIT    | DESCRIPTION | SYMBOL    | VALUE | FUNCTION       |
|--------|-------------|-----------|-------|----------------|
| D[5:0] | SDID codes  | SDID[5:0] | 00H   | <b>default</b> |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.4.9 SUBADDRESS 60H

**Table 80** Slicer status byte 0; 60H[6:2]; read only register

| BIT | DESCRIPTION          | SYMBOL | VALUE | FUNCTION                                             |
|-----|----------------------|--------|-------|------------------------------------------------------|
| D6  | framing code valid   | FC8V   | 0     | no framing code (0 error) in the last frame detected |
|     |                      |        | 1     | framing code with 0 error detected                   |
| D5  | framing code valid   | FC7V   | 0     | no framing code (1 error) in the last frame detected |
|     |                      |        | 1     | framing code with 1 error detected                   |
| D4  | VPS valid            | VPSV   | 0     | no VPS in the last frame                             |
|     |                      |        | 1     | VPS detected                                         |
| D3  | PALplus valid        | PPV    | 0     | no PALplus in the last frame                         |
|     |                      |        | 1     | PALplus detected                                     |
| D2  | closed caption valid | CCV    | 0     | no closed caption in the last frame                  |
|     |                      |        | 1     | closed caption detected                              |

## 15.4.10 SUBADDRESSES 61H AND 62H

**Table 81** Slicer status byte 1; 61H[5:0] and slicer status byte 2; 62H[7:0]; read only registers

| SUBADDRESS | BIT    | SYMBOL  | DESCRIPTION                                             |
|------------|--------|---------|---------------------------------------------------------|
| 61H        | D5     | F21_N   | field ID as seen by the VBI slicer; for field 1: D5 = 0 |
|            | D[4:0] | LN[8:4] | line number                                             |
| 62H        | D[7:4] | LN[3:0] |                                                         |
|            | D[3:0] | DT[3:0] | data type; according to Table 15                        |

## 15.5 Programming register interfaces and scaler part

### 15.5.1 SUBADDRESS 80H

**Table 82** Global control 1; global set 80H[6:4]; note 1

SWRST moved to subaddress 88H[5].

| TASK ENABLE CONTROL                                               | CONTROL BITS D6 TO D4 |     |     |
|-------------------------------------------------------------------|-----------------------|-----|-----|
|                                                                   | SMOD                  | TEB | TEA |
| Task of register set A is disabled                                | X                     | X   | 0   |
| Task of register set A is enabled                                 | X                     | X   | 1   |
| Task of register set B is disabled                                | X                     | 0   | X   |
| Task of register set B is enabled                                 | X                     | 1   | X   |
| The scaler window defines the F and V timing of the scaler output | 0                     | X   | X   |
| VBI data slicer defines the F and V timing of the scaler output   | 1                     | X   | X   |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 83** Global control 1; global set 80H[3:0]; note 1

| I PORT AND SCALER BACK-END CLOCK SELECTION                                                 | CONTROL BITS D3 TO D0 |                  |       |       |
|--------------------------------------------------------------------------------------------|-----------------------|------------------|-------|-------|
|                                                                                            | ICKS3                 | ICKS2            | ICKS1 | ICKS0 |
| ICLK output and back-end clock is line-locked clock LLC from decoder                       | X                     | X                | 0     | 0     |
| ICLK output and back-end clock is XCLK from X port                                         | X                     | X                | 0     | 1     |
| ICLK output is LLC and back-end clock is LLC2 clock                                        | X                     | X <sup>(2)</sup> | 1     | 0     |
| Back-end clock is the ICLK input                                                           | X                     | X                | 1     | 1     |
| IDQ pin carries the data qualifier                                                         | X                     | 0                | X     | X     |
| IDQ pin carries a gated back-end clock (DQ AND CLK)                                        | X                     | 1                | X     | X     |
| IDQ generation only for valid data                                                         | 0                     | X                | X     | X     |
| IDQ qualifies valid data inside the scaling region and all data outside the scaling region | 1                     | X                | X     | X     |

**Notes**

1. X = don't care.
2. Although the ICLKO I/O is independent of ICKS2 and ICKS3, this selection can only be used if ICKS2 = 1.

## 15.5.2 SUBADDRESSES 83H TO 87H

**Table 84** X port I/O enable and output clock phase control; global set 83H[5:4]

| OUTPUT CLOCK PHASE CONTROL                             | CONTROL BITS D5 AND D4 |       |
|--------------------------------------------------------|------------------------|-------|
|                                                        | XPCK1                  | XPCK0 |
| XCLK default output phase, recommended value           | 0                      | 0     |
| XCLK output inverted                                   | 0                      | 1     |
| XCLK phase shifted by approximately 3 ns               | 1                      | 0     |
| XCLK output inverted and shifted by approximately 3 ns | 1                      | 1     |

**Table 85** X port I/O enable and output clock phase control; global set 83H[2:0]; note 1

| X PORT I/O ENABLE                                                                                         | CONTROL BITS D2 TO D0 |      |      |
|-----------------------------------------------------------------------------------------------------------|-----------------------|------|------|
|                                                                                                           | XRQT                  | XPE1 | XPE0 |
| X port output is disabled by software                                                                     | X                     | 0    | 0    |
| X port output is enabled by software                                                                      | X                     | 0    | 1    |
| X port output is enabled by pin XTRI at logic 0                                                           | X                     | 1    | 0    |
| X port output is enabled by pin XTRI at logic 1                                                           | X                     | 1    | 1    |
| XRDY output signal is A/B task flag from event handler (A = 1)                                            | 0                     | X    | X    |
| XRDY output signal is ready signal from scaler path (XRDY = 1 means the SAA7114 is ready to receive data) | 1                     | X    | X    |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 86** I port signal definitions; global set 84H[7:6] and 86H[5]

| I PORT SIGNAL DEFINITIONS                                                           | CONTROL BITS |          |       |
|-------------------------------------------------------------------------------------|--------------|----------|-------|
|                                                                                     | 86H[5]       | 84H[7:6] |       |
|                                                                                     | IDG02        | IDG01    | IDG00 |
| IGP0 is output field ID, as defined by OFIDC[90H[6]]                                | 0            | 0        | 0     |
| IGP0 is A/B task flag, as defined by CONLH[90H[7]]                                  | 0            | 0        | 1     |
| IGP0 is sliced data flag, framing the sliced VBI data at the I port                 | 0            | 1        | 0     |
| <b>IGP0 is set to logic 0 (default polarity)</b>                                    | 0            | 1        | 1     |
| IGP0 is the output FIFO almost filled flag                                          | 1            | 0        | 0     |
| IGP0 is the output FIFO overflow flag                                               | 1            | 0        | 1     |
| IGP0 is the output FIFO almost full flag, level to be programmed in subaddress 86H  | 1            | 1        | 0     |
| IGP0 is the output FIFO almost empty flag, level to be programmed in subaddress 86H | 1            | 1        | 1     |

**Table 87** I port signal definitions; global set 84H[5:4] and 86H[4]

| I PORT SIGNAL DEFINITIONS                                                           | CONTROL BITS |          |       |
|-------------------------------------------------------------------------------------|--------------|----------|-------|
|                                                                                     | 86H[4]       | 84H[5:4] |       |
|                                                                                     | IDG12        | IDG11    | IDG10 |
| IGP1 is output field ID, as defined by OFIDC[90H[6]]                                | 0            | 0        | 0     |
| IGP1 is A/B task flag, as defined by CONLH[90H[7]]                                  | 0            | 0        | 1     |
| IGP1 is sliced data flag, framing the sliced VBI data at the I port                 | 0            | 1        | 0     |
| <b>IGP1 is set to logic 0 (default polarity)</b>                                    | 0            | 1        | 1     |
| IGP1 is the output FIFO almost filled flag                                          | 1            | 0        | 0     |
| IGP1 is the output FIFO overflow flag                                               | 1            | 0        | 1     |
| IGP1 is the output FIFO almost full flag, level to be programmed in subaddress 86H  | 1            | 1        | 0     |
| IGP1 is the output FIFO almost empty flag, level to be programmed in subaddress 86H | 1            | 1        | 1     |

**Table 88** I port output signal definitions; global set 84H[3:0]; note 1

| I PORT OUTPUT SIGNAL DEFINITIONS                                                                                        | CONTROL BITS D3 TO D0 |      |      |      |
|-------------------------------------------------------------------------------------------------------------------------|-----------------------|------|------|------|
|                                                                                                                         | IDV1                  | IDV0 | IDH1 | IDH0 |
| IGPH is a H gate signal, framing the scaler output                                                                      | X                     | X    | 0    | 0    |
| IGPH is an extended H gate (framing H gate during scaler output and scaler input H reference outside the scaler window) | X                     | X    | 0    | 1    |
| IGPH is a horizontal trigger pulse, on active going edge of H gate                                                      | X                     | X    | 1    | 0    |
| IGPH is a horizontal trigger pulse, on active going edge of extended H gate                                             | X                     | X    | 1    | 1    |
| IGPV is a V gate signal, framing scaled output lines                                                                    | 0                     | 0    | X    | X    |
| IGPV is the V reference signal from scaler input                                                                        | 0                     | 1    | X    | X    |
| IGPV is a vertical trigger pulse, derived from V gate                                                                   | 1                     | 0    | X    | X    |
| IGPV is a vertical trigger pulse derived from input V reference                                                         | 1                     | 1    | X    | X    |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 89** X port signal definitions text slicer; global set 85H[7:5]; note 1

| X PORT SIGNAL DEFINITIONS TEXT SLICER                                                                                            | CONTROL BITS D7 TO D5 |       |      |
|----------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------|------|
|                                                                                                                                  | ISWP1                 | ISWP0 | ILLV |
| Video data limited to range 1 to 254                                                                                             | X                     | X     | 0    |
| Video data limited to range 8 to 247                                                                                             | X                     | X     | 1    |
| Dword byte swap, influences serial output timing<br>D0 D1 D2 D3 $\Rightarrow$ FF 00 00 SAV C <sub>B0</sub> Y0 C <sub>R0</sub> Y1 | 0                     | 0     | X    |
| D1 D0 D3 D2 $\Rightarrow$ 00 FF SAV 00 Y0 C <sub>B0</sub> Y1 C <sub>R0</sub>                                                     | 0                     | 1     | X    |
| D2 D3 D0 D1 $\Rightarrow$ 00 SAV FF 00 C <sub>R0</sub> Y1 C <sub>B0</sub> Y0                                                     | 1                     | 0     | X    |
| D3 D2 D1 D0 $\Rightarrow$ SAV 00 00 FF Y1 C <sub>R0</sub> Y0 C <sub>B0</sub>                                                     | 1                     | 1     | X    |

**Note**

1. X = don't care.

**Table 90** I port reference signal polarities; global set 85H[4:0]; note 1

| I PORT REFERENCE SIGNAL POLARITIES    | CONTROL BITS D4 TO D0 |      |      |      |      |
|---------------------------------------|-----------------------|------|------|------|------|
|                                       | IG0P                  | IG1P | IRVP | IRHP | IDQP |
| IDQ at default polarity (1 = active)  | X                     | X    | X    | X    | 0    |
| IDQ is inverted                       | X                     | X    | X    | X    | 1    |
| IGPH at default polarity (1 = active) | X                     | X    | X    | 0    | X    |
| IGPH is inverted                      | X                     | X    | X    | 1    | X    |
| IGPV at default polarity (1 = active) | X                     | X    | 0    | X    | X    |
| IGPV is inverted                      | X                     | X    | 1    | X    | X    |
| IGP1 at default polarity              | X                     | 0    | X    | X    | X    |
| IGP1 is inverted                      | X                     | 1    | X    | X    | X    |
| IGP0 at default polarity              | 0                     | X    | X    | X    | X    |
| IGP0 is inverted                      | 1                     | X    | X    | X    | X    |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 91** I port FIFO flag control and arbitration; global set 86H[7:4]; note 1

| FUNCTION                                               | CONTROL BITS D7 TO D4 |       |       |       |
|--------------------------------------------------------|-----------------------|-------|-------|-------|
|                                                        | VITX1                 | VITX0 | IDG02 | IDG12 |
| See subaddress 84H: IDG11 and IDG10                    | X                     | X     | X     | 0     |
|                                                        | X                     | X     | X     | 1     |
| See subaddress 84H: IDG01 and IDG00                    | X                     | X     | 0     | X     |
|                                                        | X                     | X     | 1     | X     |
| <b>I port signal definitions</b>                       |                       |       |       |       |
| I port data output inhibited                           | 0                     | 0     | X     | X     |
| Only video data is transferred                         | 0                     | 1     | X     | X     |
| Only text data is transferred (no EAV, SAV will occur) | 1                     | 0     | X     | X     |
| Text and video data is transferred, text has priority  | 1                     | 1     | X     | X     |

**Note**

1. X = don't care.

**Table 92** I port FIFO flag control and arbitration; global set 86H[3:0]; note 1

| I PORT FIFO FLAG CONTROL AND ARBITRATION | CONTROL BITS D3 TO D0 |      |      |      |
|------------------------------------------|-----------------------|------|------|------|
|                                          | FFL1                  | FFL0 | FEL1 | FEL0 |
| FAE FIFO flag almost empty level         |                       |      |      |      |
| <16 Dwords                               | X                     | X    | 0    | 0    |
| <8 Dwords                                | X                     | X    | 0    | 1    |
| <4 Dwords                                | X                     | X    | 1    | 0    |
| 0 Dwords                                 | X                     | X    | 1    | 1    |
| FAF FIFO flag almost full level          |                       |      |      |      |
| ≥16 Dwords                               | 0                     | 0    | X    | X    |
| ≥24 Dwords                               | 0                     | 1    | X    | X    |
| ≥28 Dwords                               | 1                     | 0    | X    | X    |
| 32 Dwords                                | 1                     | 1    | X    | X    |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 93** I port I/O enable, output clock and gated clock phase control; global set 87H[7:4]; note 1

| OUTPUT CLOCK AND GATED CLOCK PHASE CONTROL                                                                                    | CONTROL BITS D7 TO D4 |                      |       |       |
|-------------------------------------------------------------------------------------------------------------------------------|-----------------------|----------------------|-------|-------|
|                                                                                                                               | IPCK3 <sup>(2)</sup>  | IPCK2 <sup>(2)</sup> | IPCK1 | IPCK0 |
| ICLK default output phase                                                                                                     | X                     | X                    | 0     | 0     |
| ICLK phase shifted by $\frac{1}{2}$ clock cycle $\Rightarrow$ recommended for ICKS1 = 1 and ICKS0 = 0 (subaddress 80H)        | X                     | X                    | 0     | 1     |
| ICLK phase shifted by approximately 3 ns                                                                                      | X                     | X                    | 1     | 0     |
| ICLK phase shifted by $\frac{1}{2}$ clock cycle + approximately 3 ns $\Rightarrow$ alternatively to setting '01'              | X                     | X                    | 1     | 1     |
| IDQ = gated clock default output phase                                                                                        | 0                     | 0                    | X     | X     |
| IDQ = gated clock phase shifted by $\frac{1}{2}$ clock cycle $\Rightarrow$ recommended for gated clock output                 | 0                     | 1                    | X     | X     |
| IDQ = gated clock phase shifted by approximately 3 ns                                                                         | 1                     | 0                    | X     | X     |
| IDQ = gated clock phase shifted by $\frac{1}{2}$ clock cycle + approximately 3 ns $\Rightarrow$ alternatively to setting '01' | 1                     | 1                    | X     | X     |

**Notes**

1. X = don't care.
2. IPCK3 and IPCK2 only affects the gated clock (subaddress 80H, bit ICKS2 = 1).

**Table 94** I port I/O enable, output clock and gated clock phase control; global set 87H[1:0]

| I PORT I/O ENABLE                               | CONTROL BITS D1 AND D0 |      |
|-------------------------------------------------|------------------------|------|
|                                                 | IPE1                   | IPE0 |
| I port output is disabled by software           | 0                      | 0    |
| I port output is enabled by software            | 0                      | 1    |
| I port output is enabled by pin ITRI at logic 0 | 1                      | 0    |
| I port output is enabled by pin ITRI at logic 1 | 1                      | 1    |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.5.3 SUBADDRESS 88H

**Table 95** Power save control; global set 88H[7:4]; note 1

| POWER SAVE CONTROL                                                                                                                                                                                                                              | CONTROL BITS D7 TO D4 |       |                      |       |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------|----------------------|-------|
|                                                                                                                                                                                                                                                 | CH4EN                 | CH2EN | SWRST <sup>(2)</sup> | DPROG |
| DPROG = 0 after reset                                                                                                                                                                                                                           | X                     | X     | X                    | 0     |
| DPROG = 1 can be used to assign that the device has been programmed; this bit can be monitored in the scalers status byte, bit PRDON; if DPROG was set to logic 1 and PRDON status bit shows a logic 0 a power-up or start-up fail has occurred | X                     | X     | X                    | 1     |
| Scaler path is reset to its idle state, software reset                                                                                                                                                                                          | X                     | X     | 0                    | X     |
| Scaler is switched back to operation                                                                                                                                                                                                            | X                     | X     | 1                    | X     |
| AD1x analog channel is in power-down mode                                                                                                                                                                                                       | X                     | 0     | X                    | X     |
| AD1x analog channel is active                                                                                                                                                                                                                   | X                     | 1     | X                    | X     |
| AD2x analog channel is in power-down mode                                                                                                                                                                                                       | 0                     | X     | X                    | X     |
| AD2x analog channel is active                                                                                                                                                                                                                   | 1                     | X     | X                    | X     |

**Notes**

1. X = don't care.
2. Bit SWRST is now located here.

**Table 96** Power save control; global set 88H[3] and 88H[1:0]; note 1

| POWER SAVE CONTROL                                                                                                                                         | CONTROL BITS D3, D1 AND D0 |      |      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|------|------|
|                                                                                                                                                            | SLM3                       | SLM1 | SLM0 |
| Decoder and VBI slicer are in operational mode                                                                                                             | X                          | X    | 0    |
| Decoder and VBI slicer are in power-down mode; scaler only operates, if scaler input and ICLK source is the X port (refer to subaddresses 80H and 91H/C1H) | X                          | X    | 1    |
| Scaler is in operational mode                                                                                                                              | X                          | 0    | X    |
| Scaler is in power-down mode; scaler in power-down stops I port output                                                                                     | X                          | 1    | X    |
| Audio clock generation active                                                                                                                              | 0                          | X    | X    |
| Audio clock generation in power-down and output disabled                                                                                                   | 1                          | X    | X    |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.5.4 SUBADDRESS 8FH

**Table 97** Status information scaler part; 8FH[7:0]; read only register

| BIT | I <sup>2</sup> C-BUS STATUS BIT | FUNCTION <sup>(1)</sup>                                                                                                                                                                                                       |
|-----|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D7  | XTRI                            | status on input pin XTRI, if not used for 3-state control, usable as hardware flag for software use                                                                                                                           |
| D6  | ITRI                            | status on input pin ITRI, if not used for 3-state control, usable as hardware flag for software use                                                                                                                           |
| D5  | FFIL                            | status of the internal 'FIFO almost filled' flag                                                                                                                                                                              |
| D4  | FFOV                            | status of the internal 'FIFO overflow' flag                                                                                                                                                                                   |
| D3  | PRDON                           | copy of bit DPROG, can be used to detect power-up and start-up fails                                                                                                                                                          |
| D2  | ERROF                           | error flag of scalers output formatter, normally set, if the output processing needs to be interrupted, due to input/output data rate conflicts, e.g. if output data rate is much too low and all internal FIFO capacity used |
| D1  | FIDSCI                          | status of the field sequence ID at the scalers input                                                                                                                                                                          |
| D0  | FIDSCO                          | status of the field sequence ID at the scalers output, scaler processing dependent                                                                                                                                            |

**Note**

- Status information is unsynchronized and shows the actual status at the time of I<sup>2</sup>C-bus read.

## 15.5.5 SUBADDRESSES 90H AND C0H

**Table 98** Task handling control; register set A [90H[7:6]] and B [C0H[7:6]]; note 1

| EVENT HANDLER CONTROL                                                                                                           | CONTROL BITS D7 AND D6 |       |
|---------------------------------------------------------------------------------------------------------------------------------|------------------------|-------|
|                                                                                                                                 | CONLH                  | OFIDC |
| Output field ID is field ID from scaler input                                                                                   | X                      | 0     |
| Output field ID is task status flag, which changes every time a selected task is activated (not synchronized to input field ID) | X                      | 1     |
| Scaler SAV/EAV byte bit D7 and task flag = 1, default                                                                           | 0                      | X     |
| Scaler SAV/EAV byte bit D7 and task flag = 0                                                                                    | 1                      | X     |

**Note**

- X = don't care.

**Table 99** Task handling control; register set A [90H[5:3]] and B [C0H[5:3]]

| EVENT HANDLER CONTROL                                    | CONTROL BITS D5 TO D3 |       |       |
|----------------------------------------------------------|-----------------------|-------|-------|
|                                                          | FSKP2                 | FSKP1 | FSKP0 |
| Active task is carried out directly                      | 0                     | 0     | 0     |
| 1 field is skipped before active task is carried out     | 0                     | 0     | 1     |
| ... fields are skipped before active task is carried out | ...                   | ...   | ...   |
| 6 fields are skipped before active task is carried out   | 1                     | 1     | 0     |
| 7 fields are skipped before active task is carried out   | 1                     | 1     | 1     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 100** Task handling control; register set A [90H[2:0]] and B [C0H[2:0]]; note 1

| EVENT HANDLER CONTROL                                                        | CONTROL BITS D2 TO D0 |       |       |
|------------------------------------------------------------------------------|-----------------------|-------|-------|
|                                                                              | RPTSK                 | STRC1 | STRC0 |
| Event handler triggers immediately after finishing a task                    | X                     | 0     | 0     |
| Event handler triggers with next V-sync                                      | X                     | 0     | 1     |
| Event handler triggers with field ID = 0                                     | X                     | 1     | 0     |
| Event handler triggers with field ID = 1                                     | X                     | 1     | 1     |
| If active task is finished, handling is taken over by the next task          | 0                     | X     | X     |
| Active task is repeated once, before handling is taken over by the next task | 1                     | X     | X     |

**Note**

1. X = don't care.

## 15.5.6 SUBADDRESSES 91H TO 93H

**Table 101** X port formats and configuration; register set A [91H[7:3]] and B [C1H[7:3]]; note 1

| SCALER INPUT FORMAT AND CONFIGURATION SOURCE SELECTION                                                                                                          | CONTROL BITS D7 TO D3 |       |        |        |       |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------|--------|--------|-------|
|                                                                                                                                                                 | CONLV                 | HLDFV | SCSRC1 | SCSRC0 | SCRQE |
| Only if XRQT[83H[2]] = 1: scaler input source reacts on SAA7114 request                                                                                         | X                     | X     | X      | X      | 0     |
| Scaler input source is a continuous data stream, which cannot be interrupted (must be logic 1, if SAA7114 decoder part is source of scaler or XRQT[83H[2]] = 0) | X                     | X     | X      | X      | 1     |
| Scaler input source is data from decoder, data type is provided according to Table 15                                                                           | X                     | X     | 0      | 0      | X     |
| Scaler input source is Y-C <sub>B</sub> -C <sub>R</sub> data from X port                                                                                        | X                     | X     | 0      | 1      | X     |
| Scaler input source is raw digital CVBS from selected analog channel, for backward compatibility only, further use is not recommended                           | X                     | X     | 1      | 0      | X     |
| Scaler input source is raw digital CVBS (or 16-bit Y + C <sub>B</sub> -C <sub>R</sub> , if no 16-bit outputs are active) from X port                            | X                     | X     | 1      | 1      | X     |
| SAV/EAV code bits D6 and D5 (F and V) may change between SAV and EAV                                                                                            | X                     | 0     | X      | X      | X     |
| SAV/EAV code bits D6 and D5 (F and V) are synchronized to scalers output line start                                                                             | X                     | 1     | X      | X      | X     |
| SAV/EAV code bit D5 (V) and V gate on pin IGPV as generated by the internal processing; see Fig.37                                                              | 0                     | X     | X      | X      | X     |
| SAV/EAV code bit D5 (V) and V gate are inverted                                                                                                                 | 1                     | X     | X      | X      | X     |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 102** X port formats and configuration; register set A [91H[2:0]] and B [C1H[2:0]]; note 1

| SCALER INPUT FORMAT AND CONFIGURATION FORMAT<br>CONTROL                  | CONTROL BITS D2 TO D0 |                     |      |
|--------------------------------------------------------------------------|-----------------------|---------------------|------|
|                                                                          | FSC2 <sup>(2)</sup>   | FSC1 <sup>(2)</sup> | FSC0 |
| Input is Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 like sampling scheme | X                     | X                   | 0    |
| Input is Y-C <sub>B</sub> -C <sub>R</sub> 4 : 1 : 1 like sampling scheme | X                     | X                   | 1    |
| <b>Chroma is provided every line, default</b>                            | 0                     | 0                   | X    |
| Chroma is provided every 2nd line                                        | 0                     | 1                   | X    |
| Chroma is provided every 3rd line                                        | 1                     | 0                   | X    |
| Chroma is provided every 4th line                                        | 1                     | 1                   | X    |

**Notes**

1. X = don't care.
2. FSC2 and FSC1 only to be used, if X port input source does not provide chroma information for every input line. X port input stream must contain dummy chroma bytes.

**Table 103** X port input reference signal definitions; register set A [92H[7:4]] and B [C2H[7:4]]; note 1

| X PORT INPUT REFERENCE SIGNAL DEFINITIONS                                        | CONTROL BITS D7 TO D4 |      |      |      |
|----------------------------------------------------------------------------------|-----------------------|------|------|------|
|                                                                                  | XFDV                  | XFDH | XDV1 | XDV0 |
| Rising edge of XRV input and decoder V123 is vertical reference                  | X                     | X    | X    | 0    |
| Falling edge of XRV input and decoder V123 is vertical reference                 | X                     | X    | X    | 1    |
| XRV is a V-sync or V gate signal                                                 | X                     | X    | 0    | X    |
| XRV is a frame sync, V pulses are generated internally on both edges of FS input | X                     | X    | 1    | X    |
| X port field ID is state of XRH at reference edge on XRV (defined by XFDV)       | X                     | 0    | X    | X    |
| Field ID (decoder and X port field ID) is inverted                               | X                     | 1    | X    | X    |
| Reference edge for field detection is falling edge of XRV                        | 0                     | X    | X    | X    |
| Reference edge for field detection is rising edge of XRV                         | 1                     | X    | X    | X    |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 104** X port input reference signal definitions; register set A [92H[3:0]] and B [C2H[3:0]]; note 1

| X PORT INPUT REFERENCE SIGNAL DEFINITIONS             | CONTROL BITS D3 TO D0 |     |     |      |
|-------------------------------------------------------|-----------------------|-----|-----|------|
|                                                       | XCODE                 | XDH | XDQ | XCKS |
| XCLK input clock and XDQ input qualifier are needed   | X                     | X   | X   | 0    |
| Data rate is defined by XCLK only, no XDQ signal used | X                     | X   | X   | 1    |
| Data are qualified at XDQ input at logic 1            | X                     | X   | 0   | X    |
| Data are qualified at XDQ input at logic 0            | X                     | X   | 1   | X    |
| Rising edge of XRH input is horizontal reference      | X                     | 0   | X   | X    |
| Falling edge of XRH input is horizontal reference     | X                     | 1   | X   | X    |
| Reference signals are taken from XRH and XRV          | 0                     | X   | X   | X    |
| Reference signals are decoded from EAV and SAV        | 1                     | X   | X   | X    |

**Note**

1. X = don't care.

**Table 105** I port output format and configuration; register set A [93H[7:5]] and B [C3H[7:5]]; note 1

| I PORT OUTPUT FORMATS AND CONFIGURATION                                                          | CONTROL BITS D7 TO D5 |       |      |
|--------------------------------------------------------------------------------------------------|-----------------------|-------|------|
|                                                                                                  | ICODE                 | I8_16 | FYSK |
| All lines will be output                                                                         | X                     | X     | 0    |
| Skip the number of leading Y only lines, as defined by FOI1 and FOI0                             | X                     | X     | 1    |
| Dwords are transferred byte wise, see subaddress 85H bits ISWP1 and ISWP0                        | X                     | 0     | X    |
| Dwords are transferred 16-bit word wise via IPD and HPD, see subaddress 85H bits ISWP1 and ISWP0 | X                     | 1     | X    |
| No ITU 656 like SAV/EAV codes are available                                                      | 0                     | X     | X    |
| ITU 656 like SAV/EAV codes are inserted in the output data stream, framed by a qualifier         | 1                     | X     | X    |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 106** I port output format and configuration; register set A [93H[4:0]] and B [C3H[4:0]]; note 1

| I PORT OUTPUT FORMATS AND CONFIGURATION                                                            | CONTROL BITS D4 TO D0 |      |      |      |      |
|----------------------------------------------------------------------------------------------------|-----------------------|------|------|------|------|
|                                                                                                    | FOI1                  | FOI0 | FSI2 | FSI1 | FSI0 |
| 4 : 2 : 2 Dword formatting                                                                         | X                     | X    | 0    | 0    | 0    |
| 4 : 1 : 1 Dword formatting                                                                         | X                     | X    | 0    | 0    | 1    |
| 4 : 2 : 0, only every 2nd line Y + C <sub>B</sub> -C <sub>R</sub> output, in between Y only output | X                     | X    | 0    | 1    | 0    |
| 4 : 1 : 0, only every 4th line Y + C <sub>B</sub> -C <sub>R</sub> output, in between Y only output | X                     | X    | 0    | 1    | 1    |
| Y only                                                                                             | X                     | X    | 1    | 0    | 0    |
| Not defined                                                                                        | X                     | X    | 1    | 0    | 1    |
| Not defined                                                                                        | X                     | X    | 1    | 1    | 0    |
| Not defined                                                                                        | X                     | X    | 1    | 1    | 1    |
| No leading Y only line, before 1st Y + C <sub>B</sub> -C <sub>R</sub> line is output               | 0                     | 0    | X    | X    | X    |
| 1 leading Y only line, before 1st Y + C <sub>B</sub> -C <sub>R</sub> line is output                | 0                     | 1    | X    | X    | X    |
| 2 leading Y only lines, before 1st Y + C <sub>B</sub> -C <sub>R</sub> line is output               | 1                     | 0    | X    | X    | X    |
| 3 leading Y only lines, before 1st Y + C <sub>B</sub> -C <sub>R</sub> line is output               | 1                     | 1    | X    | X    | X    |

**Note**

1. X = don't care.

## 15.5.7 SUBADDRESSES 94H TO 9BH

**Table 107** Horizontal input window start; register set A [94H[7:0]; 95H[3:0]] and B [C4H[7:0]; C5H[3:0]]

| HORIZONTAL INPUT<br>ACQUISITION WINDOW<br>DEFINITION OFFSET IN<br>X (HORIZONTAL) DIRECTION <sup>(1)</sup>                            | CONTROL BITS                 |      |     |     |                              |     |     |     |     |     |     |     |
|--------------------------------------------------------------------------------------------------------------------------------------|------------------------------|------|-----|-----|------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                                                                                                                      | A [95H[3:0]]<br>B [C5H[3:0]] |      |     |     | A [94H[7:0]]<br>B [C4H[7:0]] |     |     |     |     |     |     |     |
|                                                                                                                                      | XO11                         | XO10 | XO9 | XO8 | XO7                          | XO6 | XO5 | XO4 | XO3 | XO2 | XO1 | XO0 |
| A minimum of '2' should be kept, due to a line counting mismatch                                                                     | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 1   | 0   |
| Odd offsets are changing the C <sub>B</sub> -C <sub>R</sub> sequence in the output stream to C <sub>R</sub> -C <sub>B</sub> sequence | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 1   | 1   |
| Maximum possible pixel offset = 4095                                                                                                 | 1                            | 1    | 1   | 1   | 1                            | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

**Note**

1. Reference for counting are luminance samples.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 108** Horizontal input window length; register set A [96H[7:0]; 97H[3:0]] and B [C6H[7:0]; C7H[3:0]]

| HORIZONTAL INPUT<br>ACQUISITION WINDOW<br>DEFINITION INPUT WINDOW<br>LENGTH IN X (HORIZONTAL)<br>DIRECTION <sup>(1)</sup> | CONTROL BITS                 |      |     |     |                              |     |     |     |     |     |     |     |
|---------------------------------------------------------------------------------------------------------------------------|------------------------------|------|-----|-----|------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                                                                                                           | A [97H[3:0]]<br>B [C7H[3:0]] |      |     |     | A [96H[7:0]]<br>B [C6H[7:0]] |     |     |     |     |     |     |     |
|                                                                                                                           | XS11                         | XS10 | XS9 | XS8 | XS7                          | XS6 | XS5 | XS4 | XS3 | XS2 | XS1 | XS0 |
| No output                                                                                                                 | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Odd lengths are allowed, but will be rounded up to even lengths                                                           | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| Maximum possible number of input pixels = 4095                                                                            | 1                            | 1    | 1   | 1   | 1                            | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

**Note**

- Reference for counting are luminance samples.

**Table 109** Vertical input window start; register set A [98H[7:0]; 99H[3:0]] and B [C8H[7:0]; C9H[3:0]]

| VERTICAL INPUT ACQUISITION<br>WINDOW DEFINITION OFFSET IN<br>Y (VERTICAL) DIRECTION <sup>(1)</sup> | CONTROL BITS                 |      |     |     |                              |     |     |     |     |     |     |     |
|----------------------------------------------------------------------------------------------------|------------------------------|------|-----|-----|------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                                                                                    | A [99H[3:0]]<br>B [C9H[3:0]] |      |     |     | A [98H[7:0]]<br>B [C8H[7:0]] |     |     |     |     |     |     |     |
|                                                                                                    | YO11                         | YO10 | YO9 | YO8 | YO7                          | YO6 | YO5 | YO4 | YO3 | YO2 | YO1 | YO0 |
| Line offset = 0                                                                                    | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Line offset = 1                                                                                    | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| Maximum line offset = 4095                                                                         | 1                            | 1    | 1   | 1   | 1                            | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

**Note**

- For trigger condition: STRC[1:0] 90H[1:0] = 00; YO + YS > (number of input lines per field – 2), will result in field dropping. Other trigger conditions: YO > (number of input lines per field – 2), will result in field dropping.

**Table 110** Vertical input window length; register set A [9AH[7:0]; 9BH[3:0]] and B [CAH[7:0]; CBH[3:0]]

| VERTICAL INPUT ACQUISITION<br>WINDOW DEFINITION INPUT<br>WINDOW LENGTH IN<br>Y (VERTICAL) DIRECTION <sup>(1)</sup> | CONTROL BITS                 |      |     |     |                              |     |     |     |     |     |     |     |
|--------------------------------------------------------------------------------------------------------------------|------------------------------|------|-----|-----|------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                                                                                                    | A [9BH[3:0]]<br>B [CBH[3:0]] |      |     |     | A [9AH[7:0]]<br>B [CAH[7:0]] |     |     |     |     |     |     |     |
|                                                                                                                    | YS11                         | YS10 | YS9 | YS8 | YS7                          | YS6 | YS5 | YS4 | YS3 | YS2 | YS1 | YS0 |
| No input lines                                                                                                     | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 1 input line                                                                                                       | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| Maximum possible number of input lines = 4095                                                                      | 1                            | 1    | 1   | 1   | 1                            | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

**Note**

- For trigger condition: STRC[1:0] 90H[1:0] = 00; YO + YS > (number of input lines per field – 2), will result in field dropping. Other trigger conditions: YS > (number of input lines per field – 2), will result in field dropping.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.5.8 SUBADDRESSES 9CH TO 9FH

**Table 111** Horizontal output window length; register set A [9CH[7:0]; 9DH[3:0]] and B [CCH[7:0]; CDH[3:0]]

| HORIZONTAL OUTPUT<br>ACQUISITION WINDOW<br>DEFINITION NUMBER OF<br>DESIRED OUTPUT PIXELS IN<br>X (HORIZONTAL) DIRECTION <sup>(1)</sup> | CONTROL BITS                 |      |     |     |                              |     |     |     |     |     |     |     |
|----------------------------------------------------------------------------------------------------------------------------------------|------------------------------|------|-----|-----|------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                                                                                                                        | A [9DH[3:0]]<br>B [CDH[3:0]] |      |     |     | A [9CH[7:0]]<br>B [CCH[7:0]] |     |     |     |     |     |     |     |
|                                                                                                                                        | XD11                         | XD10 | XD9 | XD8 | XD7                          | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |
| No output                                                                                                                              | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| Odd lengths are allowed, but will be<br>filled up to even lengths                                                                      | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| Maximum possible number of input<br>pixels = 4095; note 2                                                                              | 1                            | 1    | 1   | 1   | 1                            | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

### Notes

- Reference for counting are luminance samples.
- If the desired output length is greater than the number of scaled output pixels, the last scaled pixel is repeated.

**Table 112** Vertical output window length; register set A [9EH[7:0]; 9FH[3:0]] and B [CEH[7:0]; CFH[3:0]]

| VERTICAL OUTPUT ACQUISITION<br>WINDOW DEFINITION NUMBER<br>OF DESIRED OUTPUT LINES IN<br>Y (VERTICAL) DIRECTION | CONTROL BITS                 |      |     |     |                              |     |     |     |     |     |     |     |
|-----------------------------------------------------------------------------------------------------------------|------------------------------|------|-----|-----|------------------------------|-----|-----|-----|-----|-----|-----|-----|
|                                                                                                                 | A [9FH[3:0]]<br>B [CFH[3:0]] |      |     |     | A [9EH[7:0]]<br>B [CEH[7:0]] |     |     |     |     |     |     |     |
|                                                                                                                 | YD11                         | YD10 | YD9 | YD8 | YD7                          | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 |
| No output                                                                                                       | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 1 pixel                                                                                                         | 0                            | 0    | 0   | 0   | 0                            | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| Maximum possible number of output<br>lines = 4095; note 1                                                       | 1                            | 1    | 1   | 1   | 1                            | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

### Note

- If the desired output length is greater than the number of scaled output lines, the processing is cut.

## 15.5.9 SUBADDRESSES A0H TO A2H

**Table 113** Horizontal prescaling; register set A [A0H[5:0]] and B [D0H[5:0]]

| HORIZONTAL INTEGER PRESCALING RATIO (XPSC) | CONTROL BITS D5 TO D0 |       |       |       |       |       |
|--------------------------------------------|-----------------------|-------|-------|-------|-------|-------|
|                                            | XPSC5                 | XPSC4 | XPSC3 | XPSC2 | XPSC1 | XPSC0 |
| Not allowed                                | 0                     | 0     | 0     | 0     | 0     | 0     |
| Downscale = 1                              | 0                     | 0     | 0     | 0     | 0     | 1     |
| Downscale = $\frac{1}{2}$                  | 0                     | 0     | 0     | 0     | 1     | 0     |
| ...                                        | ...                   | ...   | ...   | ...   | ...   | ...   |
| Downscale = $\frac{1}{63}$                 | 1                     | 1     | 1     | 1     | 1     | 1     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 114** Accumulation length; register set A [A1H[5:0]] and B [D1H[5:0]]

| HORIZONTAL PRESCALER ACCUMULATION<br>SEQUENCE LENGTH (XACL) | CONTROL BITS D5 TO D0 |       |       |       |       |       |
|-------------------------------------------------------------|-----------------------|-------|-------|-------|-------|-------|
|                                                             | XACL5                 | XACL4 | XACL3 | XACL2 | XACL1 | XACL0 |
| Accumulation length = 1                                     | 0                     | 0     | 0     | 0     | 0     | 0     |
| Accumulation length = 2                                     | 0                     | 0     | 0     | 0     | 0     | 1     |
| ...                                                         | ...                   | ...   | ...   | ...   | ...   | ...   |
| Accumulation length = 64                                    | 1                     | 1     | 1     | 1     | 1     | 1     |

**Table 115** Prescaler DC gain and FIR prefilter control; register set A [A2H[7:4]] and B [D2H[7:4]]; note 1

| FIR PREFILTER CONTROL                                        | CONTROL BITS D7 TO D4 |       |      |      |
|--------------------------------------------------------------|-----------------------|-------|------|------|
|                                                              | PFUV1                 | PFUV0 | PFY1 | PFY0 |
| Luminance FIR filter bypassed                                | X                     | X     | 0    | 0    |
| $H_y(z) = \frac{1}{4} (1 \ 2 \ 1)$                           | X                     | X     | 0    | 1    |
| $H_y(z) = \frac{1}{8} (-1 \ 1 \ 1.75 \ 4.5 \ 1.75 \ 1 \ -1)$ | X                     | X     | 1    | 0    |
| $H_y(z) = \frac{1}{8} (1 \ 2 \ 2 \ 2 \ 1)$                   | X                     | X     | 1    | 1    |
| Chrominance FIR filter bypassed                              | 0                     | 0     | X    | X    |
| $H_{uv}(z) = \frac{1}{4} (1 \ 2 \ 1)$                        | 0                     | 1     | X    | X    |
| $H_{uv}(z) = \frac{1}{32} (3 \ 8 \ 10 \ 8 \ 3)$              | 1                     | 0     | X    | X    |
| $H_{uv}(z) = \frac{1}{8} (1 \ 2 \ 2 \ 2 \ 1)$                | 1                     | 1     | X    | X    |

**Note**

1. X = don't care.

**Table 116** Prescaler DC gain and FIR prefilter control; register set A [A2H[3:0]] and B [D2H[3:0]]; note 1

| PRESCALER DC GAIN                                                                                          | CONTROL BITS D3 TO D0 |       |       |       |
|------------------------------------------------------------------------------------------------------------|-----------------------|-------|-------|-------|
|                                                                                                            | XC2_1                 | XDCG2 | XDCG1 | XDCG0 |
| Prescaler output is renormalized by gain factor = 1                                                        | X                     | 0     | 0     | 0     |
| Prescaler output is renormalized by gain factor = $\frac{1}{2}$                                            | X                     | 0     | 0     | 1     |
| Prescaler output is renormalized by gain factor = $\frac{1}{4}$                                            | X                     | 0     | 1     | 0     |
| Prescaler output is renormalized by gain factor = $\frac{1}{8}$                                            | X                     | 0     | 1     | 1     |
| Prescaler output is renormalized by gain factor = $\frac{1}{16}$                                           | X                     | 1     | 0     | 0     |
| Prescaler output is renormalized by gain factor = $\frac{1}{32}$                                           | X                     | 1     | 0     | 1     |
| Prescaler output is renormalized by gain factor = $\frac{1}{64}$                                           | X                     | 1     | 1     | 0     |
| Prescaler output is renormalized by gain factor = $\frac{1}{128}$                                          | X                     | 1     | 1     | 1     |
| Weighting of all accumulated samples is factor '1'; e.g. XACL = 4 $\Rightarrow$ sequence 1 + 1 + 1 + 1 + 1 | 0                     | X     | X     | X     |
| Weighting of samples inside sequence is factor '2'; e.g. XACL = 4 $\Rightarrow$ sequence 1 + 2 + 2 + 2 + 1 | 1                     | X     | X     | X     |

**Note**

1. X = don't care.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 15.5.10 SUBADDRESSES A4H TO A6H

**Table 117** Luminance brightness control; register set A [A4H[7:0]] and B [D4H[7:0]]

| LUMINANCE<br>BRIGHTNESS CONTROL | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|---------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                                 | BRIG7                 | BRIG6 | BRIG5 | BRIG4 | BRIG3 | BRIG2 | BRIG1 | BRIG0 |
| Value = 0                       | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Nominal value = 128             | 1                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Value = 255                     | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

**Table 118** Luminance contrast control; register set A [A5H[7:0]] and B [D5H[7:0]]

| LUMINANCE CONTRAST<br>CONTROL | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|-------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                               | CONT7                 | CONT6 | CONT5 | CONT4 | CONT3 | CONT2 | CONT1 | CONT0 |
| Gain = 0                      | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Gain = $\frac{1}{64}$         | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 1     |
| Nominal gain = 64             | 0                     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| Gain = $\frac{127}{64}$       | 0                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

**Table 119** Chrominance saturation control; register set A [A6H[7:0]] and B [D6H[7:0]]

| CHROMINANCE<br>SATURATION CONTROL | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|-----------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                                   | SATN7                 | SATN6 | SATN5 | SATN4 | SATN3 | SATN2 | SATN1 | SATN0 |
| Gain = 0                          | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Gain = $\frac{1}{64}$             | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 1     |
| Nominal gain = 64                 | 0                     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| Gain = $\frac{127}{64}$           | 0                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

## 15.5.11 SUBADDRESSES A8H TO AEH

**Table 120** Horizontal luminance scaling increment; register set A [A8H[7:0]; A9H[7:0]] and B [D8H[7:0]; D9H[7:0]]

| HORIZONTAL LUMINANCE<br>SCALING INCREMENT                               | CONTROL BITS                 |                              |                              |                              |
|-------------------------------------------------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
|                                                                         | A [A9H[7:4]]<br>B [D9H[7:4]] | A [A9H[3:0]]<br>B [D9H[3:0]] | A [A8H[7:4]]<br>B [D8H[7:4]] | A [A8H[3:0]]<br>B [D8H[3:0]] |
|                                                                         | XSCY[15:12] <sup>(1)</sup>   | XSCY[11:8]                   | XSCY[7:4]                    | XSCY[3:0]                    |
| Scale = $\frac{1024}{1}$ (theoretical) zoom                             | 0000                         | 0000                         | 0000                         | 0000                         |
| Scale = $\frac{1024}{294}$ , lower limit defined by data path structure | 0000                         | 0001                         | 0010                         | 0110                         |
| Scale = $\frac{1024}{1023}$ zoom                                        | 0000                         | 0011                         | 1111                         | 1111                         |
| Scale = 1, equals 1024                                                  | 0000                         | 0100                         | 0000                         | 0000                         |
| Scale = $\frac{1024}{1025}$ downscale                                   | 0000                         | 0100                         | 0000                         | 0001                         |
| Scale = $\frac{1024}{8191}$ downscale                                   | 0001                         | 1111                         | 1111                         | 1111                         |

**Note**

1. Bits XSCY[15:13] are reserved and are set to logic 0.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 121** Horizontal luminance phase offset; register set A [AAH[7:0]] and B [DAH[7:0]]

| HORIZONTAL LUMINANCE PHASE<br>OFFSET | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|--------------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                                      | XPHY7                 | XPHY6 | XPHY5 | XPHY4 | XPHY3 | XPHY2 | XPHY1 | XPHY0 |
| Offset = 0                           | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Offset = $\frac{1}{32}$ pixel        | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 1     |
| Offset = $\frac{32}{32} = 1$ pixel   | 0                     | 0     | 1     | 0     | 0     | 0     | 0     | 0     |
| Offset = $\frac{255}{32}$ pixel      | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

**Table 122** Horizontal chrominance scaling increment; register set A [ACH[7:0]; ADH[7:0]] and B [DCH[7:0]; DDH[7:0]]

| HORIZONTAL CHROMINANCE<br>SCALING INCREMENT                               | CONTROL BITS                 |                              |                              |                              |
|---------------------------------------------------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
|                                                                           | A [ADH[7:4]]<br>B [DDH[7:4]] | A [ADH[3:0]]<br>B [DDH[3:0]] | A [ACH[7:4]]<br>B [DCH[7:4]] | A [ACH[3:0]]<br>B [DCH[3:0]] |
|                                                                           | XSCC[15:12] <sup>(1)</sup>   | XSCC[11:8]                   | XSCC[7:4]                    | XSCC[3:0]                    |
| This value must be set to the<br>luminance value $\frac{1}{2}$ XSCY[15:0] | 0000                         | 0000                         | 0000                         | 0000                         |
|                                                                           | 0000                         | 0000                         | 0000                         | 0001                         |
|                                                                           | 0001                         | 1111                         | 1111                         | 1111                         |

**Note**

- Bits XSCC[15:13] are reserved and are set to logic 0.

**Table 123** Horizontal chrominance phase offset; register set A [AEH[7:0]] and B [DEH[7:0]]

| HORIZONTAL CHROMINANCE<br>PHASE OFFSET            | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|---------------------------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                                                   | XPHC7                 | XPHC6 | XPHC5 | XPHC4 | XPHC3 | XPHC2 | XPHC1 | XPHC0 |
| This value must be set to $\frac{1}{2}$ XPHY[7:0] | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
|                                                   | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 1     |
|                                                   | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

## 15.5.12 SUBADDRESSES B0H TO BFH

**Table 124** Vertical luminance scaling increment; register set A [B0H[7:0]; B1H[7:0]] and B [E0H[7:0]; E1H[7:0]]

| VERTICAL LUMINANCE SCALING<br>INCREMENT     | CONTROL BITS                 |                              |                              |                              |
|---------------------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
|                                             | A [B1H[7:4]]<br>B [E1H[7:4]] | A [B1H[3:0]]<br>B [E1H[3:0]] | A [B0H[7:4]]<br>B [E0H[7:4]] | A [B0H[3:0]]<br>B [E0H[3:0]] |
|                                             | YSCY[15:12]                  | YSCY[11:8]                   | YSCY[7:4]                    | YSCY[3:0]                    |
| Scale = $\frac{1024}{1}$ (theoretical) zoom | 0000                         | 0000                         | 0000                         | 0001                         |
| Scale = $\frac{1024}{1023}$ zoom            | 0000                         | 0011                         | 1111                         | 1111                         |
| Scale = 1, equals 1024                      | 0000                         | 0100                         | 0000                         | 0000                         |
| Scale = $\frac{1024}{1025}$ downscale       | 0000                         | 0100                         | 0000                         | 0001                         |
| Scale = $\frac{1}{63.999}$ downscale        | 1111                         | 1111                         | 1111                         | 1111                         |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 125** Vertical chrominance scaling increment; register set A [B2H[7:0]; B3H[7:0]] and B [E2H[7:0]; E3H[7:0]]

| VERTICAL CHROMINANCE<br>SCALING INCREMENT                   | CONTROL BITS                 |                              |                              |                              |
|-------------------------------------------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
|                                                             | A [B3H[7:4]]<br>B [E3H[7:4]] | A [B3H[3:0]]<br>B [E3H[3:0]] | A [B2H[7:4]]<br>B [E2H[7:4]] | A [B2H[3:0]]<br>B [E2H[3:0]] |
|                                                             | YSCC[15:12]                  | YSCC[11:8]                   | YSCC[7:4]                    | YSCC[3:0]                    |
| This value must be set to the<br>luminance value YSCY[15:0] | 0000                         | 0000                         | 0000                         | 0001                         |
|                                                             | 1111                         | 1111                         | 1111                         | 1111                         |

**Table 126** Vertical scaling mode control; register set A [B4H[4 and 0]] and B [E4H[4 and 0]]; note 1

| VERTICAL SCALING MODE CONTROL                                                               | CONTROL BITS D4 AND D0 |       |
|---------------------------------------------------------------------------------------------|------------------------|-------|
|                                                                                             | YMIR                   | YMODE |
| Vertical scaling performs linear interpolation between lines                                | X                      | 0     |
| Vertical scaling performs higher order accumulating interpolation, better alias suppression | X                      | 1     |
| No mirroring                                                                                | 0                      | X     |
| Lines are mirrored                                                                          | 1                      | X     |

**Note**

1. X = don't care.

**Table 127** Vertical chrominance phase offset '00'; register set A [B8H[7:0]] and B [E8H[7:0]]

| VERTICAL CHROMINANCE PHASE<br>OFFSET | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|--------------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                                      | YPC07                 | YPC06 | YPC05 | YPC04 | YPC03 | YPC02 | YPC01 | YPC00 |
| Offset = 0                           | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Offset = $\frac{32}{32} = 1$ line    | 0                     | 0     | 1     | 0     | 0     | 0     | 0     | 0     |
| Offset = $\frac{255}{32}$ lines      | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

**Table 128** Vertical luminance phase offset '00'; register set A [BCH[7:0]] and B [ECH[7:0]]

| VERTICAL LUMINANCE PHASE<br>OFFSET | CONTROL BITS D7 TO D0 |       |       |       |       |       |       |       |
|------------------------------------|-----------------------|-------|-------|-------|-------|-------|-------|-------|
|                                    | YPY07                 | YPY06 | YPY05 | YPY04 | YPY03 | YPY02 | YPY01 | YPY00 |
| Offset = 0                         | 0                     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Offset = $\frac{32}{32} = 1$ line  | 0                     | 0     | 1     | 0     | 0     | 0     | 0     | 0     |
| Offset = $\frac{255}{32}$ lines    | 1                     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 16 PROGRAMMING START SET-UP

### 16.1 Decoder part

The given values force the following behaviour of the SAA7114 decoder part:

- The analog input AI11 expects an NTSC M, PAL B, D, G, H and I or SECAM signal in CVBS format; analog anti-alias filter and AGC active
- Automatic field detection enabled
- Standard ITU 656 output format enabled on expansion (X) port
- Contrast, brightness and saturation control in accordance with ITU standards
- Adaptive comb filter for luminance and chrominance activated
- Pins LLC, LLC2, XTOUT, RTS0, RTS1 and RTCO are set to 3-state.

**Table 129** Decoder part start set-up values for the three main standards

| SUB ADDRESS (HEX) | REGISTER FUNCTION              | BIT NAME <sup>(1)</sup>                              | VALUES (HEX) |                      |       |
|-------------------|--------------------------------|------------------------------------------------------|--------------|----------------------|-------|
|                   |                                |                                                      | NTSC M       | PAL B, D, G, H AND I | SECAM |
| 00                | chip version                   | ID7 to ID4                                           | read only    |                      |       |
| 01                | increment delay                | X, X, X, X, IDEL3 to IDEL0                           | 08           | 08                   | 08    |
| 02                | analog input control 1         | FUSE1, FUSE0, GUDL1, GUDL0 and MODE3 to MODE0        | C0           | C0                   | C0    |
| 03                | analog input control 2         | X, HLNRS, VBSL, WPOFF, HOLDG, GAFIX, GAI28 and GAI18 | 10           | 10                   | 10    |
| 04                | analog input control 3         | GAI17 to GAI10                                       | 90           | 90                   | 90    |
| 05                | analog input control 4         | GAI27 to GAI20                                       | 90           | 90                   | 90    |
| 06                | horizontal sync start          | HSB7 to HSB0                                         | EB           | EB                   | EB    |
| 07                | horizontal sync stop           | HSS7 to HSS0                                         | E0           | E0                   | E0    |
| 08                | sync control                   | AUFD, FSEL, FOET, HTC1, HTC0, HPLL, VNOI1 and VNOI0  | 98           | 98                   | 98    |
| 09                | luminance control              | BYPS, YCOMB, LDEL, LUBW and LUF13 to LUF10           | 40           | 40                   | 1B    |
| 0A                | luminance brightness control   | DBRI7 to DBRI0                                       | 80           | 80                   | 80    |
| 0B                | luminance contrast control     | DCON7 to DCON0                                       | 44           | 44                   | 44    |
| 0C                | chrominance saturation control | DSAT7 to DSAT0                                       | 40           | 40                   | 40    |
| 0D                | chrominance hue control        | HUEC7 to HUEC0                                       | 00           | 00                   | 00    |
| 0E                | chrominance control 1          | CDTO, CSTD2 to CSTD0, DCVF, FCTC, X and CCOMB        | 89           | 81                   | D0    |
| 0F                | chrominance gain control       | ACGC and CGAIN6 to CGAIN0                            | 2A           | 2A                   | 80    |
| 10                | chrominance control 2          | OFFU1, OFFU0, OFFV1, OFFV0, CHBW and LCBW2 to LCBW0  | 0E           | 06                   | 00    |
| 11                | mode/delay control             | COLO, RTP1, HDEL1, HDEL0, RTP0 and YDEL2 to YDEL0    | 00           | 00                   | 00    |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

| SUB<br>ADDRESS<br>(HEX) | REGISTER<br>FUNCTION                           | BIT NAME <sup>(1)</sup>                                      | VALUES (HEX) |                         |       |
|-------------------------|------------------------------------------------|--------------------------------------------------------------|--------------|-------------------------|-------|
|                         |                                                |                                                              | NTSC M       | PAL B, D,<br>G, H AND I | SECAM |
| 12                      | RT signal control                              | RTSE13 to RTSE10 and<br>RTSE03 to RTSE00                     | 00           | 00                      | 00    |
| 13                      | RT/X port output control                       | RTCE, XRHS, XRVS1, XRVS0, HLSEL<br>and OFTS2 to OFTS0        | 00           | 00                      | 00    |
| 14                      | analog/ADC/compatibility<br>control            | CM99, UPTCV, AOSL1, AOSL0,<br>XTOUTE, OLDSB, APCK1 and APCK0 | 00           | 00                      | 00    |
| 15                      | VGATE start, FID change                        | VSTA7 to VSTA0                                               | 11           | 11                      | 11    |
| 16                      | VGATE stop                                     | VSTO7 to VSTO0                                               | FE           | FE                      | FE    |
| 17                      | miscellaneous, VGATE<br>configuration and MSBs | LLCE, LLC2E, X, X, X, VGPS,<br>VSTO8 and VSTA8               | 40           | 40                      | 40    |
| 18                      | raw data gain control                          | RAWG7 to RAWG0                                               | 40           | 40                      | 40    |
| 19                      | raw data offset control                        | RAWO7 to RAWO0                                               | 80           | 80                      | 80    |
| 1A to 1E                | reserved                                       | X, X, X, X, X, X, X, X                                       | 00           | 00                      | 00    |
| 1F                      | status byte video decoder<br>(OLDSB = 0)       | INTL, HLVLN, FIDT, GLIMT, GLIMB,<br>WIPA, COPRO and RDCAP    | read only    |                         |       |

**Note**

1. All X values must be set to logic 0.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 16.2 Audio clock generation part

The given values force the following behaviour of the SAA7114 audio clock generation part:

- Used crystal is 24.576 MHz
- Expected field frequency is 59.94 Hz (e.g. NTSC M standard)
- Generated audio master clock frequency at pin AMCLK is  $256 \times 44.1 \text{ kHz} = 11.2896 \text{ MHz}$
- AMCLK is externally connected to AMXCLK [short-cut between pins K12 (37) and J12 (41)]
- ASCLK =  $32 \times 44.1 \text{ kHz} = 1.4112 \text{ MHz}$
- ALRCLK is 44.1 kHz.

**Table 130** Audio clock part set-up values

| SUB ADDRESS (HEX) | REGISTER FUNCTION                                     | BIT NAME <sup>(1)</sup>             | START VALUES |   |   |   |   |   |   |       |
|-------------------|-------------------------------------------------------|-------------------------------------|--------------|---|---|---|---|---|---|-------|
|                   |                                                       |                                     | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 HEX |
| 30                | audio master clock cycles per field; bits D7 to D0    | ACPF7 to ACPF0                      | 1            | 0 | 1 | 1 | 1 | 1 | 0 | 0 BC  |
| 31                | audio master clock cycles per field; bits D15 to D8   | ACPF15 to ACPF8                     | 1            | 1 | 0 | 1 | 1 | 1 | 1 | 1 DF  |
| 32                | audio master clock cycles per field; bits D17 and D16 | X, X, X, X, X, X, ACPF17 and ACPF16 | 0            | 0 | 0 | 0 | 0 | 0 | 1 | 0 02  |
| 33                | reserved                                              | X, X, X, X, X, X, X, X              | 0            | 0 | 0 | 0 | 0 | 0 | 0 | 0 00  |
| 34                | audio master clock nominal increment; bits D7 to D0   | ACNI7 to ACNI0                      | 1            | 1 | 0 | 0 | 1 | 1 | 0 | 1 CD  |
| 35                | audio master clock nominal increment; bits D15 to D8  | ACNI15 to ACNI8                     | 1            | 1 | 0 | 0 | 1 | 1 | 0 | 0 CC  |
| 36                | audio master clock nominal increment; bits D21 to D16 | X, X, ACNI21 to ACNI16              | 0            | 0 | 1 | 1 | 1 | 0 | 1 | 0 3A  |
| 37                | reserved                                              | X, X, X, X, X, X, X, X              | 0            | 0 | 0 | 0 | 0 | 0 | 0 | 0 00  |
| 38                | clock ratio AMXCLK to ASCLK                           | X, X, SDIV5 to SDIV0                | 0            | 0 | 0 | 0 | 0 | 0 | 1 | 1 03  |
| 39                | clock ratio ASCLK to ALRCLK                           | X, X, LRDIV5 to LRDIV0              | 0            | 0 | 0 | 1 | 0 | 0 | 0 | 0 10  |
| 3A                | audio clock generator basic set-up                    | X, X, X, X, APLL, AMVR, LRPH, SCPH  | 0            | 0 | 0 | 0 | 0 | 0 | 0 | 0 00  |
| 3B to 3F          | reserved                                              | X, X, X, X, X, X, X, X              | 0            | 0 | 0 | 0 | 0 | 0 | 0 | 0 00  |

### Note

1. All X values must be set to logic 0.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 16.3 Data slicer and data type control part

The given values force the following behaviour of the SAA7114 VBI data slicer part:

- Closed captioning data are expected at line 21 of field 1 (60 Hz/525 line system)
- All other lines are processed as active video
- Sliced data are framed by ITU 656 like SAV/EAV sequence (DID[5:0] = 3EH  $\Rightarrow$  MSB of SAV/EAV = 1).

**Table 131** Data slicer start set-up values

| SUB ADDRESS (HEX) | REGISTER FUNCTION                                        | BIT NAME <sup>(1)</sup>                    | START VALUES       |   |   |   |   |   |   |   |                   |
|-------------------|----------------------------------------------------------|--------------------------------------------|--------------------|---|---|---|---|---|---|---|-------------------|
|                   |                                                          |                                            | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX               |
| 40                | slicer control 1                                         | X, HAM_N, FCE, HUNT_N, X, X, X, X          | 0                  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40                |
| 41 to 53          | line control register 2 to 20                            | LCRn_7 to LCRn_0 (n = 2 to 20)             | 1                  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF                |
| 54                | line control register 21                                 | LCR21_7 to LCR21_0                         | 0                  | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F                |
| 55 to 57          | line control register 22 to 24                           | LCRn_7 to LCRn_0 (n = 22 to 24)            | 1                  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF                |
| 58                | programmable framing code                                | FC7 to FC0                                 | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00                |
| 59                | horizontal offset for slicer                             | HOFF7 to HOFF0                             | 0                  | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47                |
| 5A                | vertical offset for slicer                               | VOFF7 to VOFF0                             | 0                  | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 <sup>(2)</sup> |
| 5B                | field offset and MSBs for horizontal and vertical offset | FOFF, RECODE, X, VOFF8, X, HOFF10 to HOFF8 | 1                  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 <sup>(2)</sup> |
| 5C                | reserved                                                 | X, X, X, X, X, X, X, X                     | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00                |
| 5D                | header and data identification code control              | FVREF, X, DID5 to DID0                     | 0                  | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E                |
| 5E                | sliced data identification code                          | X, X, SDID5 to SDID0                       | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00                |
| 5F                | reserved                                                 | X, X, X, X, X, X, X, X                     | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00                |
| 60                | slicer status byte 0                                     | –, FC8V, FC7V, VPSV, PPV, CCV, –, –        | read-only register |   |   |   |   |   |   |   |                   |
| 61                | slicer status byte 1                                     | –, –, F21_N, LN8 to LN4                    | read-only register |   |   |   |   |   |   |   |                   |
| 62                | slicer status byte 2                                     | LN3 to LN0, DT3 to DT0                     | read-only register |   |   |   |   |   |   |   |                   |

### Notes

1. All X values must be set to logic 0.
2. Changes for 50 Hz/625 line systems: subaddress 5AH = 03H and subaddress 5BH = 03H.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 16.4 Scaler and interfaces

Table 132 shows some examples for the scaler programming with:

- prsc = prescale ratio
- fisc = fine scale ratio
- vsc = vertical scale ratio.

The ratio is defined as:  $\frac{\text{number of input pixel}}{\text{number of output pixel}}$

In the following settings the VBI data slicer is inactive. To activate the VBI data slicer, VITX[1:0] 86H[7:6] has to be set to '11'. Depending on the VBI data slicer settings, the sliced VBI data is inserted after the end of the scaled video lines, if the regions of VBI data slicer and scaler overlaps.

To compensate the running-in of the vertical scaler, the vertical input window lengths are extended by 2 to 290 lines, respectively 242 lines for XS, but the scaler increment calculations are done with 288, respectively 240 lines.

### 16.4.1 TRIGGER CONDITION

For trigger condition STRC[1:0] 90H[1:0] not equal to '00'.

If the value of (YO + YS) is greater than or equal to 262 (NTSC), respectively 312 (PAL) the output field rate is reduced to 30 Hz, respectively 25 Hz.

Horizontal and vertical offsets (XO and YO) have to be used to adjust the displayed video in the display window. As this adjustment is application dependent, the listed values are only dummy values.

### 16.4.2 MAXIMUM ZOOM FACTOR

The maximum zoom factor is dependent on the back-end data rate and therefore back-end clock and data format dependent (8 or 16-bit output). The maximum horizontal zoom is limited to approximately 3.5, due to internal data path restrictions.

### 16.4.3 EXAMPLES

**Table 132** Example of configurations

| EXAMPLE NUMBER | SCALER SOURCE AND REFERENCE EVENTS                                                                                                                                                                                                                                                                                                           | INPUT WINDOW | OUTPUT WINDOW | SCALE RATIOS                               |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------------|--------------------------------------------|
| 1              | analog input to 8-bit I port output, with SAV/EAV codes, 8-bit serial byte stream decoder output at X port; acquisition trigger at falling edge vertical and rising edge horizontal reference signal; H and V gates on IGPH and IGPV, IGP0 = VBI sliced data flag, IGP1 = FIFO almost full, level $\geq 24$ , IDQ qualifier logic 1 active   | 720 × 240    | 720 × 240     | prsc = 1;<br>fisc = 1;<br>vsc = 1          |
| 2              | analog input to 16-bit output, without SAV/EAV codes, Y on I port, C <sub>B</sub> -C <sub>R</sub> on H port and decoder output at X port; acquisition trigger at falling edge vertical and rising edge horizontal reference signal; H and V-pulses on IGPH and IGPV, output FID on IGP0, IGP1 fixed to logic 1, IDQ qualifier logic 0 active | 704 × 288    | 768 × 288     | prsc = 1;<br>fisc = 0.91667;<br>vsc = 1    |
| 3              | X port input 8-bit with SAV/EAV codes, no reference signals on XRH and XRV, XCLK as gated clock; field detection and acquisition trigger on different events; acquisition triggers at rising edge vertical and rising edge horizontal; I port output 8-bit with SAV/EAV codes like example number 1                                          | 720 × 240    | 352 × 288     | prsc = 2;<br>fisc = 1.022;<br>vsc = 0.8333 |
| 4              | X port and H port for 16-bit Y-C <sub>B</sub> -C <sub>R</sub> 4 : 2 : 2 input (if no 16-bit output selected); XRH and XRV as references; field detection and acquisition trigger at falling edge vertical and rising edge horizontal; I port output 8-bit with SAV/EAV codes, but Y only output                                              | 720 × 288    | 200 × 80      | prsc = 2;<br>fisc = 1.8;<br>vsc = 3.6      |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

**Table 133** Scaler and interface configuration example

| I <sup>2</sup> C-BUS ADDRESS (HEX)                            | MAIN FUNCTIONALITY                                 | EXAMPLE 1 |     | EXAMPLE 2 |     | EXAMPLE 3 |     | EXAMPLE 4 |     |
|---------------------------------------------------------------|----------------------------------------------------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|
|                                                               |                                                    | HEX       | DEC | HEX       | DEC | HEX       | DEC | HEX       | DEC |
| Global settings                                               |                                                    |           |     |           |     |           |     |           |     |
| 80                                                            | task enable, IDQ and back-end clock definition     | 10        | –   | 10        | –   | 10        | –   | 10        | –   |
| 83                                                            | XCLK output phase and X port output enable         | 01        | –   | 01        | –   | 00        | –   | 00        | –   |
| 84                                                            | IGPH, IGPV, IGP0 and IGP1 output definition        | A0        | –   | C5        | –   | A0        | –   | A0        | –   |
| 85                                                            | signal polarity control and I port byte swapping   | 10        | –   | 09        | –   | 10        | –   | 10        | –   |
| 86                                                            | FIFO flag thresholds and video/text arbitration    | 45        | –   | 40        | –   | 45        | –   | 45        | –   |
| 87                                                            | ICLK and IDQ output phase and I port enable        | 01        | –   | 01        | –   | 01        | –   | 01        | –   |
| 88                                                            | power save control and software reset              | F0        | –   | F0        | –   | F0        | –   | F0        | –   |
| Task A: scaler input configuration and output format settings |                                                    |           |     |           |     |           |     |           |     |
| 90                                                            | task handling                                      | 00        | –   | 00        | –   | 00        | –   | 00        | –   |
| 91                                                            | scaler input source and format definition          | 08        | –   | 08        | –   | 18        | –   | 38        | –   |
| 92                                                            | reference signal definition at scaler input        | 10        | –   | 10        | –   | 10        | –   | 10        | –   |
| 93                                                            | I port output formats and configuration            | 80        | –   | 40        | –   | 80        | –   | 84        | –   |
| Input and output window definition                            |                                                    |           |     |           |     |           |     |           |     |
| 94                                                            | horizontal input offset (XO)                       | 10        | 16  | 10        | 16  | 10        | 16  | 10        | 16  |
| 95                                                            |                                                    | 00        | –   | 00        | –   | 00        | –   | 00        | –   |
| 96                                                            | horizontal input (source) window length (XS)       | D0        | 720 | C0        | 704 | D0        | 720 | D0        | 720 |
| 97                                                            |                                                    | 02        | –   | 02        | –   | 02        | –   | 02        | –   |
| 98                                                            | vertical input offset (YO)                         | 0A        | 10  | 0A        | 10  | 0A        | 10  | 0A        | 10  |
| 99                                                            |                                                    | 00        | –   | 00        | –   | 00        | –   | 00        | –   |
| 9A                                                            | vertical input (source) window length (YS)         | F2        | 242 | 22        | 290 | F2        | 242 | 22        | 290 |
| 9B                                                            |                                                    | 00        | –   | 01        | –   | 00        | –   | 01        | –   |
| 9C                                                            | horizontal output (destination) window length (XD) | D0        | 720 | 00        | 768 | 60        | 352 | C8        | 200 |
| 9D                                                            |                                                    | 02        | –   | 03        | –   | 01        | –   | 00        | –   |
| 9E                                                            | vertical output (destination) window length (YD)   | F0        | 240 | 20        | 288 | 20        | 288 | 50        | 80  |
| 9F                                                            |                                                    | 00        | –   | 01        | –   | 01        | –   | 00        | –   |

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

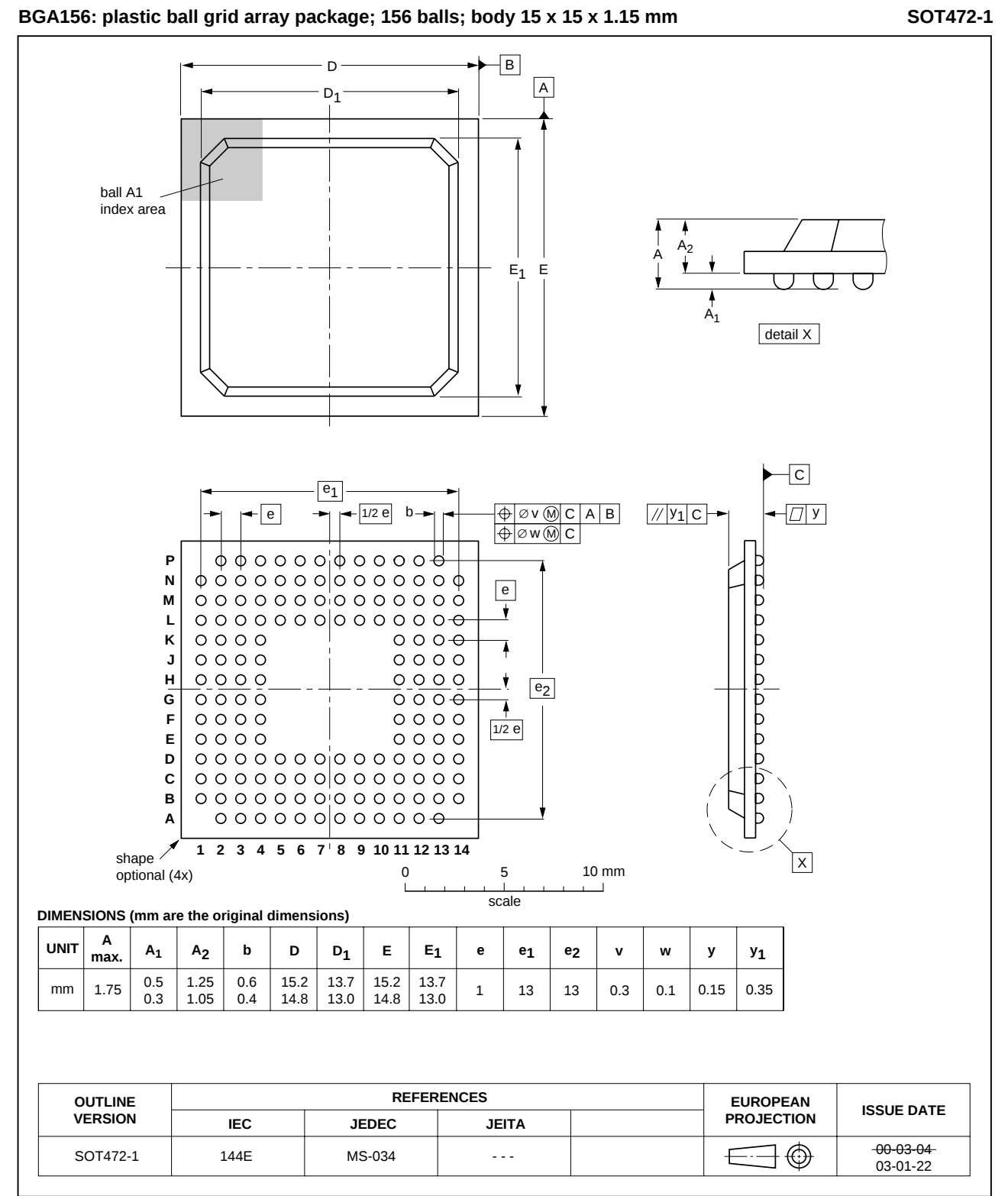
SAA7114

| I <sup>2</sup> C-BUS ADDRESS (HEX) | MAIN FUNCTIONALITY                                                                                     | EXAMPLE 1                                                                                                                    |      | EXAMPLE 2 |      | EXAMPLE 3 |      | EXAMPLE 4 |      |
|------------------------------------|--------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|------|-----------|------|-----------|------|-----------|------|
|                                    |                                                                                                        | HEX                                                                                                                          | DEC  | HEX       | DEC  | HEX       | DEC  | HEX       | DEC  |
| Prefiltering and prescaling        |                                                                                                        |                                                                                                                              |      |           |      |           |      |           |      |
| A0                                 | integer prescale (value '00' not allowed)                                                              | 01                                                                                                                           | –    | 01        | –    | 02        | –    | 02        | –    |
| A1                                 | accumulation length for prescaler                                                                      | 00                                                                                                                           | –    | 00        | –    | 02        | –    | 03        | –    |
| A2                                 | FIR prefilter and prescaler DC normalization                                                           | 00                                                                                                                           | –    | 00        | –    | AA        | –    | F2        | –    |
| A4                                 | scaler brightness control                                                                              | 80                                                                                                                           | 128  | 80        | 128  | 80        | 128  | 80        | 128  |
| A5                                 | scaler contrast control                                                                                | 40                                                                                                                           | 64   | 40        | 64   | 40        | 64   | 11        | 17   |
| A6                                 | scaler saturation control                                                                              | 40                                                                                                                           | 64   | 40        | 64   | 40        | 64   | 11        | 17   |
| Horizontal phase scaling           |                                                                                                        |                                                                                                                              |      |           |      |           |      |           |      |
| A8                                 | horizontal scaling increment for luminance                                                             | 00                                                                                                                           | 1024 | AA        | 938  | 18        | 1048 | 34        | 1844 |
| A9                                 |                                                                                                        | 04                                                                                                                           | –    | 03        | –    | 04        | –    | 07        | –    |
| AA                                 | horizontal phase offset luminance                                                                      | 00                                                                                                                           | –    | 00        | –    | 00        | –    | 00        | –    |
| AC                                 | horizontal scaling increment for chrominance                                                           | 00                                                                                                                           | 512  | D5        | 469  | 0C        | 524  | 9A        | 922  |
| AD                                 |                                                                                                        | 02                                                                                                                           | –    | 01        | –    | 02        | –    | 03        | –    |
| AE                                 | horizontal phase offset chrominance                                                                    | 00                                                                                                                           | –    | 00        | –    | 00        | –    | 00        | –    |
| Vertical scaling                   |                                                                                                        |                                                                                                                              |      |           |      |           |      |           |      |
| B0                                 | vertical scaling increment for luminance                                                               | 00                                                                                                                           | 1024 | 00        | 1024 | 55        | 853  | 66        | 3686 |
| B1                                 |                                                                                                        | 04                                                                                                                           | –    | 04        | –    | 03        | –    | 0E        | –    |
| B2                                 | vertical scaling increment for chrominance                                                             | 00                                                                                                                           | 1024 | 00        | 1024 | 55        | 853  | 66        | 3686 |
| B3                                 |                                                                                                        | 04                                                                                                                           | –    | 04        | –    | 03        | –    | 0E        | –    |
| B4                                 | vertical scaling mode control                                                                          | 00                                                                                                                           | –    | 00        | –    | 00        | –    | 01        | –    |
| B8 to BF                           | vertical phase offsets luminance and chrominance (need to be used for interlace correct scaled output) | start with B8 to BF at 00H, if there are no problems with the interlaced scaled output optimize according to Section 8.3.3.2 |      |           |      |           |      |           |      |

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

17 PACKAGE OUTLINES

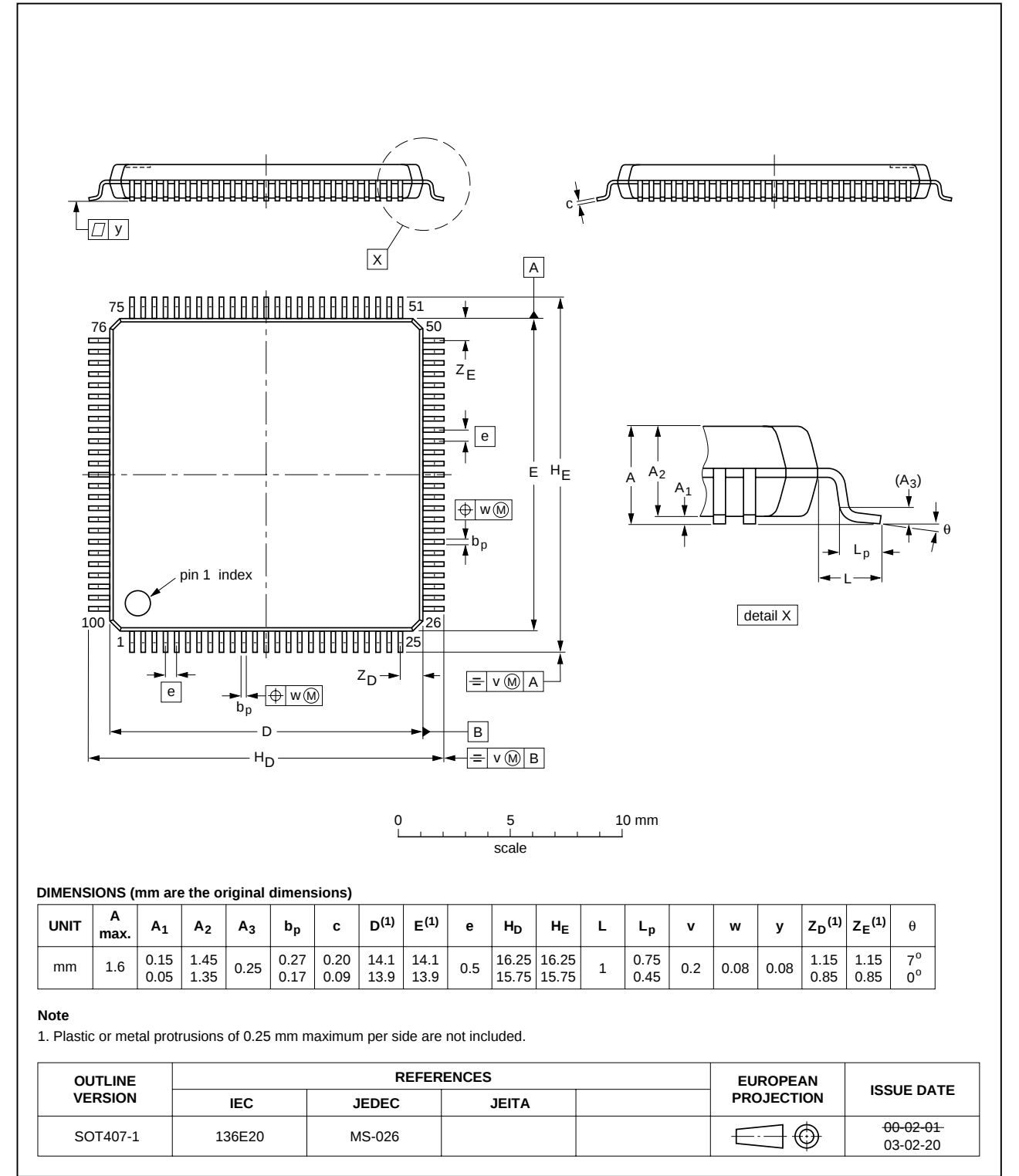


PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm

SOT407-1



# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 18 SOLDERING

### 18.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 18.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all the BGA packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 18.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### 18.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 18.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE <sup>(1)</sup>                                                   | SOLDERING METHOD                  |                       |
|--------------------------------------------------------------------------|-----------------------------------|-----------------------|
|                                                                          | WAVE                              | REFLOW <sup>(2)</sup> |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA                                     | not suitable                      | suitable              |
| DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable <sup>(3)</sup>       | suitable              |
| PLCC <sup>(4)</sup> , SO, SOJ                                            | suitable                          | suitable              |
| LQFP, QFP, TQFP                                                          | not recommended <sup>(4)(5)</sup> | suitable              |
| SSOP, TSSOP, VSO, VSSOP                                                  | not recommended <sup>(6)</sup>    | suitable              |

### Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

# PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC comb filter, VBI data slicer and high performance scaler

SAA7114

## 19 DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)(3)</sup> | DEFINITION                                                                                                                                                                                                                                                                                     |
|-------|----------------------------------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I     | Objective data                   | Development                      | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                    |
| II    | Preliminary data                 | Qualification                    | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
| III   | Product data                     | Production                       | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

### Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 20 DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 21 DISCLAIMERS

**Life support applications** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

---

PAL/NTSC/SECAM video decoder with adaptive PAL/NTSC  
comb filter, VBI data slicer and high performance scaler

---

SAA7114

## 22 PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

# ***Philips Semiconductors – a worldwide company***

## **Contact information**

For additional information please visit **<http://www.semiconductors.philips.com>**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: **[sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)**.

© Koninklijke Philips Electronics N.V. 2004

SCA76

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R21/02/pp147

Date of release: 2004 Mar 03

Document order number: 9397 750 11429

*Let's make things better.*

**Philips  
Semiconductors**



**PHILIPS**