Digital Automotive Pixel Link Transmitter

INAP125T12
INAP125T24

The INAP125T12/24 is a transmitter for the new **A**utomotive **PIX**el (APIX) link for display and camera based point-to-point applications. The APIX link features an uni-directional pixel and full-duplex sideband data transmission over one single pair of shielded twisted pair (STP) copper cable. The upstream sideband can also be transmitted over a separate pair of wires to serve the requirements for automotive applications. In addition this wire may be used for power supply.

The INAP125T12 video interface supports color widths of 10 and 12bit, the INAP125T24 widths of 10, 12, 18 and 24bit. The interface can be configured individually to match all popular display and image sensor interfaces. The pixel interface is able to handle a wide spread pixel clock for lowest EMI.

The INAP125T12/24 transmitter features dedicated high-speed outputs with adjustable drive current and pre-emphasis to facilitate the adaptation to different link distances and cable qualities while offering maximum data integrity and full EMI compliance.

Packages:

- 48 pin QFN (Quad-Flat No-Leads)
- 64 pin QFN

Features:

- Up to 1 GBit/s Downstream Link
- Up to 62.5 MBit/s Upstream Link
- Low EMI, Two- or Four-Wire Full Duplex Link
- Accepts wide spread spectrum pixel clock
- +15 m Distance with low profile STP cables
- 10/12/18/24 bit pixel Interface
- Configurable sampling edge for pixel data
- DC-balanced line coding to support AC coupling
- Line Driver Current and Pre-Emphasis adjustable
- ISO10605 and IEC61000-4-2 compliant ESD protection
- Extended Temp. Range: -40 to +105°C
- AEC-Q100 qualified

Applications:

- Automotive Infotainment Displays
- Automotive Dashboard Displays
- Head-Up Displays
- Rear-Seat Entertainment Systems
- Automotive Driver Assistance
- Surveillance Systems
- Inspection Systems

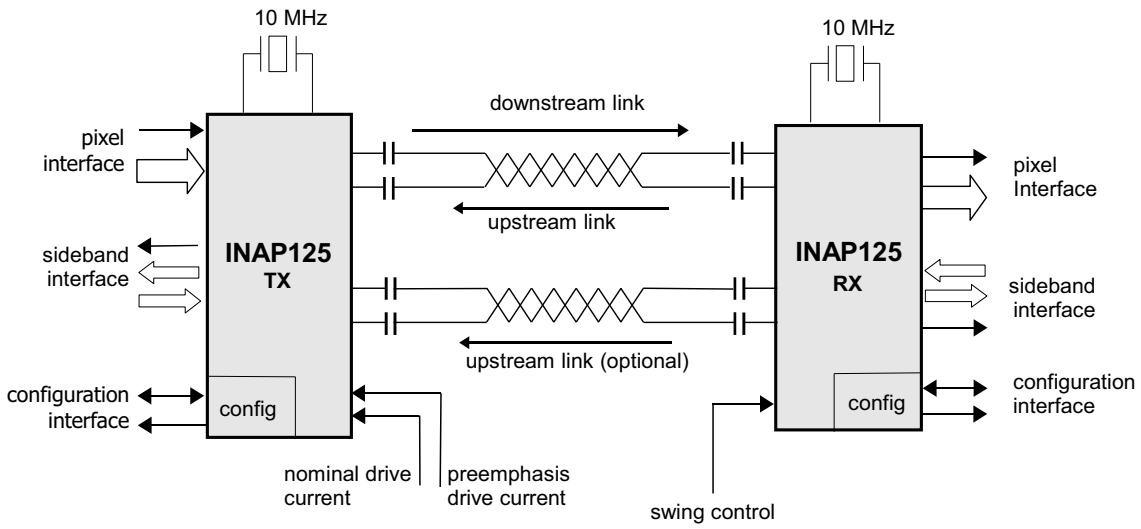


Figure 1: APIX system overview

1.0 Introduction

The APIX link transmits uncompressed pixel data with a sustained and resolution-independent link data rate of either 1 GBit/s or 500 MBit/s over one single pair of STP copper cable. In addition to the pixel data, bidirectional sideband control data can be transmitted over the same pair of wires.

The link supports distances of up to +15m (1 GBit/s mode) and up to +40m (500 MBit/s mode) depending on the output settings (current, pre-emphasis) and the cable properties.

Optimized for low EMI, the APIX link is dedicated for point-to-point applications within vehicles. The highly integrated architecture allows the implementation of video and audio links in applications like central information displays, dashboard and head-up displays, but also camera links as part of driver assistance systems requiring real-time digital video streams.

1.1 Transmission Channels

The APIX link provides three independent channels for data transfer

- the high speed downstream pixel channel
- the downstream sideband channel
- the upstream sideband channel

The pixel channel and the downstream sideband channel are multiplexed and commonly transmitted over the downstream link.

The upstream sideband channel can either be established over the same pair of wires as the downstream link (embedded upstream channel) or alternatively over a separate pair of wires. The configuration needs to be performed by the configuration vectors (see section 3.1).

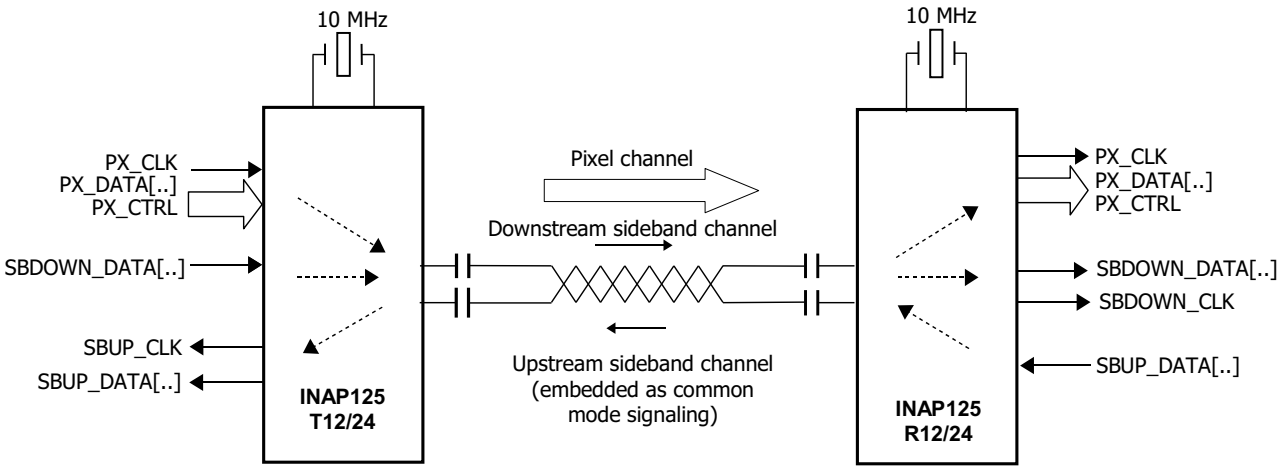


Figure 1-1: Single wire transmission channel configuration

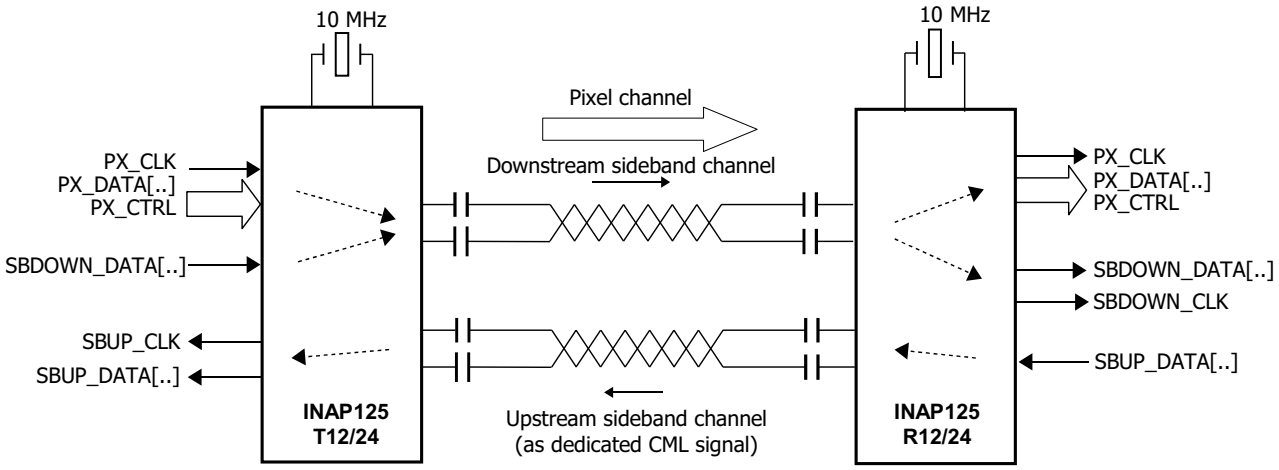


Figure 1-2: Two wire transmission channel configuration

1.2 Link Bandwidth

The bandwidth of the downstream link can be selected from these two modes:

- “full bandwidth” mode with a link data rate of 1 GBit/s, providing a net video data rate of 847MBit/s
- “half bandwidth” mode with a link data rate of 500 MBit/s, providing a net video data rate of 423.6MBit/s

The bandwidth also defines the maximum data rate possible for the sideband channels. The downstream sideband channel is transmitted in dedicated slots in the downstream link and therefore offers guaranteed low latency real-time characteristics. The maximum transmission rates is defined by the sampling frequency of the input pins as defined in section 2.3.2.

The upstream sideband channel is transmitted either as common mode signal on the same or as differential signal on a separate line (see Figure 1-2). The upstream channel data rate is configurable by configuration vectors as defined in section 3.1 and is not affected by the signalling method chosen for the upstream sideband channel.

2.0 Functional Description

2.1 Block Diagram

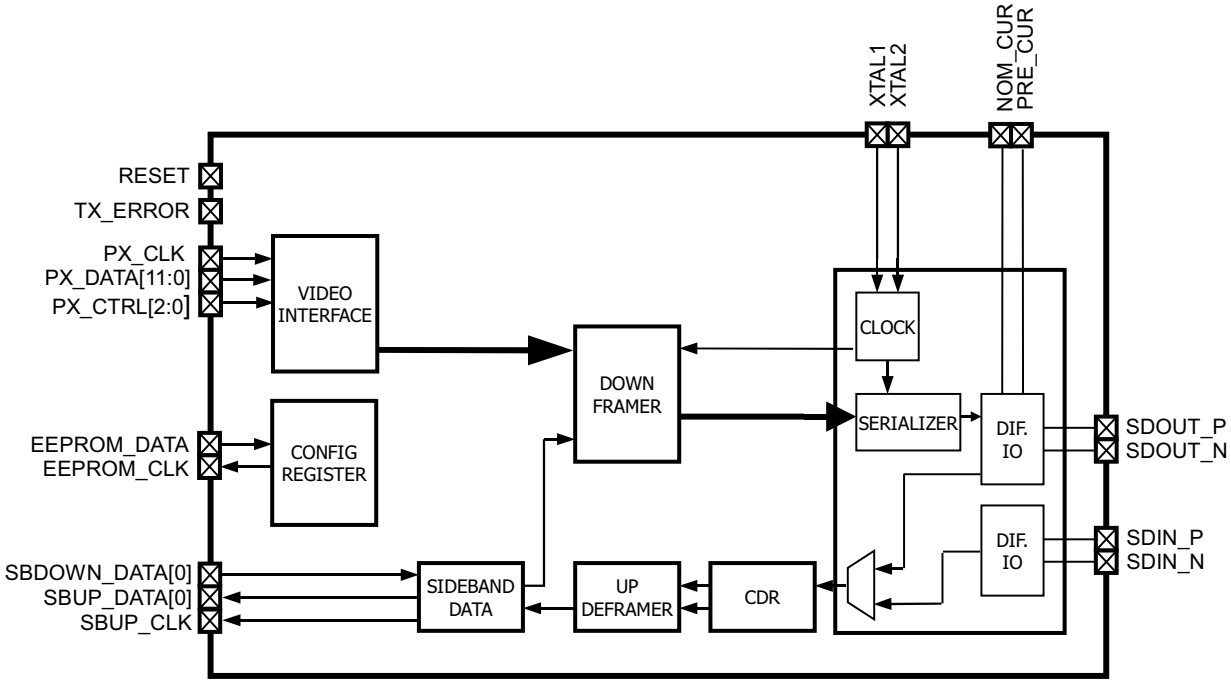


Figure 2-1: INAP125T12 Block Diagram

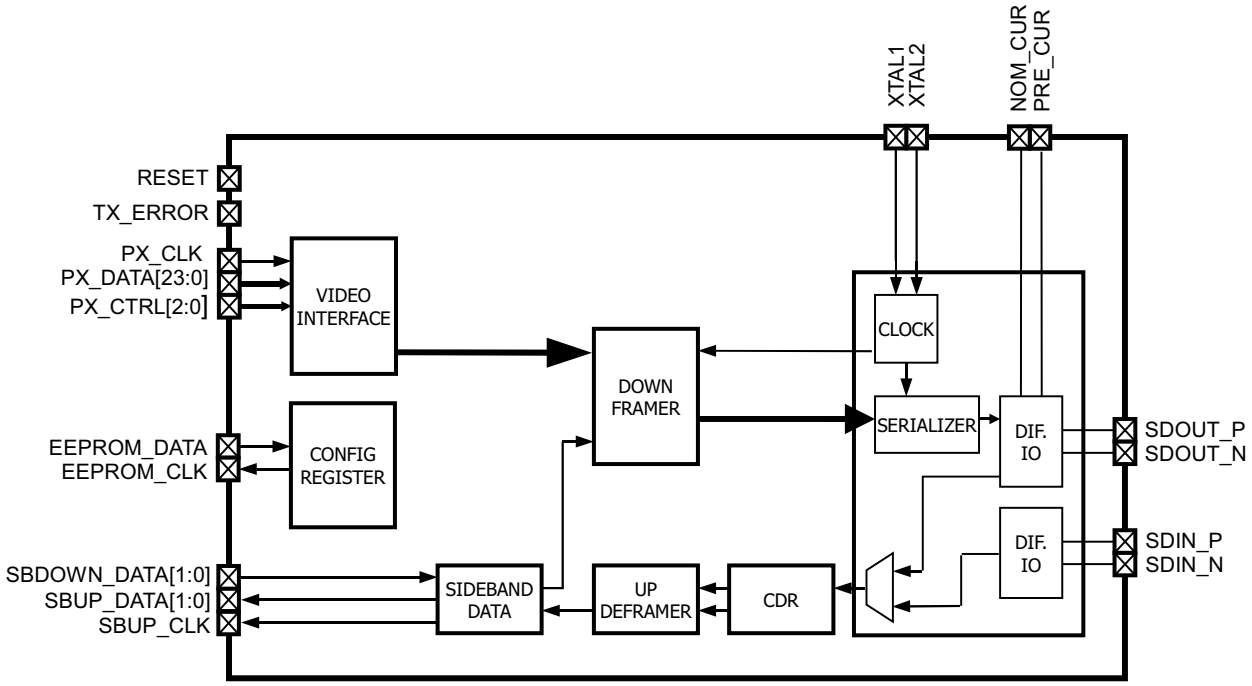


Figure 2-2: INAP125T24 Block Diagram

2.2 Serial Link Interfaces

2.2.1 Downstream Link Interface

The interface (SDOUT+, SDOUT-) of the downstream serial link (Tx -> Rx) is implemented with differential Current Mode Logic (CML).

2.2.2 Upstream Link Interface

As the upstream serial channel (from Rx to Tx) can alternatively be established over the downlink (embedded back channel) or a separate pair of STP cable, different signalling techniques will be employed.

Option 1: Upstream and downstream channels share the same pair of STP cable. The upstream link employs common mode signalling technique.

Option 2: Upstream and downstream channels are transmitted over 2 separate pairs of STP cable. The additional upstream interface of the APIX devices (SDIN+, SDIN-) is realized with differential Current Mode Logic (CML).

2.3 Digital Interfaces

2.3.1 Pixel Data Interface

The pixel data interface is the input for the 24 bit parallel pixel data representing the video data. In addition 3 pixel control signals like HSYNC, VSYNC and DATA ENABLE can be transmitted. The interface needs to be driven by an external pixel clock at PX_CLK, which acts as synchronous clock for the interface. The pixel clock is limited to 62 MHz as specified in Table 7-5. Data width and the configuration for the pixel control data are defined by configuration vectors (see section 3.1).

Channels		**control signal transmit mode configuration of transmission of pixel control signals**		
Downstream	**PX_DATA Width**	**never**	**even pixels only**	**each pixel**
Bandwidth mode 1GBit/s	10 bit	62.0 MHz	62.0 MHz	62.0 MHz
	12 bit	62.0 MHz	62.0 MHz	56.4 MHz
	18 bit	47.0 MHz	43.4 MHz	40.3 MHz
	24 bit	35.3 MHz	33.2 MHz	31.3 MHz
Bandwidth mode 500MBit/s	10 bit	42.3 MHz	36.8 MHz	32.5 MHz
	12 bit	35.2 MHz	31.3 MHz	28.2 MHz
	18 bit	23.5 MHz	21.7 MHz	20.1 MHz
	24 bit	17.6 MHz	16.6 MHz	15.6 MHz

Table 2-1: Maximum pixel clock frequency for different PX_CTRL and data width settings

The parallel pixel interface supports pixel formats of 10, 12, 18 and 24 bit + 3 control signals. Pixel data and control signals are sampled with the pixel clock. The active edge can be configured to either rising or falling.

It is recommended to consider series resistors for all PX_DATA, PX_CTRL and PX_CLK input pins close to the video source device to reduce the risk of data-related emissions and reflections.

Color Depth	INAP125T12[a]	INAP125T24
10 Bit	PX_DATA[9:0]	PX_DATA[9:0]
12 Bit	PX_DATA[11:0]	PX_DATA[11:0]
18 Bit	-	PX_DATA[17:0]
24 Bit	-	PX_DATA[23:0]

Table 2-2: Pixel data interface options

a. 18 and 24 bit configurations also possible for INAP125T12 devices, most significant bits PX_DATA[23:12] internally pulled low.

Control Function	INAP125T12	INAP125T24
HSYNC / lineSync	PX_CTRL[0]	PX_CTRL[0]
VSYNC / frameSync	PX_CTRL[1]	PX_CTRL[1]
DATA ENABLE / valid	PX_CTRL[2]	PX_CTRL[2]

Table 2-3: Pixel control interface

Please note that PX_CTRL[2] is required by the APIX link to synchronize the serial transmission to the pixel data. Therefore it is mandatory to toggle the pin at least once at the beginning of the transmission to ensure the correct operation of the APIX link.

2.3.2 Sideband Channel Downstream Interface

The sideband data downstream interface provides either one (INAP125T12) or two (INAP125T24) input pins to sample sideband data. Both pins are sampled at a specific frequency and transmitted as 2 bit data packet. The sampling frequency depends on the bandwidth mode selected for the downstream link as shown in Table 2-4.

Downstream speed	Sampling frequency	Input pins	
		INAP125T12	INAP125T24
1 GBit/s	13.89 MHz	SBDOWN_DATA[0]	SBDOWN_DATA[1:0]
500 MBit/s	6.94 MHz		

Table 2-4: Downstream Sideband channel sampling frequency

2.3.3 Sideband Channel Upstream Interface

The sideband data upstream interface provides the sideband data at either one (INAP125T12) or two (INAP125T24) output pins. The pins are provided synchronously to SBUP_CLK, which reflects the upstream sample clock at the INAP125R12/24 receiver devices. The maximum data rate is limited by the upstream serial line clock, which is defined by a configuration vector (see Table 3-1). Please see Table 2-5 for a complete list of available data rates.

Upstream Serial Line Clock	Maximum Output data rate (per pin)	Output pins	
		INAP125T12	INAP125T24
62.5 MHz	<10.40 MBit/s	SBUP_DATA[0]	SBUP_DATA[1:0]
41.61 MHz	<6.94 MBit/s		
31.25 MHz	<5.20 MBit/s		
20.83 MHz	<3.48 MBit/s		

Table 2-5: Upstream sideband channel data rate with INAP125R12/24 receiver

2.4 Signal Description

Note: Unused CMOS inputs should be tied to GND.
For thermal and functional reasons the exposed die attach pad must be connected to GND.

Signal Name	Pin #	Type	Description
PX_DATA[11:0]	13,1,11, 10,9,8,7,6, 5,4,3,2	IN	Pixel data input, sampled with respect to the rising or falling edge of PX_CLK. Inputs should be connected via series resistors.
PX_CLK	12	IN	Pixel clock input
PX_CTRL[2:0]	43,44,45	IN	Pixel control signals
SBDOWN_DATA[0]	17	IN	Downstream sideband data
SBUP_DATA[0]	18	OUT	Upstream sideband data
SBUP_CLK	24	OUT	Sideband channel upstream clock
RESET#	16	IN	Asynchronous reset (active low)
TX_ERROR	23	OUT	Upstream Link Sync Error Indicator (active high)
EEPROM_DATA	20	IN/OUT	Configuration data
EEPROM_CLK	19	OUT	Configuration clock
XTAL_IN	40	IN	Oscillator input or reference clock input
XTAL_OUT	39	OUT	Oscillator output
NOM_CUR	28	PASSIV	Serial Downstream: Nominal current control

Table 2-6: INAP125T12 Pinout description, 48-pin QFN

Signal Name	Pin #	Type	Description
PRE_CUR	29	PASSIV	Serial Downstream: Pre-emphasis current control
SDOUT+	32	OUT	CML serial data interface downstream. Interface to differential transmission line with Zdiff = 100 Ohm.
SDOUT-	33	OUT	
SDIN+	35	IN	CML serial data interface upstream. Interface to differential transmission line with Zdiff = 100 Ohm. Leave open if not used.
SDIN-	36	IN	
VCO_TUNE	27	IN	VCO loop filter tuning voltage
PFD_OUT	26	OUT	Current output for VCO loop filter
VDD	14, 47	PWR	1.8 V core supply
DVDD	22	PWR	3.3 V I/O supply
VDD_VCO	25	PWR	Regulated power supply for VCO 1.8 V, 7 mA
VDDA	34	PWR	1.8 V analog supply
VDD_OSC	41	PWR	1.8 V oscillator supply
DVDD_OSC	37	PWR	3.3 V oscillator supply
VSS[a]	15, 46	GND	Digital core ground
DVSS[a]	21,48	GND	Digital I/O ground
GNDA[a]	31	GND	Analog ground
VSS_OSC[a]	42	GND	Oscillator ground
DVSS_OSC[a]	38	GND	Oscillator I/O ground
NC	30		not connected
Exposed Dia Attach Pad	-	GND	Connection to GND with multiple VIAs

Table 2-6: INAP125T12 Pinout description, 48-pin QFN

a. All VSS, DVSS and GND pins should be connected as common ground

Signal Name	Pin #	Type	Description
PX_DATA[23:0]	35,32,18,17,16,62,37,36,61,31,60,19,15,1,13,12,11,10,9,6,5,4,3,2	IN	Pixel data input, sampled with respect to the rising or falling edge of PX_CLK. Inputs should be connected via series resistors.
PX_CLK	14	IN	Pixel clock input
PX_CTRL[2:0]	55,56,57	IN	Pixel control signals

Table 2-7: INAP125T24 Pin description, 64-pin QFN

Signal Name	Pin #	Type	Description
SBDOWN_DATA[1:0]	34,23	IN	Downstream sideband data
SBUP_DATA[1:0]	33,24	OUT	Upstream sideband data
SBUP_CLK	30	OUT	Sideband channel upstream clock
RESET#	22	IN	Asynchronous reset (active low)
TX_ERROR	29	OUT	Upstream Link Sync Error Indicator (active high)
EEPROM_DATA	26	IN/OUT	Configuration data
EEPROM_CLK	25	OUT	Configuration clock
XTAL_IN	52	IN	Oscillator input or reference clock input
XTAL_OUT	51	OUT	Oscillator output
NOM_CUR	41	PASSIV	Serial Downstream: Nominal current control
PRE_CUR	42	PASSIV	Serial Downstream: Pre-emphasis current control
SDOUT+	44	OUT	CML serial data interface downstream. Interface to differential transmission line with Zdiff = 100 Ohm.
SDOUT-	45	OUT	
SDIN+	47	IN	CML serial data interface upstream. Interface to differential transmission line with Zdiff = 100 Ohm.
SDIN-	48	IN	
VCO_TUNE	40	IN	VCO loop filter tuning voltage
PFD_OUT	39	OUT	Current output for VCO loop filter
VDD_VCO	38	PWR	Regulated power supply for VCO 1.8 V, 7 mA
VDD	7,20,59	PWR	1.8 V core supply
DVDD	28,64	PWR	3.3 V I/O supply
VDDA	46	PWR	1.8 V analog supply
VDD_OSC	53	PWR	1.8 V oscillator supply
DVDD_OSC	49	PWR	3.3 V oscillator supply
VSS[a]	8,21,58	GND	Digital core ground
DVSS[a]	27,63	GND	Digital I/O ground
GNDA[a]	43	GND	Analog ground
VSS_OSC[a]	54	GND	Oscillator ground
DVSS_OSC[a]	50	GND	Oscillator I/O ground
Exposed Dia Attach Pad	-	GND	Connection to GND with multiple VIAs

Table 2-7: INAP125T24 Pin description, 64-pin QFN

a. All VSS, DVSS and GND pins should be connected as common ground

3.0 Configuration, Reset, Power-Up and Error Detection

3.1 Configuration

The device parameters and settings are configured through a two-wire serial interface which is compatible to the MicroChip MicroWire™ interface. After power-up or reset, the INAP125T12/24 expects a serial EEPROM at the interface EEPROM_DATA and EEPROM_CLK, to read in the configuration vectors. In case no EEPROM is used, the chip needs to be stimulated with the PROM_start and PROM_stop bytes as shown in Table 3-1. If the initialization fails the default values will be used. Please see section 3.1.2 for more details on the programming flow.

3.1.1 Configuration vectors

Address byte	Bit#	Parameter	Recommended value	Default value	Comment
00	7:0	PROM_start	10111101		PROM valid byte 0
01	2:0	pre-emphasis control	000	000	regulates the delay until pre-emphasis gets active. 000 means pre-emphasis active with first bit. (recommended)
	3	dedicated upstream		0	0: enable dedicated upstream link 1: disable Note: in case bit 3 and 4 are set to '0', the upstream channel is disabled
	4	embedded upstream		1	0: enable embedded upstream link 1: disable Note: in case bit 3 and 4 are set to '0', the upstream channel is disabled
	5	reserved	1	1	reserved
	6	bandwidth mode		0	0: 500 MBit/s mode 1: 1 GBit/s mode
	7	wait period after configuration	1	1	0: no delay 1: 50 ms delay after configuration to stabilize the PLL
02	1:0	pixel data width[a]		00	selects the width of pixel data to be transmitted 00: 10 bit 01: 12 bit 10: 18 bit 11: 24 bit

Table 3-1: Configuration vectors

Address byte	Bit#	Parameter	Recommended value	Default value	Comment
	3:2	control signal transmit mode	11	11	transmission of pixel control signals 00: never 01: unused 10: on every second (even) pixels 11: on each pixel
	4	reserved	1	1	
	5	pixel clock active edge		1	0: falling edge 1: rising edge
	7:6	upstream serial link clock		10	See Table 3-2 and Table 3-3
03	3:0	upstream link data recovery		0001	See Table 3-4
	4	reserved	0	0	
	7:5	TX_Error con-fig		000	Configuration of TX_Error pin See Table 3-5
04	0	pll status	0	0	loss of PLL synchronization resets device 0: enable 1: disable
	4:1	reserved	1000	1000	
	7:5	reserved	100	100	
05	7:0	PROM_end	10011001		PROM valid byte 1

Table 3-1: Configuration vectors

a. 18 and 24 bit configurations also possible for INAP125T12 devices, most significant bits PX_DATA[23:12] internally pulled low.

Bandwidth mode	Configuration Byte 2, Bit 7:6	Upstream serial line clock
1 Gbit/s	00	62.5 MHz
1 Gbit/s	01	41.67 MHz
1 Gbit/s	10	31.25 MHz

Table 3-2: Sideband upstream configuration for full bandwidth mode

Bandwidth mode	Configuration Byte 2, Bit 7:6	Upstream serial line clock
500 MBit/s	00	62.5 MHz
500 MBit/s	10	31.25 MHz
500 MBit/s	11	20.83 MHz

Table 3-3: Sideband upstream configuration for half bandwidth mode

Upstream serial line clock	Configuration Byte 3, Bit 3:0
62.5 MHz	0011
41.67 MHz	0001
31.25 MHz	0001
20.83 MHz	0011

Table 3-4: Upstream link data recovery configuration

Status	Configuration Byte 3, Bit 7:5	Comment
SBUP_Error	000	Loss of upstream synchronization
SBUP_Restart	001	Upstream synchronization restarted
(reserved)	010:111	

Table 3-5: TX Error pin configuration

3.1.2 Configuration procedure

The configuration of the INAP125T12/24 is performed through the MicroWire™ compatible interface. In general, the configuration may be performed by connecting a standard EEPROM or by serving the data from a micro controller or FPGA. The INAP125T12/24 expects the configuration vector data in 8-bit data format. In case of invalid PROM_start or PROM_end bytes, the devices uses the default values.

Please see Figure 3-1 for the general communication flow.

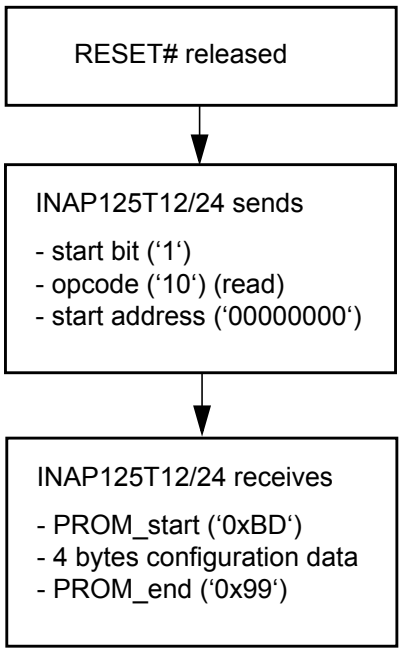


Figure 3-1: Configuration Flow

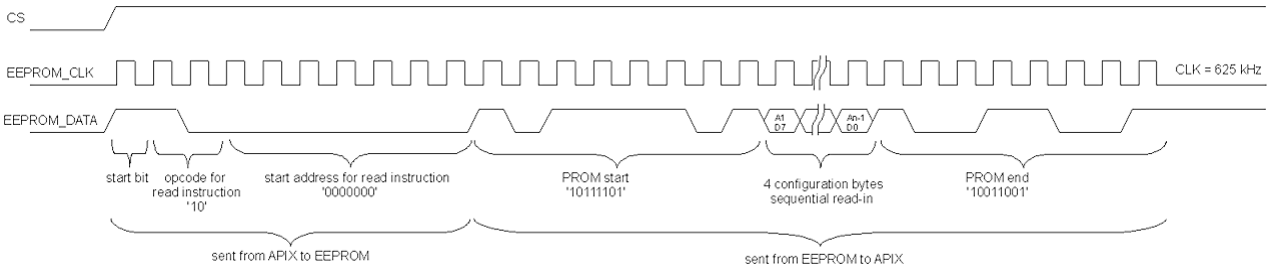


Figure 3-2: Configuration Interface Timing

Recommended EEPROMs are the 93L46A or 93L46C from Microchip Technology Inc. with selected word size of 8 bit. Since the INAP125T12/24 does not provide a dedicated CS signal, the EEPROM needs to support to send all data on just one rising edge of CS as shown in Figure 3-2. Please see Figure 3-3 for a typical connection circuitry for the EEPROM.

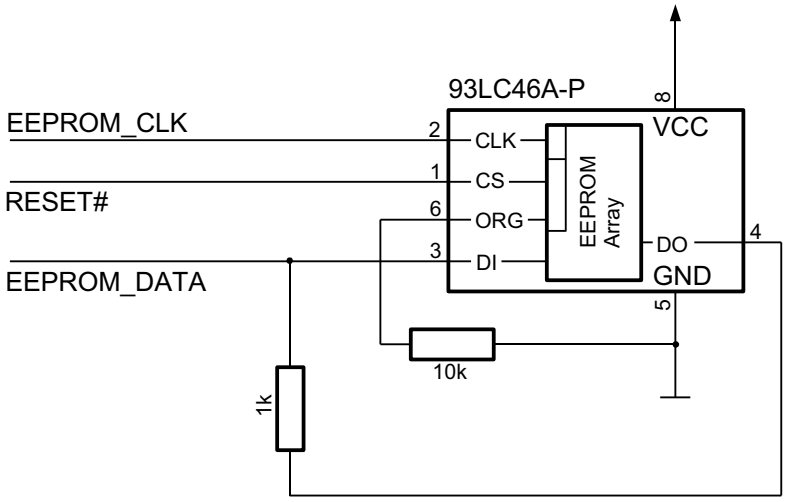


Figure 3-3: EEPROM connection circuitry

In order to connect the INAP125T12/24 configuration interface to the host controller, the host needs to be able to accept the interface clock from the APIX device.

Please note: The INAP125T12/24 is only able to respond to the PROM_Start and PROM_End command. No other Microwire commands supported.

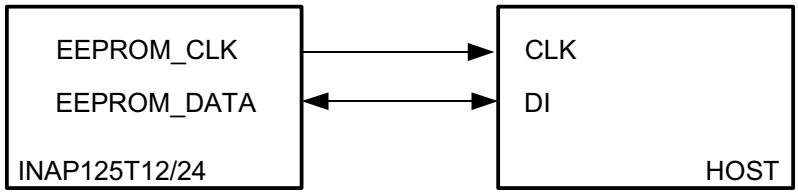


Figure 3-4: Host Connection diagram

3.2 Reset

The Reset pin triggers an asynchronous reset (active low) which sets all digital blocks of the INAP125T12/24 into a defined state. The configuration vectors are reset to the default values. The minimum low pulse width of the reset signal is 4 reference clock cycles.

During reset the serial output pins SDOUT-, SDOUT+ are held on VDDA level. All parallel outputs pins are at low level. EEPROM_DATA is set to Hi-Z.

3.3 Power-Up

3.3.1 Power-Up Sequence and Timing

The INAP125T12/24 tolerates the supply voltages to be ramped simultaneously. To avoid high IO currents, 1.8V supply voltages should ramp before 3.3V on power-up. On power-down, 3.3V should be powered down before 1.8V. On power-up all supply voltages have to rise steadily from GND level up to the VCC_{MIN} level without turn to negative direction. The ramping times must be within the limits as specified in Table 3-6. All 1.8V supplies have to be ramped up simultaneously starting from GND according figure 3.5. Reset has to be held low until all supplies reached recommended operating conditions.

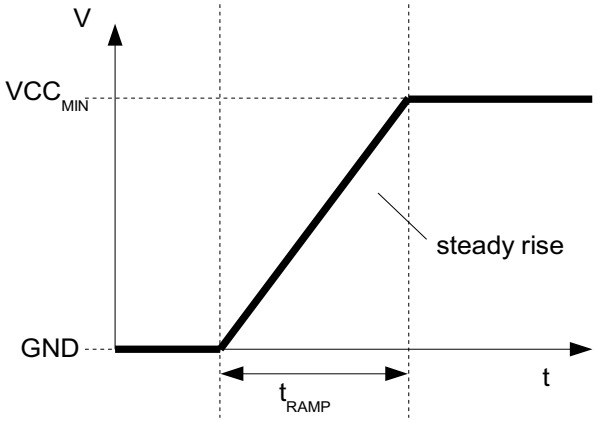


Figure 3-5: Steady voltage ramp-up

Parameter	Description	Min.	Typ.	Max.	Unit
t_{RAMP}	Supply Ramp Up Time for all supplies GND to VCC_{min}	0.05	1	10	ms

Table 3-6: Power supply ramp-up time

3.3.2 Power Supply Filtering

To achieve best transmission performance a noise level of less than 50mV on all analog and digital supply voltages VDD, VDDA, VDD_OSC and DVDD is recommended. The loop filter supply VDD_VCO requires lowest possible noise for best performance. See also section 6.0 for recommendations on power supply filtering.

3.4 Error detection

The INAP125T12/24 device includes an automatic error detection, which, with upstream channel enabled, indicates an upstream link synchronization error on pin TX_ERROR. The TX_ERROR output can be configured to different options using configuration vectors as described in section 3.1.

4.0 Electrical Specification

4.1 Interface Timing

4.1.1 Pixel Interface

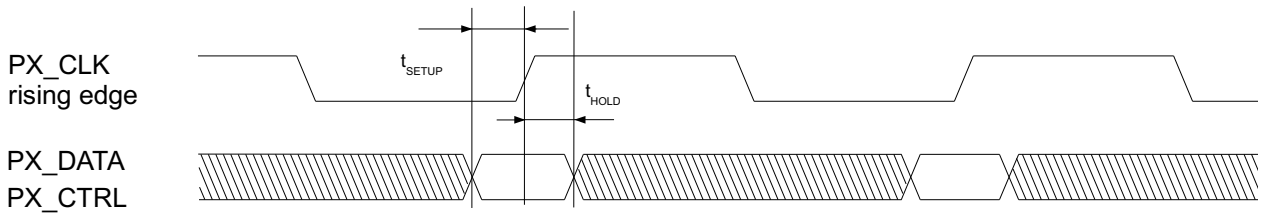


Figure 4-1: Pixel Interface timing at rising edge

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SETUP}	Pixel data and control signal setup time to pixel clock	1.5	2	-	ns
t_{HOLD}	Pixel data and control signal hold time to pixel clock	1	-	-	ns

Table 4-1: Pixel interface timing at rising edge

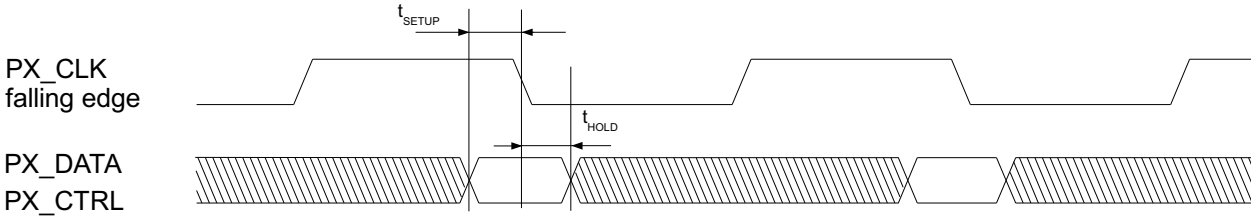


Figure 4-2: Pixel interface timing at falling edge

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SETUP}	Pixel data and control signal setup time to pixel clock	1.5	2	-	ns
t_{HOLD}	Pixel data and control signal hold time to pixel clock	1	-	-	ns

Table 4-2: Pixel interface timing at falling edge

4.1.2 Sideband Interface Timing

The upstream interface clock SBUP_CLK provides the internal sampling clock used at the APIX receiver to sample the data at SBUP_DATA[1:0]. In general the clock is defined as 1/3 of the upstream serial line clock as defined in Table 2-5. Due to the framing structure of the upstream link, the sideband clock is not available every 16th clock cycle as shown in Figure 4-3.

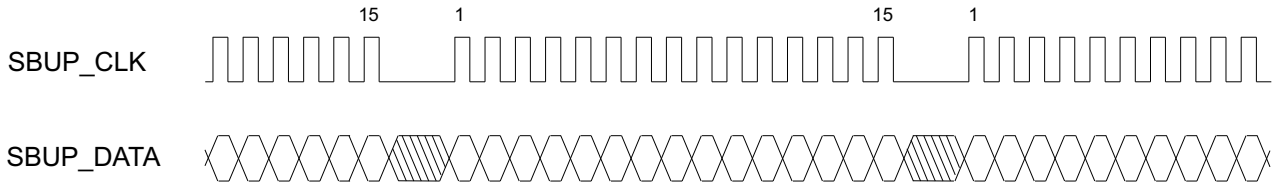


Figure 4-3: Upstream sideband interface

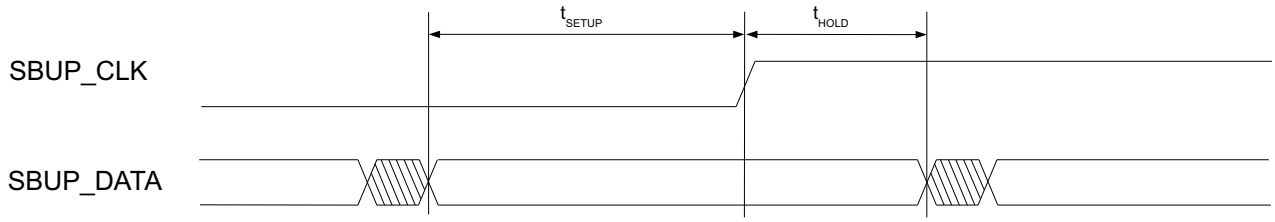


Figure 4-4: Upstream sideband Interface Timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SETUP}	Sideband data setup time to sideband clock	-	60	-	ns
t_{HOLD}	Sideband data hold time to sideband clock	-	60	-	ns

Table 4-3: Upstream sideband Interface Timing at 20.83MHz upstream serial line clock

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SETUP}	Sideband data setup time to sideband clock	-	40	-	ns
t_{HOLD}	Sideband data hold time to sideband clock	-	40	-	ns

Table 4-4: Upstream Interface Timing at 31.25MHz upstream serial line clock

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SETUP}	Sideband data setup time to sideband clock	-	30	-	ns
t_{HOLD}	Sideband data hold time to sideband clock	-	30	-	ns

Table 4-5: Upstream Interface Timing at 41.67MHz upstream serial line clock

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SETUP}	Sideband data setup time to sideband clock	-	20	-	ns
t_{HOLD}	Sideband data hold time to sideband clock	-	20	-	ns

Table 4-6: Upstream Interface Timing at 62.5 MHz upstream serial line clock

4.1.3 Configuration interface timing

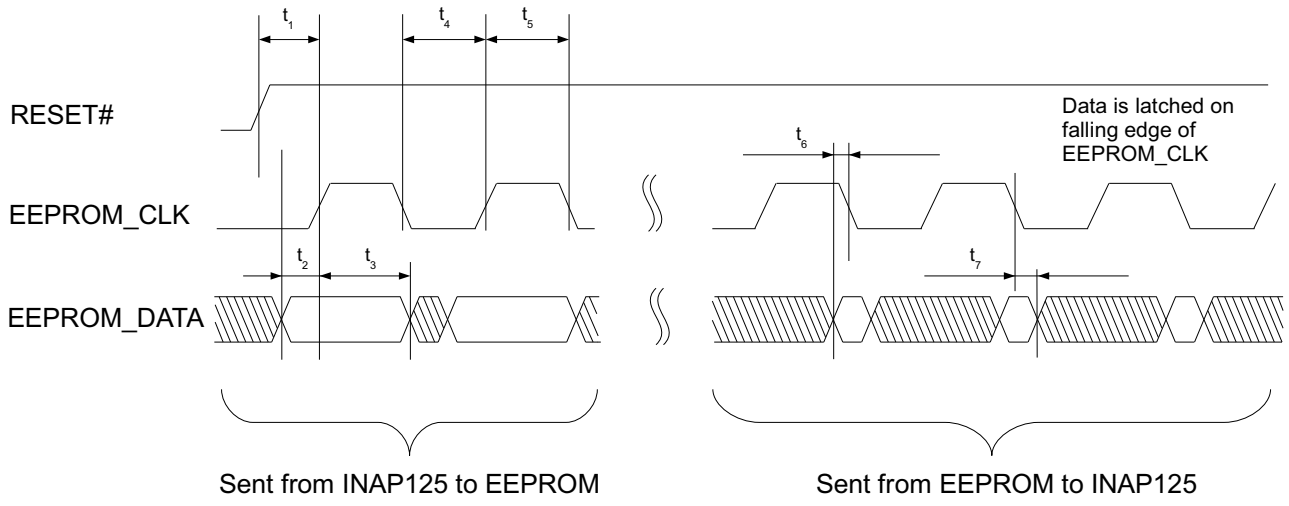


Figure 4-5: Configuration interface timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_1	RESET high to first EEPROM clk	$6xt_{OSC}$ [a]	650	-	ns
t_2	setup time EEPROM_DATA to EEPROM_CLK	-	400	-	ns
t_3	hold time EEPROM_DATA to EEPROM_CLK	-	1200	-	ns
t_4	EEPROM_CLK low time	-	800	-	ns
t_5	EEPROM_CLK high time	-	800	-	ns
t_6	setup time EEPROM_DATA to EEPROM_CLK	-	20	-	ns
t_7	hold time EEPROM_DATA to EEPROM_CLK	-	10	-	ns

Table 4-7: Configuration interface timing

a. t_{OSC} reflects one clock cycle as defined by the external reference clock, see section 5.2.4.

5.0 External circuits

5.1 External Termination Resistors

There are no external termination resistors required – for both Upstream and Downstream the dedicated 50 Ohm termination resistors are integrated in the circuit.

5.2 External Coupling Capacitors

5.2.1 Downstream Coupling Capacitors

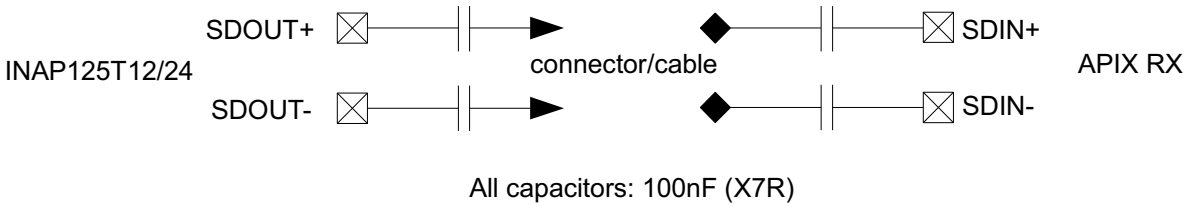


Figure 5-1: External coupling capacitors in downstream

5.2.2 Upstream Coupling Capacitors

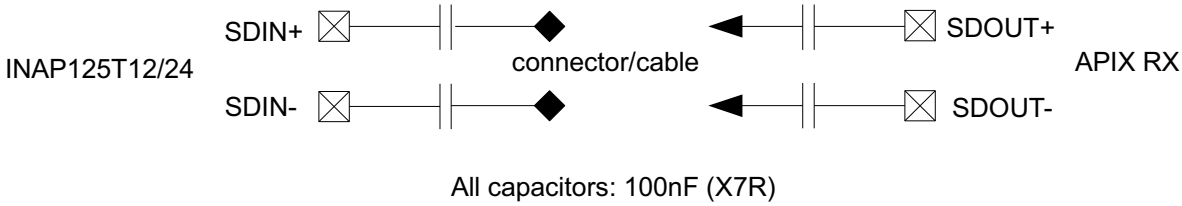


Figure 5-2: External coupling capacitors in upstream

5.2.3 External Loop Filter

The INAP125T12/24 PLL circuit for the core system requires an external loop filter which should be implemented as shown in Figure 5-3.

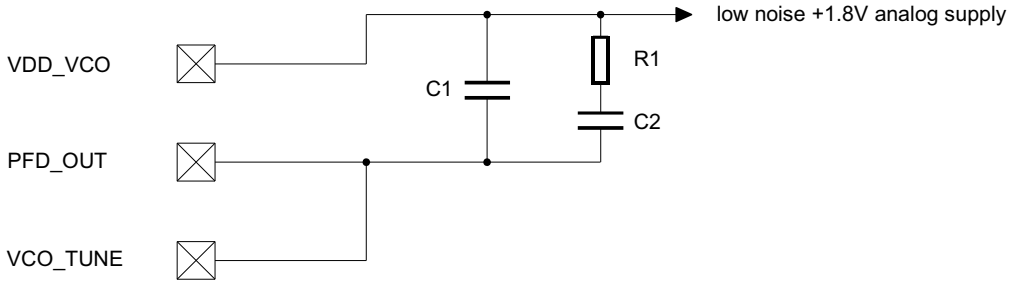


Figure 5-3: External loop filter circuit for the system clock VCO

Symbol	Description	Value Setting A	Value Setting B	Unit
C_1	Capacitor C_1	1.5	3.3	nF
C_2	Capacitor C_2	10	68	nF
R_1	Resistor R_1	220	6.5	kΩ

Table 5-1: Loop filter values for the system clock VCO

The external loop filter components allow to change the PLL characteristics within narrow limits. While value setting A (nominal) provides a high PLL bandwidth of 4.5kHz, value setting B sligthly decreases this bandwidth but increases immunity against undesired voltage drops / spikes.

5.2.4 External Reference Clock

The INAP125T12/24 core clock frequency is generated by an internal PLL controlled by an external 10 MHz crystal. Figure 5-4 shows a typical crystal design required for the oscillator circuit. The values for C1, C2 and R1 need to be selected to match the oscillation requirements of the crystal Q1. Please see Table 5-2 for the external crystal.

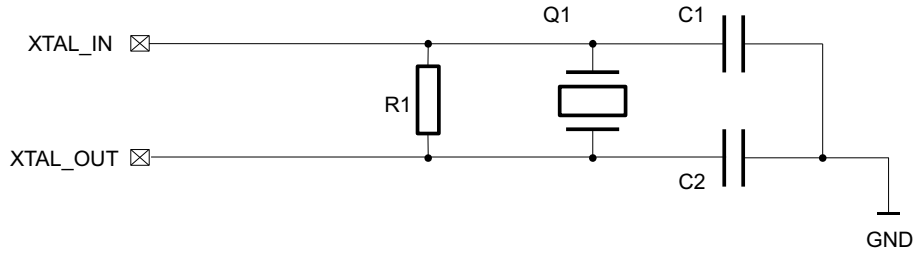


Figure 5-4: Crystal clock schematic example

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_{OSC}	-	10	-	MHz
Frequency Tolerance	F_{tol}	-100	-	+100	ppm
Equivalent Series Resistance	ESR	-	-	80	Ohm
Drive Level		see Table 5-3			

Table 5-2: Crystal requirements

For resonance at the correct frequency, the crystal needs to be loaded with its specified load capacitance C_L, which is the value of capacitance used in conjunction with the oscillation unit. The INAP125T12/24 oscillator provides some of the load with internal capacitance which is specified within the range of 10pF to 12.5pF. The remainder is generated by the external capacitors and tuning capacitors labeled C1 and C2.

The load capacitance C_L can be calculated from $C_L = C_{int}$ + C1//C2. E.g. selecting C1 and C2 with 15pF, C_L can be calculated to C_L = 12.5pF + 7.5pF = 20pF.

The crystal needs to be able to withstand the power dissipation, produced by the INAP125T12/24. The power dissipation depends on the ESR of the crystal and is reflected by the maximum drive level of the crystal. Table 5-3 illustrates the power dissipation of the INAP125T12/24 and therefore the minimum drive level capabilities of the crystal at different crystal ESR levels.

Crystal ESR	INAP125T12/24 Power dissipation / Minimum crystal drive level	Unit
30	77	µW
50	121	µW
80	179	µW

Table 5-3: Minimum Drive level vs. Crystal ESR

Alternatively a stable 10 MHz clock signal (3.3V CMOS TTL) can be directly connected to XTAL_IN with XTAL_OUT left open. Clock oscillator signal must start after ramping of all supply voltages is completed.

5.2.5 Pre-Emphasis and Nominal Current

For optimized signal integrity and lowest EMI in dependence of the quality and length of the STP cable used, the output nominal current and the pre-emphasis current of the INAP125T12/24 can be set individually by means of external resistors.

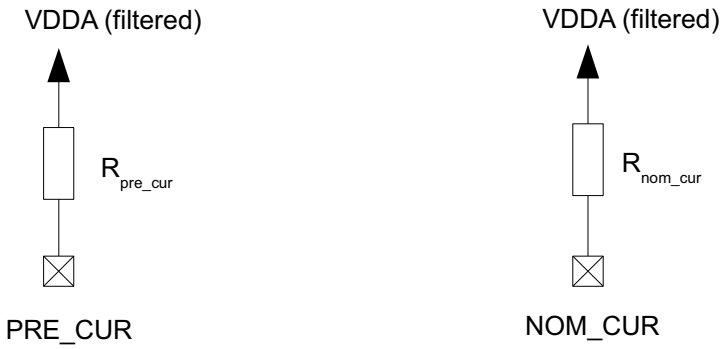
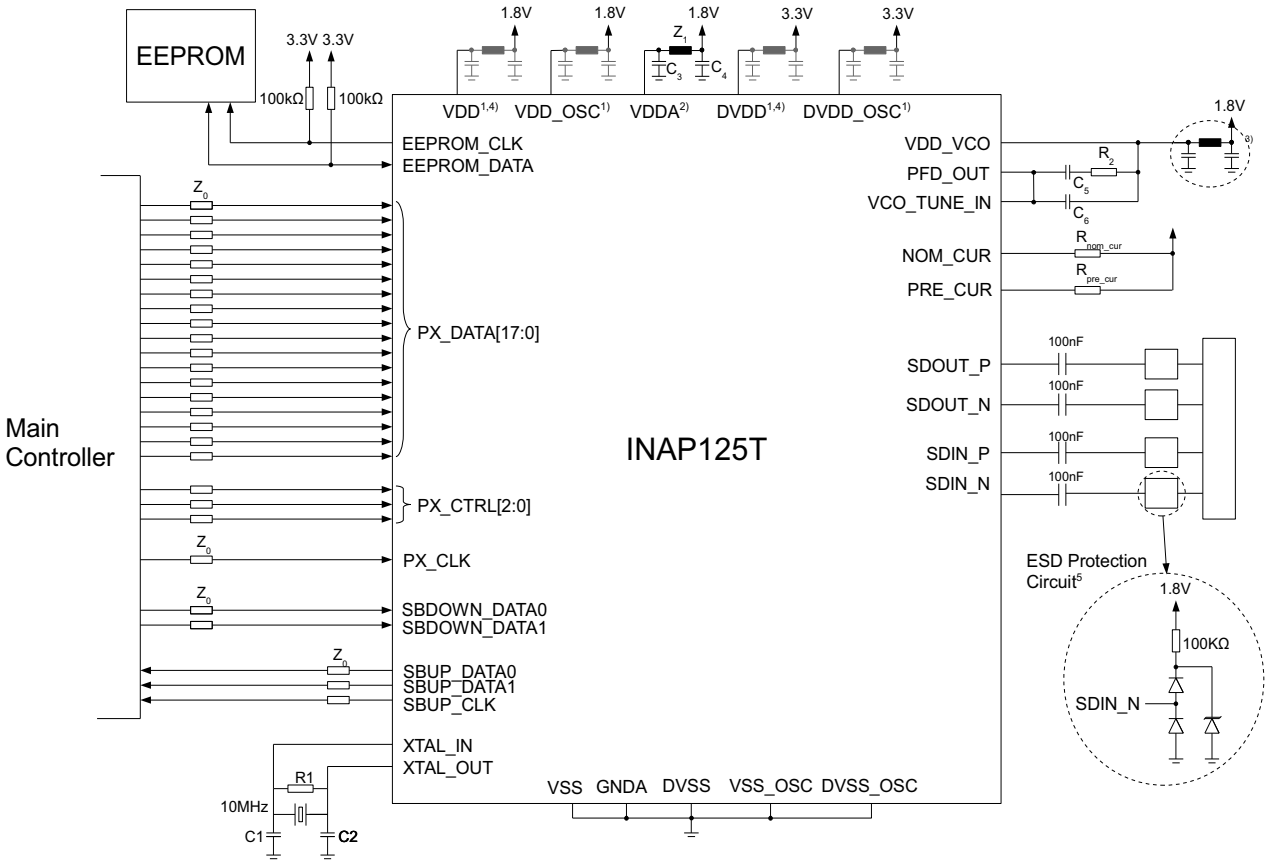


Figure 5-5: Pre-emphasis and Nominal current

Symbol	Pin	Description	Min.	Max.	Unit
R_{pre_cur}	PRE_CUR	resistor value (typical current of pre-emphasis)	500 (1mA)	10000 (0.05mA)	Ohm
R_{nom_cur}	NOM_CUR	resistor value (typical add-on output current)	500 (5mA)	10000 (0.5mA)	Ohm

Table 5-4: Recommended component values for nominal and pre-emphasis

6.0 Application Example



$Z_{0:}$ Trace impedance
R1,C1,C2: Please check crystal requirements for component values
Z1,C3,C4: Filter design must be designed to eliminate oscillation on high dynamic currents with VDDA meeting specification requirements
R2,C5,C6: Please check loopfilter requirements for component values

1) Filter not required for functional reasons, but might be considered for EMI performance
2) Filter not required for functional reasons, but strongly recommended for EMI performance
3) Filter recommended for performance reasons
4) Filter recommended on all input pins, if applicable
5) ESD protection design implementation example, please check available circuitry

Figure 6-1: Application example

7.0 Electrical Characteristics

7.1 Absolute Maximum ratings

The absolute maximum ratings define values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The functional operation of the device at these or any other conditions beyond the recommended operating ratings is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{DVDD}, V_{DVDD_OSC}	-0.5	5.0	V	
Input Voltage	V_{VDD}, V_{VDDA}, V_{VDD_OSC}	-0.5	3.0	V	
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	
Storage Temperature	T_{stg}	-55	+150	° C	
Max Soldering Temperature	T_{SLD} / T_{SLD}		260	° C	40 seconds maximum
ESD Protection IEC61000-4-2 Contact discharge [a] SDOUT+,SDOUT-,SDIN+,SDIN-		-8	+8	kV	R_D=330Ω, C_S=150pF
ESD Protection IEC61000-4-2 Air discharge [a] SDOUT+,SDOUT-,SDIN+,SDIN-		-12	+12	kV	R_D=330Ω, C_S=150pF
ESD Protection ISO10605 Contact discharge [a] SDOUT+,SDOUT-,SDIN+,SDIN-		-8	+8	kV	R_D=2kΩ, C_S=150pF
ESD Protection ISO10605 Air discharge [a] SDOUT+,SDOUT-,SDIN+,SDIN-		-20	+20	kV	R_D=2kΩ, C_S=150pF
ESD Protection HBM JEDEC JESD22/A114		-3	+3	kV	R_D=1.5kΩ, C_S=100pF
ESD Protection CDM EIA/JEDEC JESD22/C101		-1	+1	kV	

Table 7-1: Absolute maximum ratings

a. ESD Protection values measured without external protection circuitry. Higher protection grades possible with external circuitry as described in section 6.0.

7.2 Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Digital Core supply	V_{VDD}	1.71	1.8	1.89	V	
Analog supply	V_{VDDA}	1.71	1.8	1.89	V	
Oscillator supply	V_{VDD_OSC}	1.71	1.8	1.89	V	
Digital IO Supply	V_{DVDD}	2.97	3.3	3.63	V	
Oscillator supply	V_{DVDD_OSC}	2.97	3.3	3.63	V	
CML Current	I_{CML}	0.8	-	24	mA	Internal Current Source
Ambient Temperature	T_a	-40	-	+105	° C	

Figure 7-1: Recommended operating conditions

7.3 DC Characteristics

under recommended operating conditions. Unused inputs should be tied to ground.

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
CMOS Input High Voltage	V_{IH}	V_{DVDD} = 3.3 V	2.0	-	V_{DVDD}	V
CMOS Input Low Voltage	V_{IL}	V_{DVDD} = 3.3 V	0	-	0.8	V
CMOS Input High Current	I_{IH}	$V_{IN} = V_{DVDD}$	-10	-	10	µA
CMOS Input Low Current	I_{IL}	V_{IN} = 0 V	-15	-	-77	µA
CMOS Output High Voltage	V_{OH}	I_{OH} = -4 mA	2.4	-	-	V
CMOS Output Low Voltage	V_{OL}	I_{OL} = 4 mA	-	-	0.4	V
CMOS Output High Current	I_{OH}	V_{OH} = 0.9 x DVDD	-	-	4	mA
CMOS Output Low Current	I_{OL}	V_{OL} = 0.1 x DVDD	-	-	-4	mA
Power Dissipation Tx	P_{max_Tx}	max data transmis-sion rate	-	170	-	mW

Table 7-2: DC characteristics

7.3.1 Supply Current

Parameter	min.	typ.	max.	Units
I_{vdd/vdd_osc}	-	11	14	mA
I_{vdda/vdd_vco} [a]	-	82	95	mA
$I_{dvdd/dvdd\_osc}$	-	7	8	mA

Table 7-3: Supply Current

a. values at maximum serial drive current NOM_CUR, configurable as described in section 5.2.5

7.4 AC-Characteristics

Parameter	Min.	Typ.	Max.	Units
Input Capacitance, any pin	-	3	5	pF
Serial Transmission Gross Data Rate (Downstream)	500	-	1000	MBit/s
Serial Transmission Gross Data Rate (Upstream)	20.8	-	62.5	MBit/s
CMOS Output Rise / Fall Time (CL = 10 pF)	-	5	10	ns

Table 7-4: AC-Characteristics

7.5 Pixel Clock Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Pixel Clock Frequency	f_{PIX}	6	-	62	MHz	Maximum frequency depends on selected bit width

Table 7-5: Pixel Clock Range

8.0 Package Options / Ordering information

Device / Ordering Code	Description	Package	Minimum Order Quantity
INAP125T12	Tx w/10...12 bit Interface + 1 bit Sideband	QFN48	416 pcs/tray
INAP125T12-R2	Tx w/10...12 bit Interface + 1 bit Sideband	QFN48	2000 pcs/reel
INAP125T12-R4	Tx w/10...12 bit Interface + 1 bit Sideband	QFN48	4000 pcs/reel
INAP125T24	Tx w/10...24 bit Interface + 2 bit Sideband	QFN64	260 pcs/tray
INAP125T24-R2	Tx w/10...24 bit Interface + 2 bit Sideband	QFN64	2000 pcs/reel
INAP125T24-R4	Tx w/10...24 bit Interface + 2 bit Sideband	QFN64	4000 pcs/reel

Table 8-1: Package Options

8.1 RoHS compliance

The devices INAP125T12 and INAP125T24 are released as RoHS compliant.

9.0 Soldering information

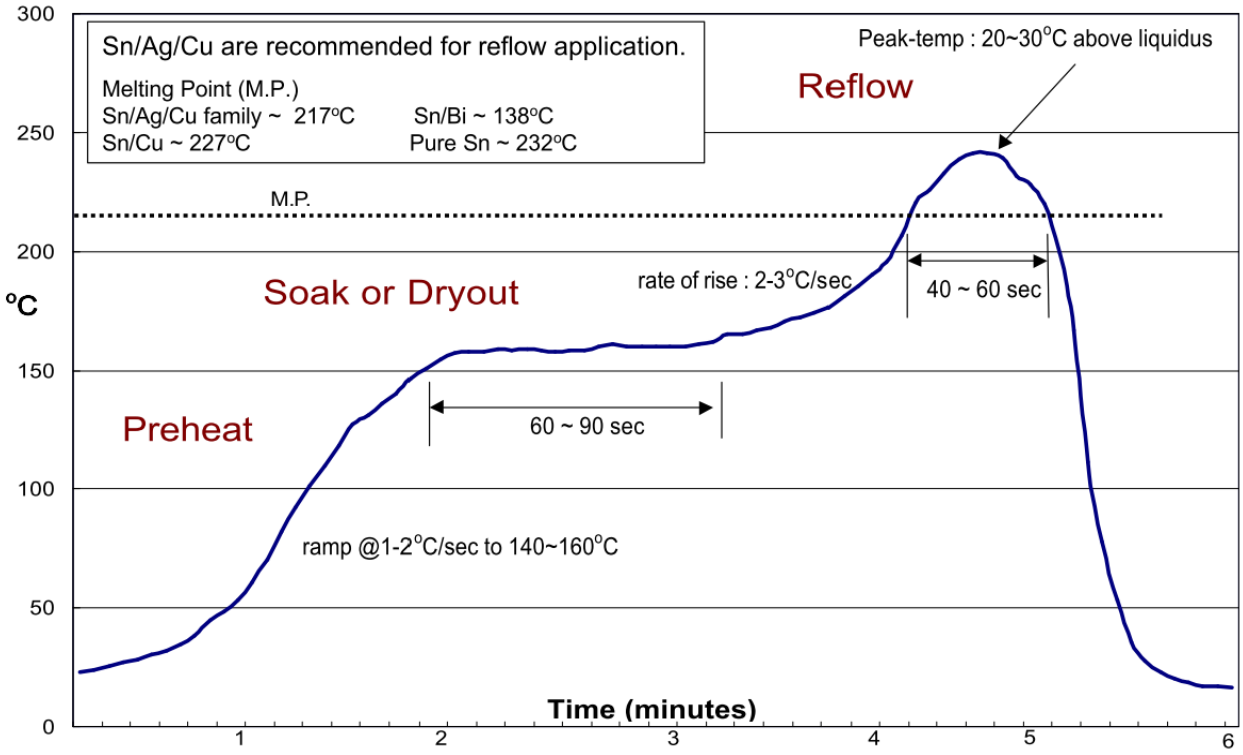


Figure 9-1: Reflow profile

10.0 Package information

10.1 Pinout diagrams

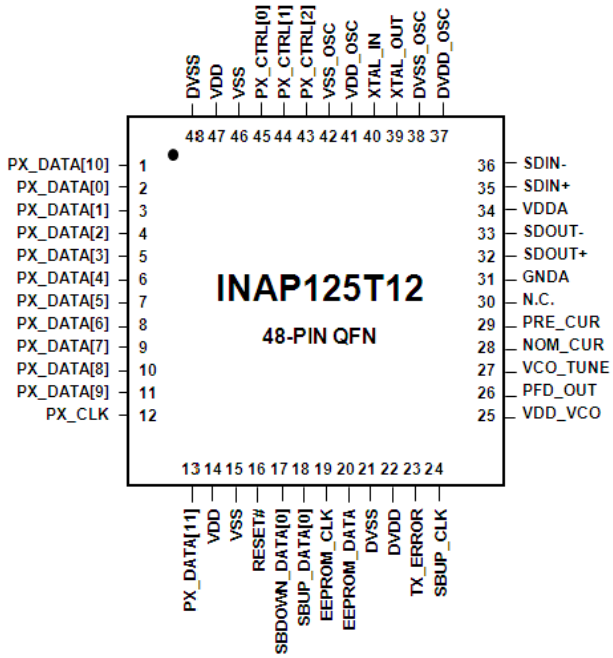


Figure 10-1: INAP125T12 pinout diagram

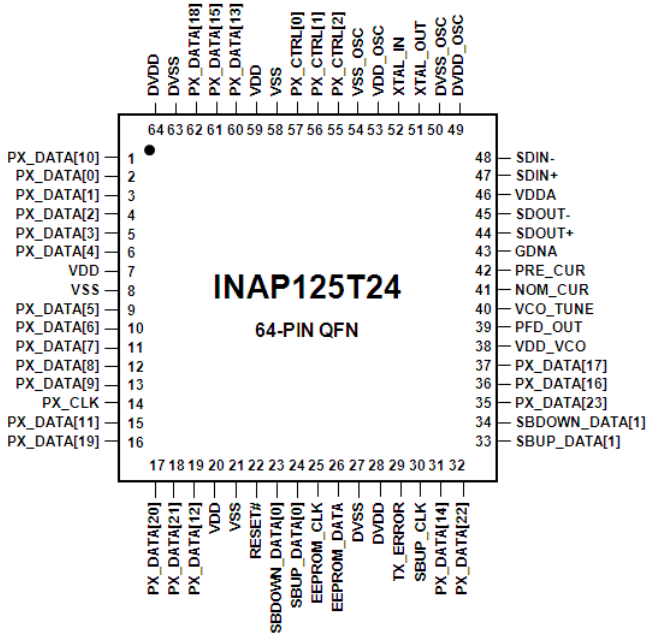


Figure 10-2: INAP125T24 pinout diagram

10.2 Package dimensions

all values in millimeter

10.2.1 48-pin QFN

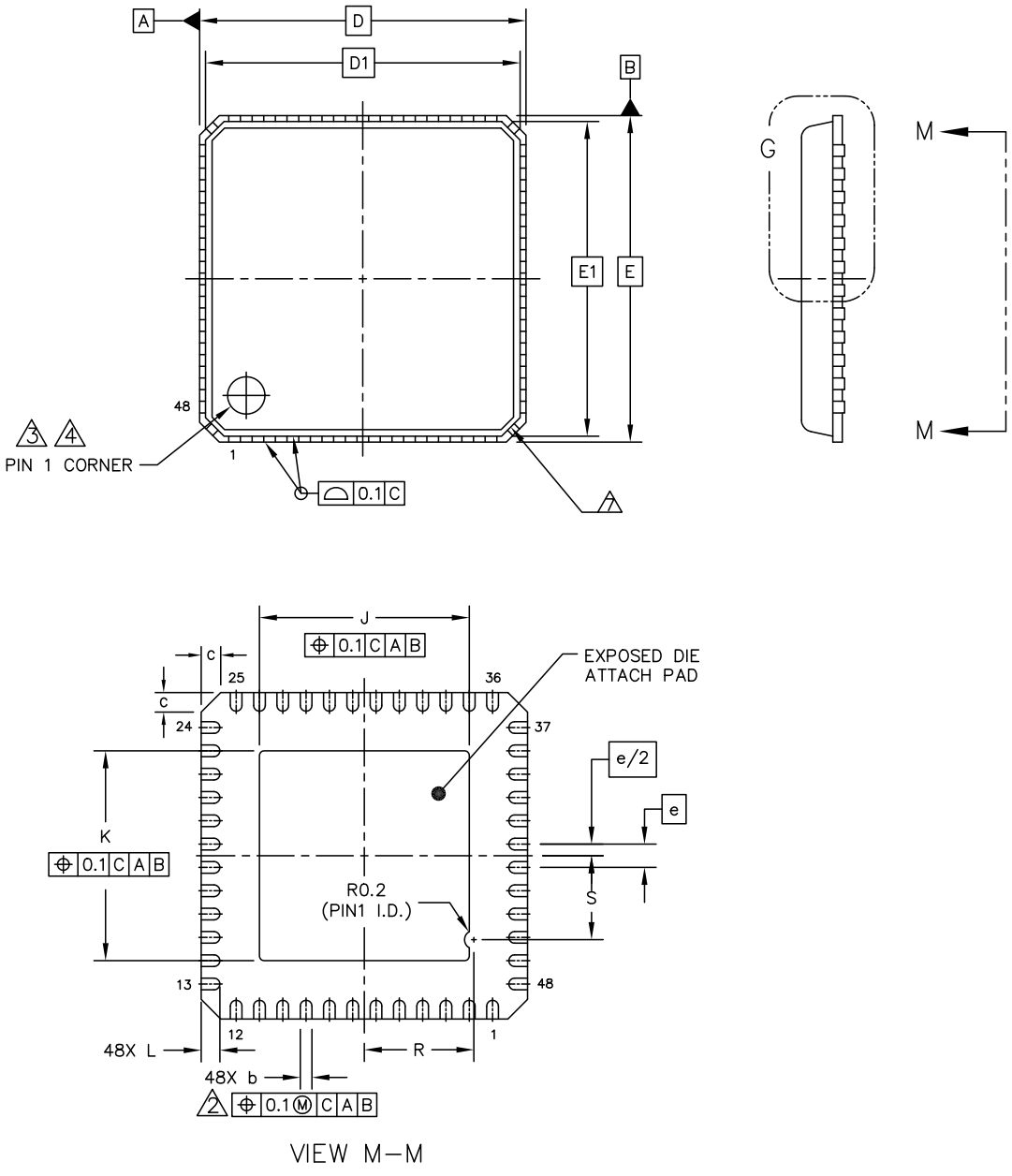
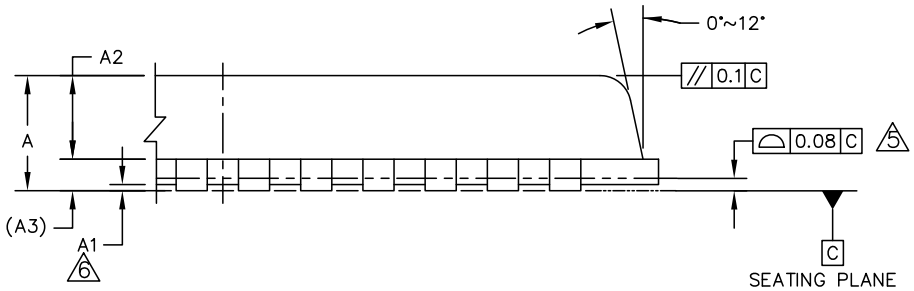


Figure 10-3: 48-pin QFN package dimensions



DETAIL G
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF.	
b	0.18	0.25	0.3
C	0.24	0.42	0.6
D		7 BSC	
D1		6.75 BSC	
E		7 BSC	
E1		6.75 BSC	
e		0.5 BSC	
J	4.4	4.5	4.6
K	4.4	4.5	4.6
L	0.3	0.4	0.5
R	2.25	2.35	2.45
S	1.7	1.8	1.9

NOTES

1. DIE THICKNESS ALLLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
6. APPLIED ONLY TO TERMINALS.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	---

Figure 10-4: 48-pin QFN package dimensions

10.2.2 64-pin QFN

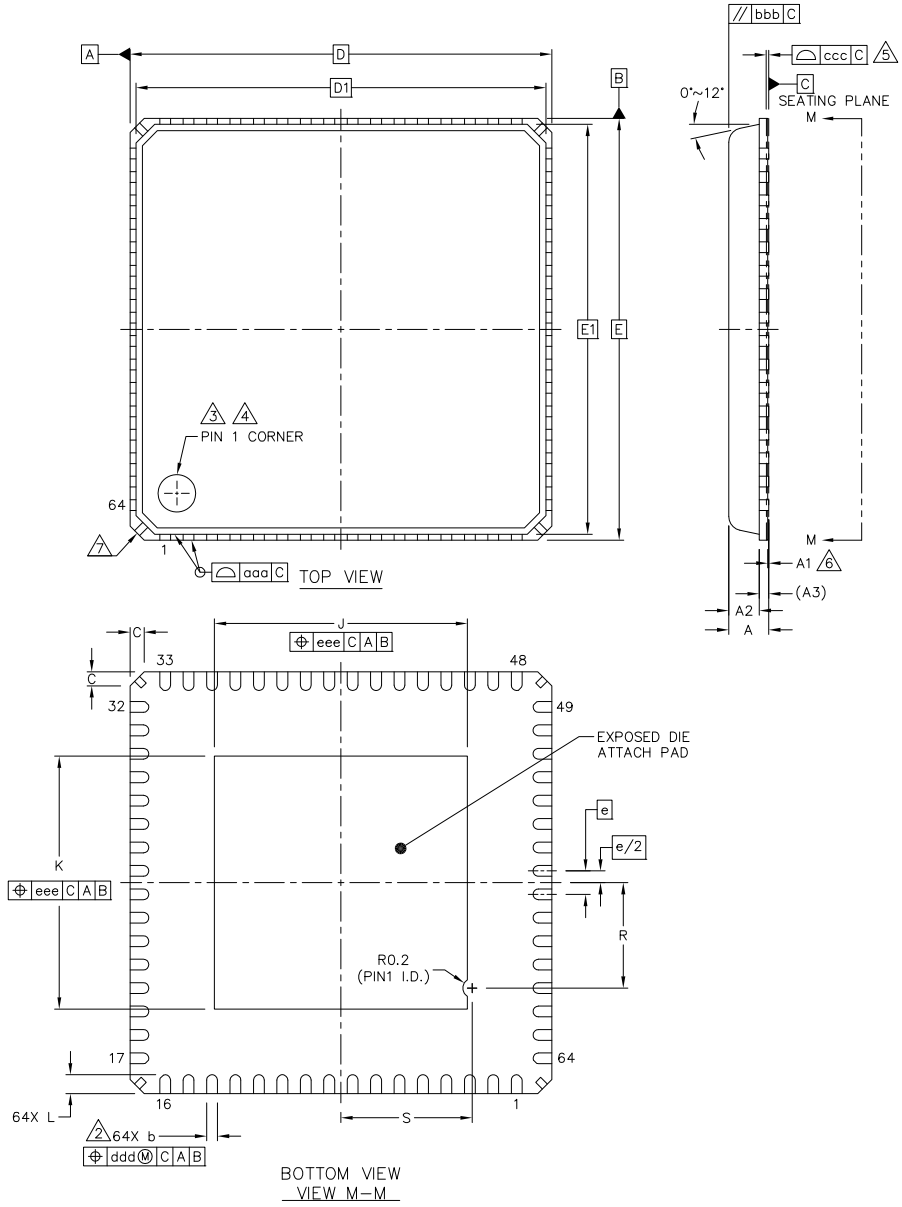


Figure 10-5: 64-pin QFN package dimensions

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	0.65	---	0.69
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.18	0.23	0.28
CHAMFER		C	0.24	---	0.6
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
MOLD CAP	X	D1		8.75 BSC	
	Y	E1		8.75 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.3	5.4	5.5
	Y	K	5.3	5.4	5.5
LEAD LENGTH		L	0.3	0.4	0.5
		R	2.15	2.25	2.35
		S	2.7	2.8	2.9
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.08	
COPLANARITY		ccc		0.05	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1. DIE THICKNESS ALLLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)

2. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.

3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.

4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

5. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.

6. APPLIED ONLY TO TERMINALS.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

Figure 10-6: 64-pin QFN package dimensions

11.0 Revision History

Revision	Date	Changes
1.0	February 2008	Released Datasheet
1.1	December 2008	• Separated Transmitter and Receiver Datasheet • Various updates on general description and formatting • Added separate block diagrams for T12 and T24 • Updated Section "Pixel Data Interface" at page 5 • Updated Section "Sideband Channel Downstream Interface" at page 6 • Updated Table 2-6, “INAP125T12 Pinout description, 48-pin QFN,” on page 7 • Updated Table 2-7, “INAP125T24 Pin description, 64-pin QFN,” on page 8 • Updated Section "Configuration vectors" at page 10 • Added Table 3-5, “TX Error pin configuration,” on page 12 • Updated Section "External Reference Clock" at page 20 • Added Section "Application Example" at page 23 • Updated Section "Electrical Characteristics" at page 24 • Added Section "Soldering information" at page 27
1.2	February 2009	• Updated V_{ESDCDM} to 1000V in Table 7-1, “Absolute maximum ratings,” on page 24
1.3	June 2009	• Added ESD protection values for ISO10605 and IEC61000-4-2 in Table 7-1, “Absolute maximum ratings,” on page 24
1.4	December 2011	• Updated Section "Application Example" at page 23 • Updated Section "Soldering information" at page 27
1.5	August 2012	• Updated Section "Reset" at page 14 • Updated Section "Power-Up Sequence and Timing" at page 15 • Updated Section "External Loop Filter" at page 20 • Updated Section "External Reference Clock" at page 20
1.6	November 2012	• Updated Section "64-pin QFN" at page 31

Table 11-1: Revision History

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