# WM5110

## Low Power Audio System with Wolfson myZone™ Ambient Noise Cancellation and Echo Cancellation

## DESCRIPTION

The WM5110[1] is a highly-integrated low-power audio system for smartphones, tablets and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub CODEC.

The WM5110 digital core combines a quad-core, 600MMAC DSP system with a variety of power-efficient fixed-function audio processing blocks. The programmable DSP cores support advanced audio features, including multi-mic wideband noise reduction and beamforming, high-performance acoustic echo cancellation (AEC), stereo ambient noise cancellation (ANC), speech enhancement, advanced media enhancement, and many more. The DSP cores are supported by a fully-flexible, all-digital mixing and routing engine with sample rate converters, for wide use-case flexibility.

A SLIMbus interface supports multi-channel audio paths and host control register access. Multiple sample rates are supported concurrently via the SLIMbus interface. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample rate detection enables seamless wideband/narrowband voice call handover.

Three stereo headphone drivers each provide stereo ground-referenced or mono BTL outputs. 110dB SNR, and noise levels as low as 2μV$_{RMS}$, offer hi-fi quality line or headphone output. High power, high-quality speaker output is provided by a stereo pair of 2W Class-D speaker amplifiers. Four channels of stereo PDM output are provided, for connection to external amplifiers.

The WM5110 supports up to eight microphone inputs, (up to six analogue, or up to eight PDM digital, or combinations of each). Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection.

The WM5110 power, clocking and output driver architectures are all designed to maximise battery life in voice, music and standby modes. The WM5110 is powered from a 1.8V external supply. A separate supply is required for the Class D speaker drivers (typically direct connection to 4.2V battery).

Two integrated FLLs provide support for a wide range of system clock frequencies. The WM5110 is configured using the I2C, SPI or SLIMbus interfaces. The fully-differential internal analogue architecture, minimal analogue signal paths and on-chip RF noise filters ensure a very high degree of noise immunity.

## FEATURES

- 600 MIPS, 600MMAC multi-core audio-signal processor
- Programmable wideband, multi-mic audio processing
    - myZone™ stereo adaptive ambient noise cancellation
    - Transmit-path noise reduction and echo cancellation
    - Microphone beam-forming
    - Wind noise, sidetone and other programmable filters
    - Dynamic Range Control, Fully parametric EQs
    - Multiband Compression, Virtual Surround Sound
- Multi-channel asynchronous sample rate conversion
- Integrated 6/8 channel 24-bit hi-fi audio hub CODEC
    - 6 ADCs, 100dB SNR microphone input (48kHz)
    - 8 DACs, 110dB SNR headphone playback (48kHz)
- Audio inputs
    - Up to 6 analogue or 8 digital microphone inputs
    - Single-ended or differential mic/line inputs
- Multi-purpose headphone / earpiece / line output drivers
    - 3 stereo output paths
    - 33mW into 32Ω load at 1% THD+N
    - 100mW into 16Ω BTL load at 5% THD+N
    - 3mW typical headphone playback power consumption
    - Pop suppression functions
    - 2μV$_{RMS}$ noise floor (A-weighted)
- 2 x 2W stereo Class D speaker output drivers
- Four-channel digital speaker (PDM) interface
- SLIMbus® audio and control interface
- 3 full digital audio interfaces
    - Standard sample rates from 4kHz up to 192kHz
    - Ultrasonic accessory function support
    - TDM support on all AIFs
    - 8 channel input and output on AIF1
- Flexible clocking, derived from MCLKn, BCLKn or SLIMbus
- 2 low-power FLLs support reference clocks down to 32kHz
- Advanced accessory detection functions
    - Low-power standby mode
    - 'Switchable ground' support for different headset types
- Configurable functions on 5 GPIO pins
- Integrated LDO regulators and charge pumps
- Small W-CSP package, 0.4mm pitch

## APPLICATIONS

- Smartphones and Multimedia handsets
- Tablets and Mobile Internet Devices (MID)
- General-purpose low-power audio CODEC hub

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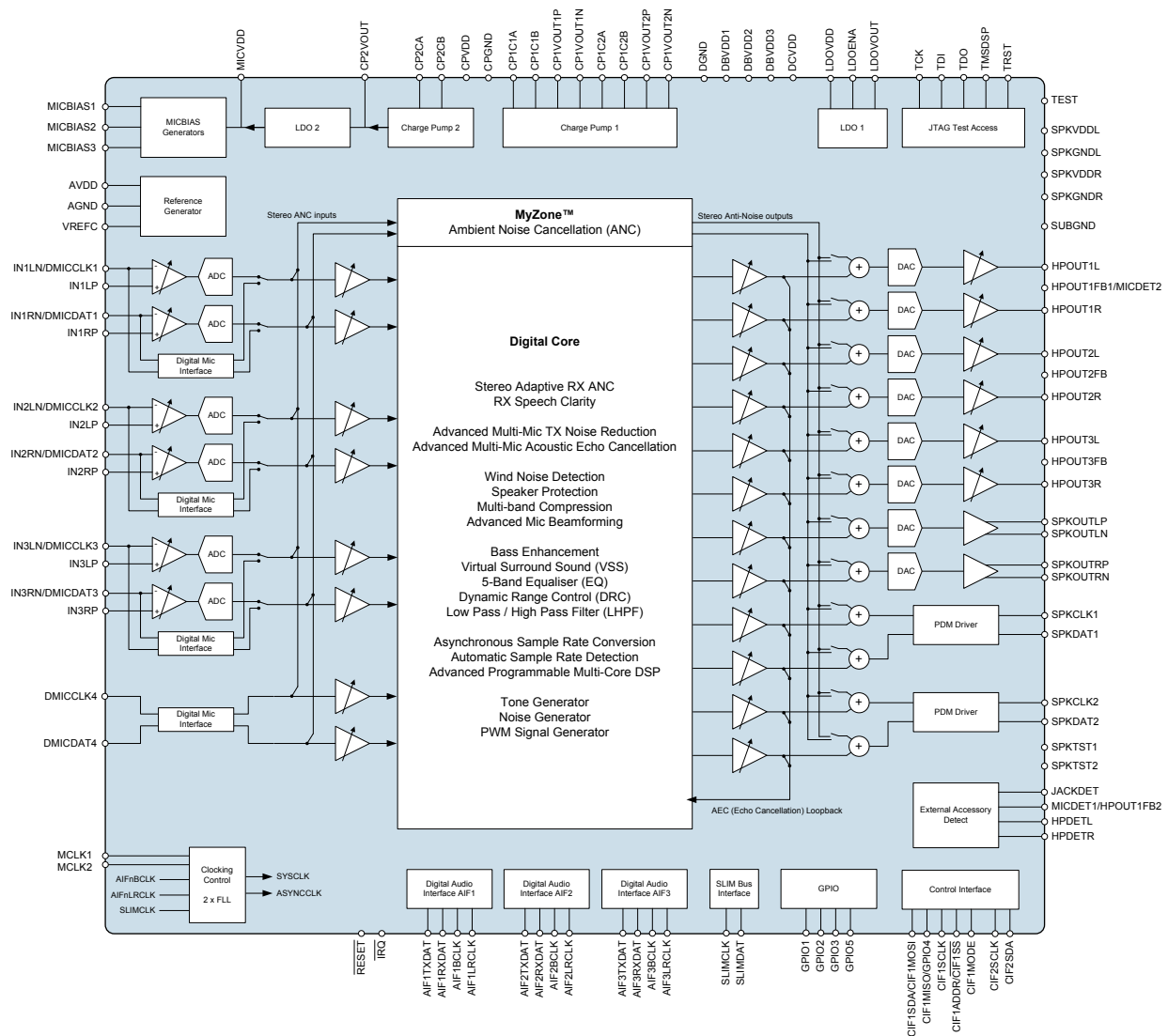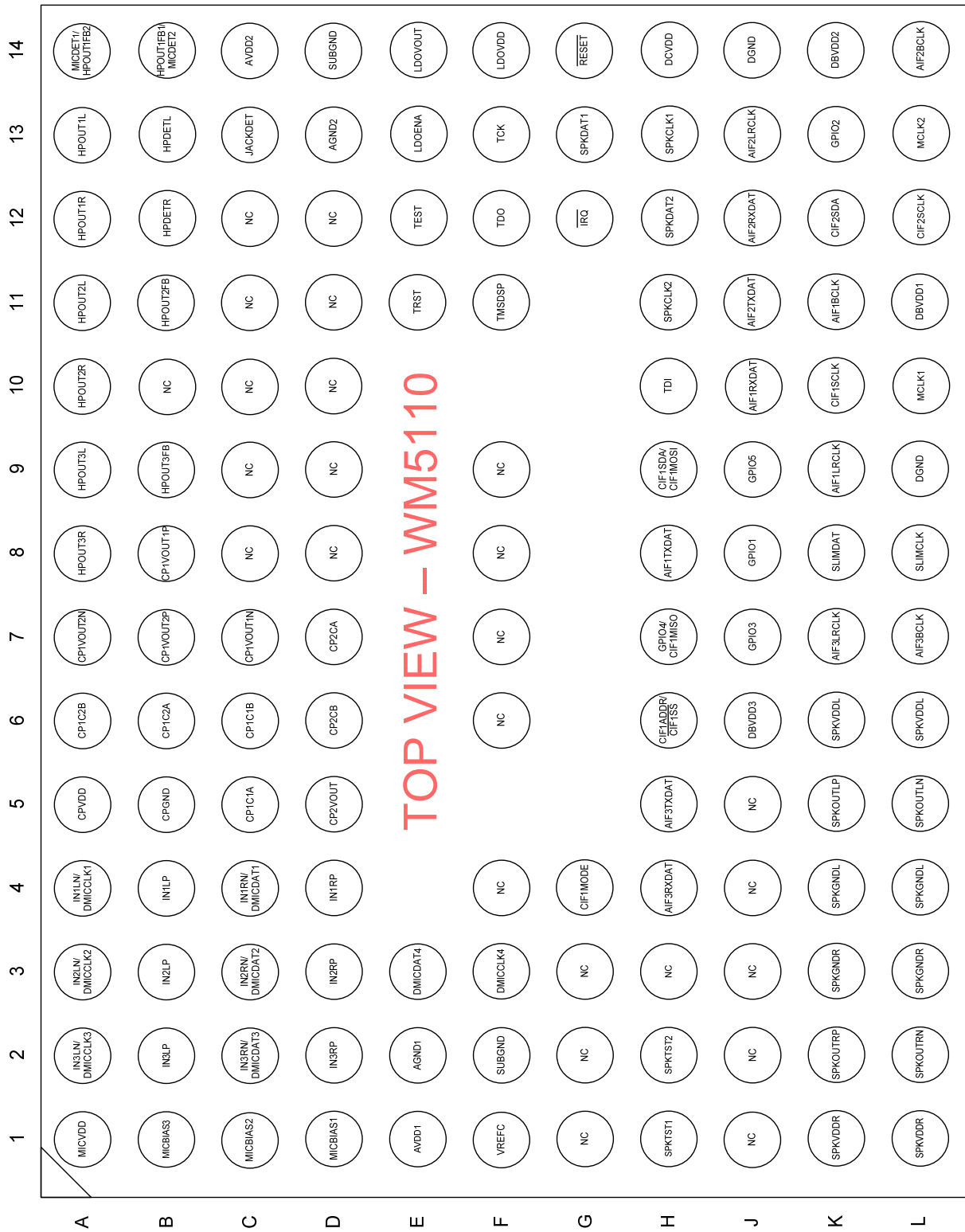[1] This product is protected by Patents US 7,622,984, US 7,626,445,US 7,765,019 and GB 2,432,765

## BLOCK DIAGRAM

## TABLE OF CONTENTS

## PIN CONFIGURATION

TOP VIEW – WM5110

| | A | B | C | D | E | F | G | H | J | K | L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | MICDET1/HPOUTFB2 | HPOUTFB1/MICDET2 | AVDD2 | SUBGND | LDOVOUT | LDOVDD | RESET | DCVDD | DGND | DBVDD2 | AIF2BCLK |
| 13 | HPOUT1L | HPDETL | JACKDET | AGND2 | LDOENA | TCK | SPKDAT1 | SPKCLK1 | AIF2LRCLK | GPIO2 | MCLK2 |
| 12 | HPOUT1R | HPDETR | NC | NC | TEST | TDO | IRQ | SPKDAT2 | AIF2RXDAT | CIF2SDA | CIF2SCLK |
| 11 | HPOUT2L | HPOUT2FB | NC | NC | TRST | TMSDSP | | SPKCLK2 | AIF2TXDAT | AIF1BCLK | DBVDD1 |
| 10 | HPOUT2R | NC | NC | NC | | | | TDI | AIF1RXDAT | CIF1SCLK | MCLK1 |
| 9 | HPOUT3L | HPOUT3FB | NC | NC | | NC | | CIF1SDA/CIF1MOSI | GPIO5 | AIF1LRCLK | DGND |
| 8 | HPOUT3R | CP1VOUT1P | NC | NC | | NC | | AIF1TXDAT | GPIO1 | SLIMDAT | SLIMCLK |
| 7 | CP1VOUT2N | CP1VOUT2P | CP1VOUT1N | CP2CA | | NC | | GPIO4/CIF1MISO | GPIO3 | AIF3LRCLK | AIF3BCLK |
| 6 | CP1C2B | CP1C2A | CP1C1B | CP2CB | | NC | | CIF1ADDR/CIF1SS | DBVDD3 | SPKVDDL | SPKVDDL |
| 5 | CPVDD | CPGND | CP1C1A | CP2VOUT | | | | AIF3TXDAT | NC | SPKOUTLP | SPKOUTLN |
| 4 | IN1LN/DMICCLK1 | IN1LP | IN1RN/DMICDAT1 | IN1RP | | NC | CIF1MODE | AIF3RXDAT | NC | SPKGNDL | SPKGNDL |
| 3 | IN2LN/DMICCLK2 | IN2LP | IN2RN/DMICDAT2 | IN2RP | DMICDAT4 | DMICCLK4 | NC | NC | NC | SPKGNDR | SPKGNDR |
| 2 | IN3LN/DMICCLK3 | IN3LP | IN3RN/DMICDAT3 | IN3RP | AGND1 | SUBGND | NC | SPKTST2 | NC | SPKOUTRP | SPKOUTRN |
| 1 | MICVDD | MICBIAS3 | MICBIAS2 | MICBIAS1 | AVDD1 | VREFC | NC | SPKTST1 | NC | SPKVDDR | SPKVDDR |

## ORDERING INFORMATION

| ORDER CODE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---|---|---|---|---|
| WM5110ECS/R | -40°C to +85°C | W-CSP (Pb-free, Tape and reel) | MSL1 | 260°C |

**Note:**

Reel quantity = 5000

## PIN DESCRIPTION

A description of each pin on the WM5110 is provided below.

Note that, where multiple pins share a common name, these pins should be tied together on the PCB.

| PIN NO | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| E2 | AGND1 | Supply | Analogue ground (Return path for AVDD1) |
| D13 | AGND2 | Supply | Analogue ground (Return path for AVDD2) |
| K11 | AIF1BCLK | Digital Input / Output | Audio interface 1 bit clock |
| J10 | AIF1RXDAT | Digital Input | Audio interface 1 RX digital audio data |
| K9 | AIF1LRCLK | Digital Input / Output | Audio interface 1 left / right clock |
| H8 | AIF1TXDAT | Digital Output | Audio interface 1 TX digital audio data |
| L14 | AIF2BCLK | Digital Input / Output | Audio interface 2 bit clock |
| J12 | AIF2RXDAT | Digital Input | Audio interface 2 RX digital audio data |
| J13 | AIF2LRCLK | Digital Input / Output | Audio interface 2 left / right clock |
| J11 | AIF2TXDAT | Digital Output | Audio interface 2 TX digital audio data |
| L7 | AIF3BCLK | Digital Input / Output | Audio interface 3 bit clock |
| H4 | AIF3RXDAT | Digital Input | Audio interface 3 RXdigital audio data |
| K7 | AIF3LRCLK | Digital Input / Output | Audio interface 3 left / right clock |
| H5 | AIF3TXDAT | Digital Output | Audio interface 3 TX digital audio data |
| E1 | AVDD1 | Supply | Analogue supply |
| C14 | AVDD2 | Supply | Analogue supply |
| H6 | CIF1ADDR/ $\overline{\text{CIF1SS}}$ | Digital Input | Control interface 1 (I2C) address select / Control interface 1 (SPI) Slave Select (SS) |
| H7 | CIF1MISO/ GPIO4 | Digital Input / Output | Control interface 1 Master In Slave Out data / General Purpose pin GPIO4 |
| G4 | CIF1MODE | Digital Input | Control interface 1 mode select input |
| K10 | CIF1SCLK | Digital Input | Control interface 1 clock input |
| H9 | CIF1SDA/ CIF1MOSI | Digital Input / Output | Control interface 1 (I2C) data input and output / Control interface 1 (SPI) Master Out Slave In data |
| L12 | CIF2SCLK | Digital Input | Control interface 2 clock input |
| K12 | CIF2SDA | Digital Input / Output | Control interface 2 data input and output / acknowledge output |
| C5 | CP1C1A | Analogue Output | Charge pump 1 fly-back capacitor 1 pin |
| C6 | CP1C1B | Analogue Output | Charge pump 1 fly-back capacitor 1 pin |
| B6 | CP1C2A | Analogue Output | Charge pump 1 fly-back capacitor 2 pin |
| A6 | CP1C2B | Analogue Output | Charge pump 1 fly-back capacitor 2 pin |
| C7 | CP1VOUT1N | Analogue Output | Charge pump 1 negative output 1 decoupling pin |
| B8 | CP1VOUT1P | Analogue Output | Charge pump 1 positive output 1 decoupling pin |
| A7 | CP1VOUT2N | Analogue Output | Charge pump 1 negative output 2 decoupling pin |
| B7 | CP1VOUT2P | Analogue Output | Charge pump 1 positive output 2 decoupling pin |
| D7 | CP2CA | Analogue Output | Charge pump 2 fly-back capacitor pin |
| D6 | CP2CB | Analogue Output | Charge pump 2 fly-back capacitor pin |
| D5 | CP2VOUT | Analogue Output | Charge pump 2 output decoupling pin / Supply for LDO2 |
| B5 | CPGND | Supply | Charge pump 1 & 2 ground (Return path for CPVDD) |

| PIN NO | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| A5 | CPVDD | Supply | Supply for Charge Pump 1 & 2 |
| L11 | DBVDD1 | Supply | Digital buffer (I/O) supply (core functions and Audio Interface 1) |
| K14 | DBVDD2 | Supply | Digital buffer (I/O) supply (for Audio Interface 2) |
| J6 | DBVDD3 | Supply | Digital buffer (I/O) supply (for Audio Interface 3) |
| H14 | DCVDD | Supply | Digital core supply |
| J14, L9 | DGND | Supply | Digital ground (Return path for DCVDD, DBVDD1, DBVDD2 and DBVDD3) |
| F3 | DMICCLK4 | Digital Output | Digital MIC clock output 4 |
| E3 | DMICDAT4 | Digital Input | Digital MIC data input 4 |
| J8 | GPIO1 | Digital Input / Output | General Purpose pin GPIO1 |
| K13 | GPIO2 | Digital Input / Output | General Purpose pin GPIO2 |
| J7 | GPIO3 | Digital Input / Output | General Purpose pin GPIO3 |
| J9 | GPIO5 | Digital Input / Output | General Purpose pin GPIO5 |
| B13 | HPDETL | Analogue Input | Headphone left (HPOUT1L) sense input |
| B12 | HPDETR | Analogue Input | Headphone right (HPOUT1R) sense input |
| B14 | HPOUT1FB1/ MICDET2 | Analogue Input | HPOUT1L and HPOUT1R ground feedback pin 1/ Microphone & accessory sense input 2 |
| A13 | HPOUT1L | Analogue Output | Left headphone 1 output |
| A12 | HPOUT1R | Analogue Output | Right headphone 1 output |
| B11 | HPOUT2FB | Analogue Input | HPOUT2L and HPOUT2R ground loop noise rejection feedback |
| A11 | HPOUT2L | Analogue Output | Left headphone 2 output |
| A10 | HPOUT2R | Analogue Output | Right headphone 2 output |
| B9 | HPOUT3FB | Analogue Input | HPOUT3L and HPOUT3R ground loop noise rejection feedback |
| A9 | HPOUT3L | Analogue Output | Left headphone 3 output |
| A8 | HPOUT3R | Analogue Output | Right headphone 3 output |
| A4 | IN1LN/ DMICCLK1 | Analogue Input / Digital Output | Left channel single-ended Mic/Line input / Left channel negative differential Mic/Line input / Digital MIC clock output 1 |
| B4 | IN1LP | Analogue Input | Left channel positive differential Mic/Line input |
| C4 | IN1RN/ DMICDAT1 | Analogue input / Digital Input | Right channel single-ended Mic/Line input / Right channel negative differential Mic/Line input / Digital MIC data input 1 |
| D4 | IN1RP | Analogue Input | Right channel positive differential Mic/Line input |
| A3 | IN2LN/ DMICCLK2 | Analogue Input / Digital Output | Left channel single-ended Mic/Line input / Left channel negative differential Mic/Line input / Digital MIC clock output 2 |
| B3 | IN2LP | Analogue Input | Left channel positive differential Mic/Line input |
| C3 | IN2RN/ DMICDAT2 | Analogue input / Digital Input | Right channel single-ended Mic/Line input / Right channel negative differential Mic/Line input / Digital MIC data input 2 |
| D3 | IN2RP | Analogue Input | Right channel positive differential Mic/Line input |
| A2 | IN3LN/ DMICCLK3 | Analogue Input / Digital Output | Left channel single-ended Mic/Line input / Left channel negative differential Mic/Line input / Digital MIC clock output 3 |
| B2 | IN3LP | Analogue Input | Left channel positive differential Mic/Line input |
| C2 | IN3RN/ DMICDAT3 | Analogue input / Digital Input | Right channel single-ended Mic/Line input / Right channel negative differential Mic/Line input / Digital MIC data input 3 |
| D2 | IN3RP | Analogue Input | Right channel positive differential Mic/Line input |
| G12 | $\overline{\text{IRQ}}$ | Digital Output | Interrupt Request (IRQ) output (default is active low) |
| C13 | JACKDET | Analogue Input | Jack detect input |
| E13 | LDOENA | Digital Input | Enable pin for LDO1 |
| F14 | LDOVDD | Supply | Supply for LDO1 |

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| PIN NO | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| E14 | LDOVOUT | Analogue Output | LDO1 output |
| L10 | MCLK1 | Digital Input | Master clock 1 |
| L13 | MCLK2 | Digital Input | Master clock 2 |
| D1 | MICBIAS1 | Analogue Output | Microphone bias 1 |
| C1 | MICBIAS2 | Analogue Output | Microphone bias 2 |
| B1 | MICBIAS3 | Analogue Output | Microphone bias 3 |
| A14 | MICDET1/<br>HPOUT1FB2 | Analogue Input | Microphone & accessory sense input 1/<br>HPOUT1L and HPOUT1R ground feedback pin 2 |
| A1 | MICVDD | Analogue Output | LDO2 output decoupling pin (generated internally by WM5110) |
| G14 | $\overline{\text{RESET}}$ | Digital Input | Digital Reset input (active low) |
| L8 | SLIMCLK | Digital Input / Output | SLIM Bus Clock input / output |
| K8 | SLIMDAT | Digital Input / Output | SLIM Bus Data input / output |
| H13 | SPKCLK1 | Digital Output | Digital speaker (PDM) 1 clock output |
| H11 | SPKCLK2 | Digital Output | Digital speaker (PDM) 2 clock output |
| G13 | SPKDAT1 | Digital Output | Digital speaker (PDM) 1 data output |
| H12 | SPKDAT2 | Digital Output | Digital speaker (PDM) 2 data output |
| K4, L4 | SPKGNDL | Supply | Left speaker driver ground (Return path for SPKVDDL) |
| K3, L3 | SPKGNDR | Supply | Right speaker driver ground (Return path for SPKVDDR) |
| L5 | SPKOUTLN | Analogue Output | Left speaker negative output |
| K5 | SPKOUTLP | Analogue Output | Left speaker positive output |
| L2 | SPKOUTRN | Analogue Output | Right speaker negative output |
| K2 | SPKOUTRP | Analogue Output | Right speaker positive output |
| H1 | SPKTST1 | Analogue Output | Test function (recommend no external connection) |
| H2 | SPKTST2 | Analogue Output | Test function (recommend no external connection) |
| K6, L6 | SPKVDDL | Supply | Left speaker driver supply |
| K1, L1 | SPKVDDR | Supply | Right speaker driver supply |
| D14, F2 | SUBGND | Supply | Substrate ground |
| F13 | TCK | Digital Input | JTAG clock input |
| H10 | TDI | Digital Input | JTAG data input |
| F12 | TDO | Digital Output | JTAG data output |
| E12 | TEST | Digital Input | Digital Core Test function input (connect to GND) |
| F11 | TMSDSP | Digital Input | JTAG mode select input |
| E11 | TRST | Digital Input | JTAG Test Access Port reset (active low, internal pull-down).<br>This input should be logic 0 for normal WM5110 operation. |
| F1 | VREFC | Analogue Output | Bandgap reference decoupling capacitor connection |
| B10, C8, C9, C10, C11, C12, D8, D9, D10, D11, D12, F4, F6, F7, F8, F9, G1, G2, G3, H3, J1, J2, J3, J4, J5 | NC | n/a | No Connection |

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## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|---|---|
| Supply voltages (DCVDD) | -0.3V | 1.6V |
| Supply voltages (DBVDD1) | -0.3V | 4.0V |
| Supply voltages (DBVDD2, DBVDD3, LDOVDD, AVDD, CPVDD, MICVDD) | -0.3V | 5.0V |
| Supply voltages (SPKVDDL, SPKVDDR) | -0.3V | TBD |
| Voltage range digital inputs (DBVDD1 domain) | SUBGND - 0.3V | DBVDD1 + 0.3V |
| Voltage range digital inputs (DBVDD2 domain) | SUBGND - 0.3V | DBVDD2 + 0.3V |
| Voltage range digital inputs (DBVDD3 domain) | SUBGND - 0.3V | DBVDD3 + 0.3V |
| Voltage range digital inputs (DMICDATn) | SUBGND - 0.3V | MICVDD + 0.3V |
| Voltage range analogue inputs (INnLP, INnLN, INnRP, INnRN) | SUBGND - 0.3V | MICVDD + 0.3V |
| Voltage range analogue inputs (HPOUT1FB1, HPOUT1FB2, HPOUTnFB) | SUBGND - 0.3V | SUBGND + 0.3V |
| Voltage range analogue inputs (MICDETn) | SUBGND - 0.3V | MICVDD + 0.3V |
| Voltage range analogue inputs (JACKDET, HPDETL, HPDETR) | CP1VOUTN - 0.3V | AVDD + 0.3V |
| Ground (AGND, DGND, CPGND, SPKGNDL, SPKGNDR) | SUBGND - 0.3V | SUBGND + 0.3V |
| Operating temperature range, $T_A$ | -40ºC | +85ºC |
| Operating junction temperature, $T_J$ | -40ºC | +125ºC |
| Storage temperature after soldering | -65ºC | +150ºC |

**Notes:**

1. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.

2. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.

3. The HPOUT1FBn and MICDETn functions share common pins. The Absolute Maximum Rating varies according to the applicable function of each pin.

4. CP1VOUTN is an internal supply, generated by the WM5110 Charge Pump (CP1). The CP1VOUTN voltage may vary between AGND and -CPVDD.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Digital supply range (Core) See note 3 | DCVDD | 1.14 | 1.2 | 1.26 | V |
| Digital supply range (I/O) See note 4 | DBVDD1 | 1.14 | | 1.95 | V |
| Digital supply range (I/O) | DBVDD2, DBVDD3 | 1.71 | | 2.62 | V |
| LDO supply range | LDOVDD | 1.71 | 1.8 | 1.89 | V |
| Charge Pump supply range | CPVDD | 1.71 | 1.8 | 1.89 | V |
| Speaker supply range | SPKVDDL, SPKVDDR | 2.4 | | 5.5 | V |
| Analogue supply range See notes 5, 6 | AVDD | 1.71 | 1.8 | 1.89 | V |
| Microphone Bias supply See note 7 | MICVDD | 2.375 | 2.5 | 3.6 | V |
| Ground | DGND, AGND, CPGND, SPKGNDL, SPKGNDR, SUBGND | | 0 | | V |
| Power supply rise time See notes 8, 9, 10 | All supplies | 1 | | | µs |
| Operating temperature range | $T_A$ | -40 | | 85 | °C |

**Notes:**

1. The grounds must always be within 0.3V of SUBGND.

2. There is no power sequencing requirement; the supplies may be enabled in any order.

3. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD supply.

4. If the SLIMbus interface is enabled, then DBVDD1 must be in the range 1.65V to 1.95V or in the range 1.14V to 1.30V.

5. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.

6. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.

7. An internal Charge Pump and LDO (powered by CPVDD) provide the Microphone Bias supply; the MICVDD pin should not be connected to an external supply.

8. DCVDD and MICVDD minimum rise times do not apply when these domains are powered using the internal LDOs.

9. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Wolfson strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.

10. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

## ELECTRICAL CHARACTERISTICS

**Test Conditions**

AVDD = 1.8V,
With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Analogue Input Signal Level (IN1L, IN1R, IN2L, IN2R, IN3L, IN3R)** | | | | | | |
| Full-scale input signal level | $V_{INFS}$ | Single-ended PGA input | 0.5 | | | $V_{RMS}$ |
| | | | -6 | | | dBV |
| | | Differential PGA input | 1 | | | $V_{RMS}$ |
| | | | 0 | | | dBV |

**Notes:**

1. The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
2. A $1.0V_{RMS}$ differential signal equates to $0.5V_{RMS}$/-6dBV per input.
3. A sinusoidal input signal is assumed.

**Test Conditions**

$T_A$ = +25$^{\circ}$C
With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Analogue Input Pin Characteristics (IN1L, IN1R, IN2L, IN2R, IN3L, IN3R)** | | | | | | |
| Input resistance | $R_{IN}$ | Single-ended PGA input, All PGA gain settings | 10 | 12 | | k$\Omega$ |
| | | Differential PGA input, All PGA gain settings | 20 | 24 | | |
| Input capacitance | $C_{IN}$ | | | | 5 | pF |

**Test Conditions**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Input Programmable Gain Amplifiers (PGAs)** | | | | | | |
| Minimum programmable gain | | | | 0 | | dB |
| Maximum programmable gain | | | | 31 | | dB |
| Programmable gain step size | | Guaranteed monotonic | | 1 | | dB |
| **Headphone Output Programmable Gain Amplifiers (PGAs)** | | | | | | |
| Minimum programmable gain | | | | -12 | | dB |
| Maximum programmable gain | | | | 0 | | dB |
| Programmable gain step size | | Guaranteed monotonic | | 1 | | dB |

**Test Conditions**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)** | | | | | | |
| Load resistance | | Normal operation | 15 | | | Ω |
| | | Device survival with load applied indefinitely | 1 | | | |
| Load capacitance | | Direct connection, Normal Mode | | | 500 | pF |
| | | Direct connection, Mono Mode (BTL) | | | 200 | |
| | | Connection via 16Ω series resistor | | | 2 | nF |
| DC offset at Load | | Single-ended mode | | 0.1 | 0.2 | mV |
| | | Differential (BTL) mode | | 0.2 | 0.5 | |
| **Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)** | | | | | | |
| Load resistance | | Stereo Mode | 4 | | | Ω |
| | | Mono Mode | 3 | | | |
| Load capacitance | | | | | 200 | pF |
| DC offset at Load | | | | | 5 | mV |
| SPKVDD leakage current | | | | | 1 | µA |

**Test Conditions**

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V, SPKVDDL = SPKVDDR = 4.2V,
$T_A$ = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Analogue Input Paths (INnL, INnR) to ADC (Differential Input Mode, INn_MODE = 01)** | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | 48kHz sample rate | 94 | 100 | | dB |
| | | 16kHz sample rate, (wideband voice) | 100 | 106 | | |
| Total Harmonic Distortion | THD | -1dBV input | | -91 | -85 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | -1dBV input | | -90 | -84 | dB |
| Channel separation (Left/Right) | | | | 100 | | dB |
| Input-referred noise floor | | A-weighted, PGA gain = +20dB | | 3.2 | | µV$_{RMS}$ |
| Common mode rejection ratio | CMRR | PGA gain = +30dB | 54 | 60 | | dB |
| | | PGA gain = 0dB | 64 | 70 | | |
| PSRR (AVDD) | PSRR | 100mV (peak-peak) 217Hz, PGA gain = 0dB | TBD | TBD | | dB |
| | | 100mV (peak-peak) 217Hz, PGA gain = +20dB | TBD | TBD | | |
| | | 100mV (peak-peak) 1kHz, PGA gain = +20dB | TBD | TBD | | |
| | | 100mV (peak-peak) 10kHz, PGA gain = +20dB | TBD | TBD | | |
| **Analogue Input Paths (INnL, INnR) to ADC (Single-Ended Input Mode, INn_MODE = 00)** | | | | | | |
| PGA Gain = +6dB unless otherwise stated. | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | 48kHz sample rate | | 100 | | dB |
| | | 16kHz sample rate, (wideband voice) | | 106 | | |
| Total Harmonic Distortion | THD | -7dBV input | | -91 | | dB |
| Total Harmonic Distortion Plus Noise | THD+N | -7dBV input | | -90 | | dB |
| Channel separation (Left/Right) | | | | 100 | | dB |
| Input-referred noise floor | | A-weighted, PGA gain = +20dB | | 3.2 | | µV$_{RMS}$ |
| PSRR (AVDD) | PSRR | 100mV (peak-peak) 217Hz | | TBD | | dB |
| | | 100mV (peak-peak) 10kHz | | TBD | | |

**Test Conditions**

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V, SPKVDDL = SPKVDDR = 4.2V,
$T_A$ = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DAC to Line Output (HPOUTnL, HPOUTnR; Load = 10kΩ, 50pF)** | | | | | | |
| Full-scale output signal level | $V_{OUT}$ | 0dBFS input | 1<br>0 | | | Vrms<br>dBV |
| Signal to Noise Ratio (A-weighted) | SNR | High performance mode (OUTn_LP_MODE=0) | 104 | 110 | | dB |
| | | Low power mode (OUTn_LP_MODE=1) | 101 | 107 | | |
| Total Harmonic Distortion | THD | 0dBFS input | | -91 | -85 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | 0dBFS input | | -90 | -84 | dB |
| Channel separation (Left/Right) | | | | 95 | | dB |
| Output noise floor (A-weighted) | | High performance mode (OUTn_LP_MODE=0) | | 3.2 | | $\mu V_{RMS}$ |
| | | Low power mode (OUTn_LP_MODE=1) | | 4.5 | | |
| PSRR (all supplies) | PSRR | 100mV (peak-peak) 217Hz | TBD | TBD | | dB |
| | | 100mV (peak-peak) 10kHz | TBD | TBD | | |
| **DAC to Headphone Output (HPOUTnL, HPOUTnR; $R_L$ = 32Ω)** | | | | | | |
| Maximum output power | $P_O$ | 0.1% THD | | 30 | | mW |
| Signal to Noise Ratio (A-weighted) | SNR | High performance mode (OUTn_LP_MODE=0) | 104 | 110 | | dB |
| | | Low power mode (OUTn_LP_MODE=1) | 97 | 103 | | |
| Total Harmonic Distortion | THD | $P_O$ = 20mW | | -86 | -80 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 20mW | | -85 | -79 | dB |
| Total Harmonic Distortion | THD | $P_O$ = 5mW | | -91 | -85 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 5mW | | -90 | -84 | dB |
| Channel separation (Left/Right) | | | | 95 | | dB |
| Output noise floor | | A-weighted, PGA gain = -12dB | | 1.8 | | $\mu V_{RMS}$ |
| PSRR (all supplies) | PSRR | 100mV (peak-peak) 217Hz | TBD | TBD | | dB |
| | | 100mV (peak-peak) 10kHz | TBD | TBD | | |
| **DAC to Headphone Output (HPOUTnL, HPOUTnR; $R_L$ = 16Ω)** | | | | | | |
| Maximum output power | $P_O$ | 0.1% THD | | 33 | | mW |
| Signal to Noise Ratio (A-weighted) | SNR | High performance mode (OUTn_LP_MODE=0) | 104 | 110 | | dB |
| | | Low power mode (OUTn_LP_MODE=1) | 97 | 103 | | |
| Total Harmonic Distortion | THD | $P_O$ = 20mW | | -86 | -82 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 20mW | | -85 | -79 | dB |
| Total Harmonic Distortion | THD | $P_O$ = 5mW | | -91 | -85 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 5mW | | -90 | -84 | dB |
| Channel separation (Left/Right) | | | | 95 | | dB |
| Output noise floor | | A-weighted, PGA gain = -12dB | | 1.8 | | $\mu V_{RMS}$ |

**Test Conditions**

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V, SPKVDDL = SPKVDDR = 4.2V,
$T_A$ = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| PSRR (all supplies) | PSRR | 100mV (peak-peak) 217Hz | TBD | TBD | | dB |
| | | 100mV (peak-peak) 10kHz | TBD | TBD | | |
| **DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, $R_L$ = 32Ω BTL)** | | | | | | |
| Maximum output power | $P_O$ | 0.1% THD | | 60 | | mW |
| | | 5% THD | | 100 | | |
| Signal to Noise Ratio | SNR | A-weighted | 104 | 110 | | dB |
| Total Harmonic Distortion | THD | $P_O$ = 75mW | | -76 | -70 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 75mW | | -75 | -69 | dB |
| Total Harmonic Distortion | THD | $P_O$ = 5mW | | -86 | -80 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 5mW | | -85 | -79 | dB |
| Output noise floor | | A-weighted, PGA gain = -12dB | | | TBD | µV$_{RMS}$ |
| PSRR (AVDD, CPVDD) | PSRR | 100mV (peak-peak) 217Hz | TBD | TBD | | dB |
| | | 100mV (peak-peak) 10kHz | TBD | TBD | | |
| **DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, $R_L$ = 16Ω BTL)** | | | | | | |
| Maximum output power | $P_O$ | 0.1% THD | | 60 | | mW |
| | | 10% THD | | 115 | | |
| Signal to Noise Ratio | SNR | A-weighted | 104 | 110 | | dB |
| Total Harmonic Distortion | THD | $P_O$ = 75mW | | -76 | -71 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 75mW | | -75 | -69 | dB |
| Total Harmonic Distortion | THD | $P_O$ = 5mW | | -86 | -80 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 5mW | | -85 | -79 | dB |
| Output noise floor | | A-weighted PGA gain = -12dB | | | TBD | µV$_{RMS}$ |
| PSRR (all supplies) | PSRR | 100mV (peak-peak) 217Hz | TBD | TBD | | dB |
| | | 100mV (peak-peak) 10kHz | TBD | TBD | | |

**Test Conditions**

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V, SPKVDDL = SPKVDDR = 4.2V,
$T_A$ = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 8Ω, 22µH, BTL)** | | | | | | |
| Maximum output power | $P_O$ | SPKVDD = 5.0V, 1% THD | | 1.2 | | W |
| | | SPKVDD = 4.2V, 1% THD | | 1.0 | | |
| | | SPKVDD = 3.6V, 1% THD | | 0.7 | | |
| Signal to Noise Ratio | SNR | A-weighted | 89 | 95 | | dB |
| Total Harmonic Distortion | THD | $P_O$ = 1.0W | | -70 | -64 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 1.0W | | -68 | -62 | dB |
| Total Harmonic Distortion | THD | $P_O$ = 0.5W | | -65 | -59 | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 0.5W | | -63 | -57 | dB |
| Channel separation (Left/Right) | | | | 80 | | dB |
| Output noise floor | | A-weighted | | | TBD | µV$_{RMS}$ |
| PSRR (all supplies) | PSRR | 100mV (peak-peak) 217Hz | 65 | 70 | | dB |
| | | 100mV (peak-peak) 10kHz | 60 | 65 | | |
| **DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 4Ω, 15µH, BTL)** | | | | | | |
| Maximum output power | $P_O$ | SPKVDD = 5.0V, 1% THD | | 2 | | W |
| | | SPKVDD = 4.2V, 1% THD | | 1.8 | | |
| | | SPKVDD = 3.6V, 1% THD | | TBD | | |
| Signal to Noise Ratio | SNR | A-weighted | | 95 | | dB |
| Total Harmonic Distortion | THD | $P_O$ = 1.0W | | TBD | | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 1.0W | | TBD | | dB |
| Total Harmonic Distortion | THD | $P_O$ = 0.5W | | TBD | | dB |
| Total Harmonic Distortion Plus Noise | THD+N | $P_O$ = 0.5W | | TBD | | dB |
| Channel separation (Left/Right) | | | | 80 | | dB |
| Output noise floor | | A-weighted | | TBD | | µV$_{RMS}$ |
| PSRR (all supplies) | PSRR | 100mV (peak-peak) 217Hz | | TBD | | dB |
| | | 100mV (peak-peak) 10kHz | | TBD | | |
| **DAC to Speaker Output (SPKOUTxP+SPKOUTxN, Mono Mode, Load = 4Ω, 15µH, BTL)** | | | | | | |
| Maximum output power | $P_O$ | SPKVDD = 5.0V, 1% THD | | 2.5 | | W |

**Test Conditions**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Digital Input / Output (except DMICDATn and DMICCLKn)** | | | | | | |
| **Digital I/O is referenced to DBVDD1, DBVDD2 or DBVDD3.** | | | | | | |
| **See "Recommended Operating Conditions" for the valid operating voltage range of each DBVDDn domain.** | | | | | | |
| Input HIGH Level | $V_{IH}$ | $V_{DBVDDn}$ = 1.2V ±10% | $0.65 \times V_{DBVDDn}$ | | | V |
| | | $V_{DBVDDn}$ = 1.8V ±10% | $0.65 \times V_{DBVDDn}$ | | | |
| | | $V_{DBVDDn}$ = 2.5V ±10% | $0.7 \times V_{DBVDDn}$ | | | |
| Input LOW Level | $V_{IL}$ | $V_{DBVDDn}$ = 1.2V ±10% | | | $0.35 \times V_{DBVDDn}$ | V |
| | | $V_{DBVDDn}$ = 1.8V ±10% | | | $0.35 \times V_{DBVDDn}$ | |
| | | $V_{DBVDDn}$ = 2.5V ±10% | | | $0.3 \times V_{DBVDDn}$ | |
| Note that digital input pins should not be left unconnected or floating. | | | | | | |
| Output HIGH Level | $V_{OH}$ | $I_{OH}$ = 1mA | $0.9 \times V_{DBVDDn}$ | | | V |
| Output LOW Level | $V_{OL}$ | $I_{OL}$ = -1mA | | | $0.1 \times V_{DBVDDn}$ | V |
| Input capacitance | | | | 10 | | pF |
| Input leakage | | | -1 | | 1 | µA |
| Pull-up / pull-down resistance (where applicable) | | | 28 | 36 | 45 | kΩ |
| **Digital Microphone Input / Output (DMICDATn and DMICCLKn)** | | | | | | |
| **DMICDATn and DMICCLKn are each referenced to a selectable supply, $V_{SUP}$, according to the INn_DMIC_SUP registers** | | | | | | |
| DMICDATn input HIGH Level | $V_{IH}$ | | $0.65 \times V_{SUP}$ | | | V |
| DMICDATn input LOW Level | $V_{IL}$ | | | | $0.35 \times V_{SUP}$ | V |
| DMICCLKn output HIGH Level | $V_{OH}$ | $I_{OH}$ = 1mA | $0.8 \times V_{SUP}$ | | | V |
| DMICCLKn output LOW Level | $V_{OL}$ | $I_{OL}$ = -1mA | | | $0.2 \times V_{SUP}$ | V |
| Input capacitance | | | | 25 | | pF |
| Input leakage | | | -1 | | 1 | µA |
| **SLIMbus Digital Input / Output (SLIMCLK and SLIMDAT)** | | | | | | |
| **1.2V I/O Signalling (ie. 1.10V ≤ DBVDD1 ≤1.3V)** | | | | | | |
| Input LOW Level | $V_{IL}$ | | | | TBD | V |
| Input HIGH Level | $V_{IH}$ | | TBD | | | V |
| Output LOW Level | $V_{OL}$ | $I_{OL}$ = -1mA | | | TBD | V |
| Output HIGH Level | $V_{OH}$ | $I_{OH}$ = 1mA | TBD | | | V |
| Pin capacitance | | | | | TBD | pF |
| **SLIMbus Digital Input / Output (SLIMCLK and SLIMDAT)** | | | | | | |
| **1.8V I/O Signalling (ie. 1.65V ≤ DBVDD1 ≤1.95V)** | | | | | | |
| Input LOW Level | $V_{IL}$ | | | | TBD | V |
| Input HIGH Level | $V_{IH}$ | | TBD | | | V |
| Output LOW Level | $V_{OL}$ | $I_{OL}$ = -1mA | | | TBD | V |
| Output HIGH Level | $V_{OH}$ | $I_{OH}$ = 1mA | TBD | | | V |
| Pin capacitance | | | | | TBD | pF |
| **General Purpose Input / Output (GPIOn)** | | | | | | |
| Clock output frequency | | GPIO pin configured as OPCLK or FLL output | | | 40 | MHz |

**Test Conditions**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ADC Decimation Filters** | | | | | | |
| Passband | | +/- 0.05dB | 0 | | 0.454 fs | |
| | | -6dB | | 0.5 fs | | |
| Passband ripple | | | | | +/- 0.05 | dB |
| Stopband | | | 0.546 fs | | | |
| Stopband attenuation | | f > 0.546 fs | -85 | | | dB |
| Group delay | | | | | 2 | ms |
| **DAC Interpolation Filters** | | | | | | |
| Passband | | +/- 0.05dB | 0 | | 0.454 fs | |
| | | -6dB | | 0.5 fs | | |
| Passband ripple | | | | | +/- 0.05 | dB |
| Stopband | | | 0.546 fs | | | |
| Stopband attenuation | | f > 0.546 fs | -85 | | | dB |
| Group delay | | | | | 1.5 | ms |

**Test Conditions**

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,

DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V, SPKVDDL = SPKVDDR = 4.2V,

$T_A$ = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Microphone Bias (MICBIAS1, MICBIAS2, MICBIAS3)** | | | | | | |
| Note - No capacitor on MICBIASn | | | | | | |
| Note - In regulator mode, it is required that $V_{MICVDD}$ - $V_{MICBIASn}$ > 200mV | | | | | | |
| Minimum Bias Voltage | $V_{MICBIAS}$ | Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA | | 1.5 | | V |
| Maximum Bias Voltage | | | | 2.8 | | V |
| Bias Voltage output step size | | | | 0.1 | | V |
| Bias Voltage accuracy | | | -5% | | +5% | V |
| Bias Current | | Regulator mode (MICBn_BYPASS=0), $V_{MICVDD}$ - $V_{MICBIAS}$ >200mV | | | 2.4 | mA |
| | | Bypass mode (MICBn_BYPASS=1) | | | 5.0 | |
| Output Noise Density | | Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz | | 100 | | nV/√Hz |
| Integrated noise voltage | | Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted | | 5 | | μVrms |
| Power Supply Rejection Ratio (CPVDD) | PSRR | 100mV (peak-peak) 217Hz | 100 | | | dB |
| | | 100mV (peak-peak) 10kHz | 80 | | | |
| Load capacitance | | Regulator mode (MICBn_BYPASS=0) | | | 50 | pF |
| Output discharge resistance | | MICBn_ENA=0, MICBn_DISCH=1 | | 15 | | kΩ |
| **External Accessory Detect** | | | | | | |
| Load impedance detection range (HPDETL or HPDETR) | | | 8 | | 128 | Ω |
| Load impedance detection accuracy (HPDETL or HPDETR) | | | -30 | | +30 | % |
| Load impedance detection range (MICDET1 or MICDET2) 2.2kΩ (2%) MICBIAS resistor. Note these characteristics assume no other component is connected to MICDETn. | | for MICD_LVL[0] = 1 | 0 | | 3 | Ω |
| | | for MICD_LVL[1] = 1 | 17 | | 21 | |
| | | for MICD_LVL[2] = 1 | 36 | | 44 | |
| | | for MICD_LVL[3] = 1 | 62 | | 88 | |
| | | for MICD_LVL[4] = 1 | 115 | | 160 | |
| | | for MICD_LVL[5] = 1 | 207 | | 381 | |
| | | for MICD_LVL[8] = 1 | 475 | | 30000 | |
| Jack Detection input threshold voltage (JACKDET) | $V_{JACKDET}$ | Jack insertion | | 0.5 x AVDD | | V |
| | | Jack removal | | 0.85 x AVDD | | |

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**Test Conditions**

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V, SPKVDDL = SPKVDDR = 4.2V,
$T_A$ = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **MICVDD Regulator (LDO2)** | | | | | | |
| Output voltage | $V_{MICVDD}$ | | 1.7 | 2.7 | 3.3 | V |
| Programmable output voltage step size | | LDO2_VSEL=00h to 14h (0.9V to 1.4V) | | 25 | | mV |
| | | LDO2_VSEL=14h to 27h (1.4V to 3.3V) | | 100 | | |
| Maximum output current | | | | 8 | | mA |
| Start-up time | | 4.7µF on MICVDD | | | 1.5 | ms |
| **Frequency Locked Loop (FLL1, FLL2)** | | | | | | |
| Output frequency | | | 39 | | 298 | MHz |
| Lock Time | | $F_{REF}$ = 32kHz, $F_{OUT}$ = 24.576MHz | | | 2 | ms |
| | | $F_{REF}$ = 12MHz, $F_{OUT}$ = 24.576MHz | | | 0.3 | |
| **RESET pin Input** | | | | | | |
| RESET de-bounce time (The RESET input may be ignored if asserted for less than this duration) | $V_{IH}$ | | | | TBD | µs |
| **Device Reset Thresholds** | | | | | | |
| AVDD Reset Threshold | $V_{AVDD}$ | | 0.6 | | 1.5 | V |
| DCVDD Reset Threshold | $V_{DCVDD}$ | | 0.4 | | 0.7 | V |
| DBVDD2 Reset Threshold | $V_{DBVDD2}$ | | 0.4 | | 0.7 | V |
| Note that the reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in the "Recommended Operating Conditions" section. Refer to this section for the WM5110 power-up sequencing requirements. | | | | | | |

## TERMINOLOGY

1.  Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied. (Note that this is measured without any mute function enabled.)

2.  Total Harmonic Distortion (dB) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.

3.  Total Harmonic Distortion plus Noise (dB) – THD+N is the ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.

4.  Power Supply Rejection Ratio (dB) - PSRR is the ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.

5.  Common Mode Rejection Ratio (dB) – CMRR is the ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.

6.  Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.

7.  Multi-Path Crosstalk (dB) – is the difference in level between the output of the active path and the measured signal level in the idle path at the test signal frequency. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.

8.  Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

9.  All performance measurements are specified with a 20kHz low pass 'brick-wall' filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise.

## DEVICE DESCRIPTION

### INTRODUCTION

The WM5110 is a highly integrated low-power audio hub CODEC for mobile telephony and portable devices. It provides flexible, high-performance audio interfacing for handheld devices in a small and cost-effective package. It provides exceptional levels of performance and signal processing capability, suitable for a wide variety of mobile and handheld devices.

The WM5110 digital core incorporates the Wolfson MyZone™ Ambient Noise Cancellation (ANC), and provides an extensive capability for programmable signal processing algorithms, including receive (RX) path noise cancellation, transmit (TX) path noise reduction, Acoustic Echo Cancellation (AEC) and microphone beam-forming algorithms.

The WM5110 digital core supports audio enhancements such as Dynamic Range Control (DRC), Multi-band Compression (MBC), Virtual Surround Sound (VSS), Speaker Protection and Bass Enhancement. Highly flexible digital mixing, including stereo full-duplex asynchronous sample rate conversion, provides use-case flexibility across a broad range of system architectures.

The WM5110 provides multiple digital audio interfaces, including SLIMbus, in order to provide independent and fully asynchronous connections to different processors (eg. application processor, baseband processor and wireless transceiver).

A flexible clocking arrangement supports a wide variety of external clock references, including clocking derived from the digital audio interface. Two integrated Frequency Locked Loop (FLL) circuits provide additional flexibility.

Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, and support for external accessory / push-button detection inputs. Comprehensive Interrupt (IRQ) logic and status readback are also provided.

### HI-FI AUDIO CODEC

The WM5110 is a high-performance low-power audio CODEC which uses a simple analogue architecture. 6 ADCs and 8 DACs are incorporated, providing a dedicated ADC for each analogue input and a dedicated DAC for each output channel.

The analogue outputs comprise three 30mW (110dB SNR) stereo headphone amplifiers with ground-referenced output, and a Class D mono speaker driver capable of delivering 2W per channel into a 4Ω load. Six analogue inputs are provided, each supporting single-ended or differential input modes. In differential mode, the input path SNR is 106dB (16kHz sample rate, ie. wideband voice mode). The ADC input paths can be bypassed, supporting up to 8 channels of digital microphone input.

The audio CODEC is controlled directly via register access. The simple analogue architecture, combined with the integrated tone generator, enables simple device configuration and testing, minimising debug time and reducing software effort.

The WM5110 output drivers are designed to support as many different system architectures as possible. Each output has a dedicated DAC which allows mixing, equalisation, filtering, gain and other audio processing to be configured independently for each channel. This allows each signal path to be individually tailored for the load characteristics. All outputs have integrated pop and click suppression features.

The headphone output drivers are ground-referenced, powered from an integrated charge pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. Ground loop feedback is incorporated, providing rejection of noise on the ground connections. A mono mode is available on the headphone outputs; this configures the drivers as differential (BTL) outputs, suitable for an earpiece or hearing aid coil.

The Class D speaker drivers deliver excellent power efficiency. High PSRR, low leakage and optimised supply voltage ranges enable powering from switching regulators or directly from the battery. Battery current consumption is minimised across a wide variety of voice communication and multimedia playback use cases.

The WM5110 is cost-optimised for a wide range of mobile phone applications, and features two channels of Class D power amplification. For applications requiring more than two channels of power amplification, the PDM output channels can be used to drive up to four external PDM-input speaker drivers. In applications where stereo loudspeakers are physically widely separated, the PDM outputs can ease layout and EMC by avoiding the need to run the Class-D speaker outputs over long distances and interconnects.

## DIGITAL AUDIO CORE

The WM5110 uses a core architecture based on all-digital signal routing, making digital audio effects available on all signal paths, regardless of whether the source data input is analogue or digital. The digital mixing desk allows different audio effects to be applied simultaneously on many independent paths, whilst also supporting a variety of sample rates concurrently. This helps support many new audio use-cases. Soft mute and un-mute control allows smooth transitions between use-cases without interrupting existing audio streams elsewhere.

The Wolfson myZone™ Ambient Noise Cancellation (ANC) processor within the WM5110 provides the capability to improve the intelligibility of a voice call by using destructive interference to reduce the acoustic energy of the ambient sound. The stereo ANC capability supports a wide variety of headset/handset applications.

The Wolfson myZone™ technology supports receive (RX) path noise cancellation. Transmit (TX) path noise reduction, multi-mic Acoustic Echo Cancellation (AEC), and microphone beam-forming algorithms are also supported. The WM5110 is ideal for mobile telephony, providing enhanced voice communication quality for near-end and far-end handset users.

The WM5110 digital core provides an extensive capability for programmable signal processing algorithms. The DSP can support functions such as wind noise, side-tone and other programmable filters. A wide range of application-specific filters and audio enhancements can also be implemented, including Dynamic Range Control (DRC), Multi-band Compression (MBC), Virtual Surround Sound (VSS), Speaker Protection and Bass Enhancement. These digital effects can be used to improve audibility and stereo imaging while minimising supply current.

Highly flexible digital mixing, including mixing between audio interfaces, is possible. The WM5110 performs multi-channel full-duplex asynchronous sample rate conversion, providing use-case flexibility across a broad range of system architectures. Automatic sample rate detection is provided, enabling seamless wideband/narrowband voice call handover.

Dynamic Range Controller (DRC) functions are available for optimising audio signal levels. In playback modes, the DRC can be used to maximise loudness, while limiting the signal level to avoid distortion, clipping or battery droop, in particular for high-power output drivers such as speaker amplifiers. In record modes, the DRC assists in applications where the signal level is unpredictable.

The 5-band parametric equaliser (EQ) functions can be used to compensate for the frequency characteristics of the output transducers. EQ functions can be cascaded to provide additional frequency control. Programmable high-pass and low-pass filters are also available for general filtering applications such as removal of wind and other low-frequency noise.

## DIGITAL INTERFACES

Three serial digital audio interfaces (AIFs) each support PCM, TDM and I2S data formats for compatibility with most industry-standard chipsets. AIF1 supports eight input/output channels; AIF2 and AIF3 each support two input/output channels. Bidirectional operation at sample rates up to 192kHz is supported.

Eight digital PDM input channels are available (four stereo interfaces); these are typically used for digital microphones, powered from the integrated MICBIAS power supply regulators. Four PDM output channels are also available (two stereo interfaces); these are typically used for external power amplifiers. Embedded mute codes provide a control mechanism for external PDM-input devices.

The WM5110 features a MIPI-compliant SLIMbus interface, providing eight channels of audio input/output. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the WM5110 control registers.

The WM5110 is equipped with an I2C/SPI control interface and an I2C-only control interface. The I2C slave port operates up to 1MHz; the SPI ports operate up to 26MHz. Full access to the register map is also provided via the SLIMbus port.

## OTHER FEATURES

The WM5110 incorporates two 1kHz tone generators which can be used for 'beep' functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

A white noise generator is provided, which can be routed within the digital core. The noise generator can provide 'comfort noise' in cases where silence (digital mute) is not desirable.

Two Pulse Width Modulation (PWM) signal generators are incorporated. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting. The PWM signal generators can be output directly on a GPIO pin.
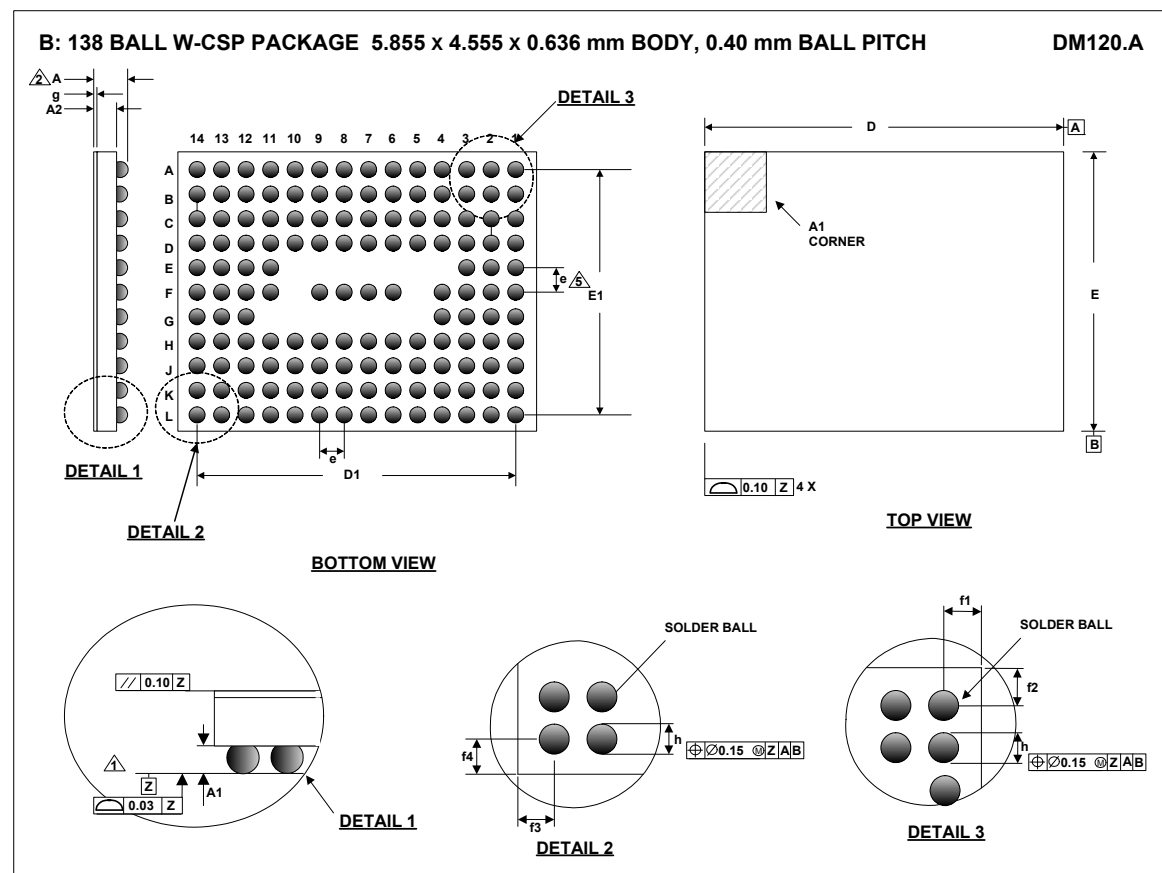
The WM5110 provides 5 GPIO pins, supporting selectable input/output functions for interfacing, detection of external hardware, and to provide logic outputs to other devices. Comprehensive Interrupt (IRQ) functionality is also provided for monitoring internal and external event conditions.

The WM5110 can be powered from a 1.8V external supply. A separate supply (4.2V) is typically required for the Class D speaker driver. Integrated Charge Pump and LDO Regulators circuits are used to generate supply rails for internal functions and to support powering or biasing of external microphones.

A smart accessory interface is included, supporting most standard 3.5mm accessories. Jack detection, accessory sensing and impedance measurement is provided, for external accessory and push-button detection. 'Switchable ground' features enable support for different headset types. Microphone activity detection with interrupt is also available.

System clocking can be derived from the MCLK1 or MCLK2 input pins. Alternatively, the SLIMbus interface, or the audio interfaces (configured in Slave mode), can be used to provide a clock reference. Two integrated Frequency Locked Loop (FLL) circuits provide support for a wide range of clocking configurations, including the use of a 32kHz input clock reference.

# RECOMMENDED EXTERNAL COMPONENTS

4.2V  1.8V  1.2V

1.0μF

DCVDD
LDOVOUT
LDOVDD

SPKVDDL
SPKVDDR
CPVDD
AVDD1
AVDD2
DBVDD1
DBVDD2
DBVDD3

4.7μF  4.7μF

4.7μF

2 x 1μF  3 x 0.1μF

LDO Control — LDOENA
Reset Control — RESET
Interrupt Output — IRQ

SLIMbus Interface — SLIMCLK / SLIMDAT

Audio Interface 1 — AIF1BCLK / AIF1LRCLK / AIF1RXDAT / AIF1TXDAT

Audio Interface 2 — AIF2BCLK / AIF2LRCLK / AIF2RXDAT / AIF2TXDAT

**WM5110**

Audio Interface 3 — AIF3BCLK / AIF3LRCLK / AIF3RXDAT / AIF3TXDAT

Differential Microphone connection

MICBIAS1
2.2kΩ
1μF
1μF
2.2kΩ

MICDET1/HPOUT1FB2
IN1LN/DMICCLK1
IN1LP
IN1RN/DMICDAT1
IN1RP

Single-ended Line connection
1μF  IN2LN/DMICCLK2
IN2LP
1μF  IN2RN/DMICDAT2
IN2RP

MICBIAS2

VDD / CHAN / GND — DMIC — CLK / DAT
IN3LN/DMICCLK3
IN3LP
IN3RN/DMICDAT3
IN3RP
DMICCLK4

VDD / CHAN / GND — DMIC — CLK / DAT
DMICDAT4

Stereo Digital Microphone connection

Analogue and Digital Inputs

Bias / Supplies for Microphones and External Accessory Detection
MICBIAS1
MICBIAS2
MICBIAS3
MICVDD
4.7μF

SPKGNDL  SPKGNDR  AGND  CPGND  DGND  SUBGND

VREFC  2.2μF

CIF2SDA / CIF2SCLK — Control Interface 2

CIF1MODE
CIF1ADDR/CIF1SS
CIF1SCLK
CIF1SDA/CIF1MOSI
CIF1MISO/GPIO4 — Control Interface 1

MCLK1 / MCLK2 — Master Clocks

GPIO1 / GPIO2 / GPIO3 / GPIO5 — GPIO

CP1C1A  2.2μF
CP1C1B
CP1VOUT1P  4.7μF
CP1VOUT1N  4.7μF
CP1C2A  2.2μF
CP1C2B
CP1VOUT2P  4.7μF
CP1VOUT2N  4.7μF

CP2CA  470nF
CP2CB
CP2VOUT  4.7μF

JACKDET — Jack Detect input

HPOUT1L
HPOUT1R — Headphone
HPOUT1FB1/MICDET2
HPDETL
HPDETR

(Note: HPOUT1FB ground connection close to headset jack)

HPOUT2L
HPOUT2R — Line Output
HPOUT2FB

(Note: HPOUT2FB ground connection close to headset jack)

HPOUT3L
HPOUT3R — Earpiece Speaker
HPOUT3FB

Outputs HPOUT1, HPOUT2 and HPOUT3 can be configured as Stereo pairs or Differential Mono.

SPKOUTLN
SPKOUTLP — Loudspeaker

SPKOUTRN
SPKOUTRP — Loudspeaker

SPKCLK1
SPKDAT1
SPKCLK2
SPKDAT2 — Digital Speaker (PDM) interface

## PACKAGE DIMENSIONS

**B: 138 BALL W-CSP PACKAGE  5.855 x 4.555 x 0.636 mm BODY, 0.40 mm BALL PITCH**     **DM120.A**



BOTTOM VIEW

TOP VIEW

DETAIL 1

DETAIL 2

DETAIL 3

| Symbols | Dimensions (mm) | | | |
|---|---|---|---|---|
| | MIN | NOM | MAX | NOTE |
| A | 0.592 | 0.636 | 0.681 | |
| A1 | 0.175 | 0.190 | 0.205 | |
| A2 | 0.417 | 0.446 | 0.476 | |
| D | 5.800 | 5.855 | 5.880 | |
| D1 | | 5.20 BSC | | |
| E | 4.500 | 4.555 | 4.580 | |
| E1 | | 4.00 BSC | | |
| e | | 0.40 BSC | | 5 |
| f1 | | 0.3275 BSC | | |
| f2 | | 0.2775 BSC | | |
| f3 | | 0.3275 BSC | | |
| f4 | | 0.2775 BSC | | |
| g | 0.036 | 0.040 | 0.044 | |
| h | 0.216 | 0.270 | 0.324 | |

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1'.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.

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## REVISION HISTORY

| DATE | REV | DESCRIPTION OF CHANGES | PAGE | CHANGED BY |
|---|---|---|---|---|
| 18/04/12 | 1.0 | First Release | | |
| 22/05/12 | 1.1 | Correction to AIF2BCLK pin number | 5 | PH |
| 08/06/12 | 1.2 | Sample rates greater than 192kHz deleted<br>DCVDD domain can be powered from LDO1<br>Single-ended analogue input pins are INnxN (not INnxP)<br>MICVDD=2.5V added to generic Test Conditions for Elec Chars | | PH |
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